LP339 - Ultra-Low Power Quad Comparator

Features

- Ultra-low power supply current drain (60 µA)-independent of the supply voltage (75 µW/comparator at +5 V_{DC})
- Low input biasing current: 3 nA
- Low input offset current: ±0.5 nA
- Low input offset voltage: ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O=2 V_{DC})
- Supply Input protected against reverse voltages

Applications

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Parametric Table

Response Time	8 us
Output Bus	Open Drain
Supply Min	2 Volt
Supply Max	36 Volt
Channels	4 Channels
Offset Voltage max, 25C	5 mV
Output Current	30 mA
Input Range	Vcm to V-
Supply Current Per Channel	0.02125 mA
PowerWise Rating 3	170 uA x us
Max Input Bias Current	40 nA
Special Features	Undefined
Temperature Min	0 deg C
Temperature Max	70 deg C
Function	Comparator

Datasheet

RoHS Compliance Information

LP339 Ultra-Low Power Quad Comparator

LP339 Ultra-Low Power Quad Comparator (**Japanese**)

Package Availability, Models

Part Number	Package							Factory Lead Time		Models				td Pack Size	Package Marking Format
	Type	Pins	Spec.	MSL Rating	Peak Reflow	RoHS Report		Weeks	Qty						
LP339M	SOIC NARROW	14	STD	1	235	RoHS		Full production		N/A				rail of 55	NSUZXYTT LP339M
			NOPB	1	260			6 weeks	2000						
LP339MX	SOIC NARROW	14	STD	1	235	RoHS		Full production		N/A				reel of 2500	NSUZXYTT LP339M
			NOPB	1	260			6 weeks	7500						
LP339N	MDIP	14	STD	1	NA	RoHS		Full production		N/A				rail of 25	NSUZXYYTTE# LP339N
			NOPB	1	NA			6 weeks	2000						
LP339 MWA	Wafer							Obsolete		N/A				wafer jar of N/A	-
								N/A	N/A						

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 µA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

Reliability Metrics

Part Number	Process	EFR Reject	EFR Sample Size	PPM *	LTA Rejects	LTA Device Hours	FITS	MTTF (Hours)
LP339 MWA	SLM	0	42786	0	0	3352500	2	951281028
LP339M	SLM	0	42786	0	0	3352500	2	951281028
LP339MX	SLM	0	42786	0	0	3352500	2	951281028
LP339N	SLM	0	42786	0	0	3352500	2	951281028

Note: The Early Failure Rates were calculated as point estimates. The Long Term Failure Rates were calculated at 60% confidence using the Arrhenius equation at 0.7eV activation energy and derating the assumed stress temperature of 150°C to an application temperature of 55°C.

National Semiconductor

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Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Features

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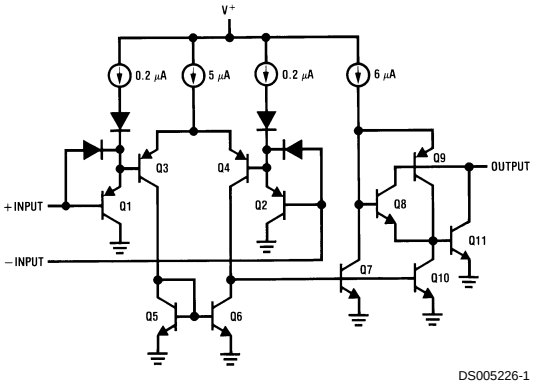
Schematic and Connection Diagrams



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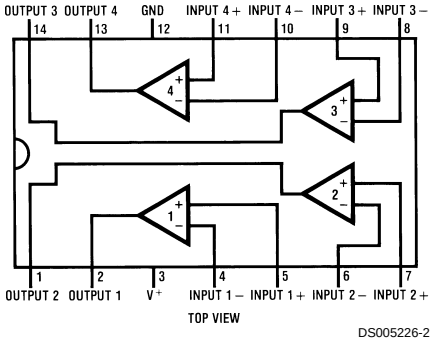

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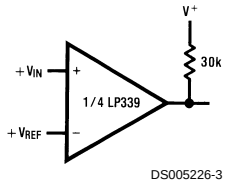
Order Number LP339M for S.O. Package
See NS Package Number M14A
Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

Typical Applications (V^+= 5.0 V_{DC})

Basic Comparator



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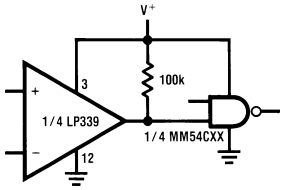
Driving CMOS



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 2)	
Molded DIP	570 mW
Output Short Circuit to GND (Note 3)	Continuous
Input Current V_{IN}<−0.3 V_{DC} (Note 4)	50 mA
Operating Temperature Range	0˚C to +70˚C
Storage Temperature Range	−65˚ to +150˚C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260˚C
S.O. Package:	
Vapor Phase (60 sec.)	+215˚C
Infrared (15 sec.)	+220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics

(V+=5 V_{DC}) (Note 5)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	T_A=25˚C (Note 10)		±2	±5	mV_{DC}
Input Bias Current	I_{IN}(+) or I_{IN}(−) with the Output in the Linear Range, T_A=25˚C (Note 6)		2.5	25	nA_{DC}
Input Offset Current	I_{IN}(+)−I_{IN}(−), T_A=25˚C		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	T_A=25˚C (Note 7)	0		V+−1.5	V_{DC}
Supply Current	R_L=Infinite on all Comparators, T_A=25˚C		60	100	μA_{DC}
Voltage Gain	V_O = 1 V_{DC} to 11 V_{DC}, R_L=15 kΩ, V^+=15 V_{DC}, T_A=25˚C		500		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25˚C		1.3		µSec
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25˚C (Note 8)		8		µSec
Output Sink Current	V_{IN}(−)=1 V_{DC}, V_{IN}(+)=0, V_O=2 V_{DC}, T_A=25˚C (Note 12)	15	30		mA_{DC}
	V_O=0.4 V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	V_{IN}(+)=1 V_{DC}, V_{IN}(−)=0, V_O=5 V_{DC}, T_A=25˚C		0.1		nA_{DC}
Input Offset Voltage	(Note 10)			±9	mV_{DC}
Input Offset Current	I_{IN}(+)−I_{IN}(−)		±1	±15	nA_{DC}
Input Bias Current	I_{IN}(+) or I_{IN}(−) with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		V+−2.0	V_{DC}
Output Sink Current	V_{IN}(−)=1 V_{DC}, V_{IN}(+)=0, V_O=2 V_{DC}	10			mA_{DC}
Output Leakage Current	V_{IN}(+)=1 V_{DC}, V_{IN}(−)=0, V_O=30 V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All $V_{IN'S}$≥0 V_{DC} (or V^- on split supplies) (Note 9)			36	V_{DC}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For elevated temperature operation, T_j max is 125˚C for the LP339. θ_{ja} (junction to ambient) is 175˚C/W for the LP339N and 120˚C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the “ON-OFF” characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} (T_A=25˚C).

Note 5: These specifications apply for V^+=5V_{DC} and 0˚C≤T_A≤70˚ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 7: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V (T_A=25˚C), but either or both inputs can go to 30 V_{DC} without damage.

Note 8: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 µs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics (Continued)

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at T_A=25˚C.

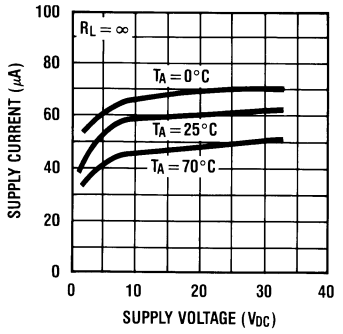
Note 10: At output switch point, V_O=1.4V, R_S=0Ω with V^+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+−1.5 V_{DC}).

Note 11: For input signals that exceed V^+, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Note 12: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).

Typical Performance Characteristics

Supply Current



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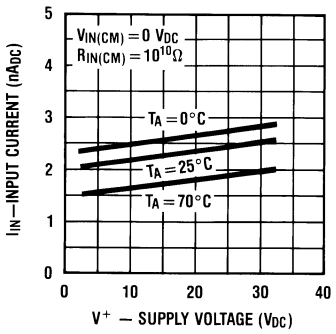
Input Current



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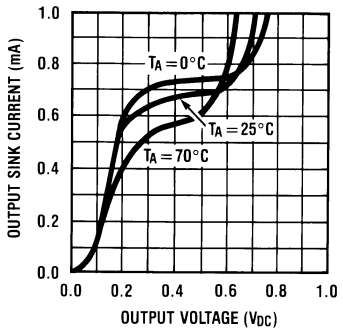
Output Sink Current



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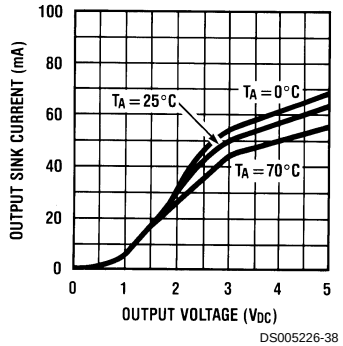
Output Sink Current



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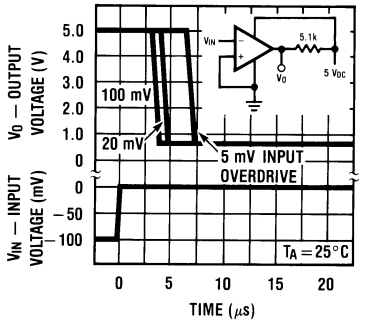
Response Times for Various Input Overdrives — Negative Transition



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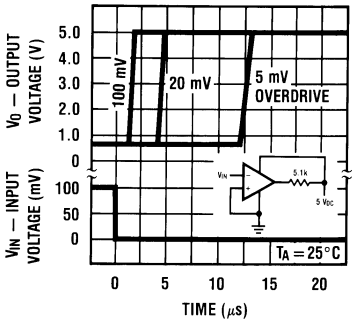
Response Times for Various Input Overdrives — Positive Transition



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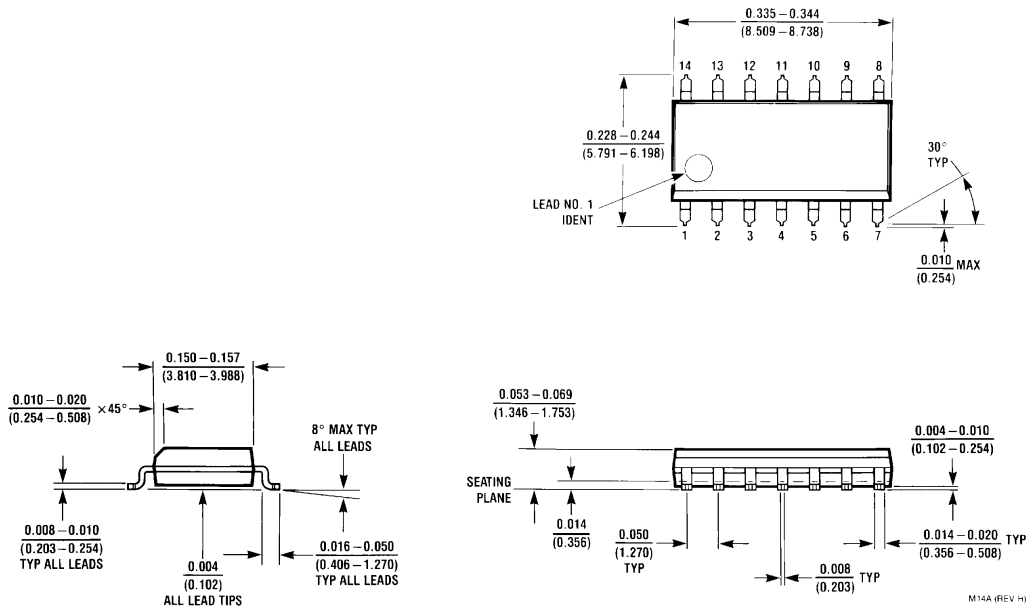
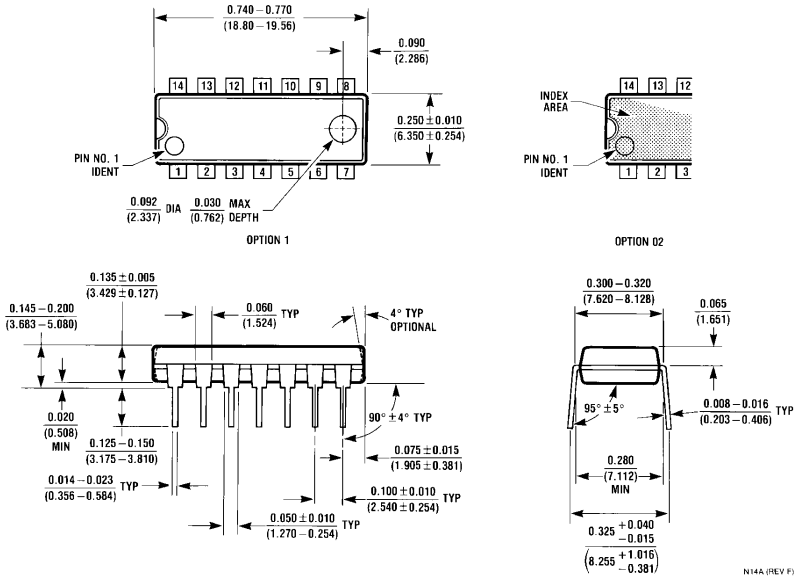
Physical Dimensions inches (millimeters) unless otherwise noted



S.O. Package (M)
Order Number LP339M or LP339MX
NS Package M14A



Molded Dual-In-Line Package (N)
Order Number LP339N
NS Package Number N14A