REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. - ro	02-03-07	R. MONNIN

REV																				
SHEET																				
REV	A	A	A	A	A															
SHEET	15	16	17	18	19															

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
93-11-05

MICROCIRCUIT, LINEAR, 12-BIT ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
A	A	**67268**	**5962-93164**

SHEET 1 OF 19

DSCC FORM 2233
APR 97

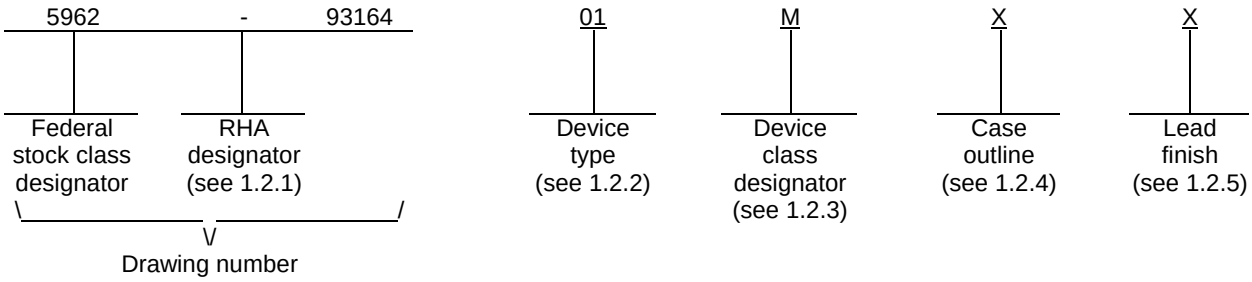
5962-E217-02

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD1674	12-Bit analog-to-digital converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. (unless otherwise specified, T_A = +25°C)

V_{CC} to digital common	+16.5 V
V_{EE} to digital common	-16.5 V
V_{LOGIC} to digital common	+7 V
Analog common to digital common	±1.0 V
Control inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to digital common	-0.5 V to V_{LOGIC} +0.5 V
Analog inputs (REF IN, BIP OFF, 10 V_{IN}) to analog common	V_{EE} to V_{CC}
20 V_{IN} to analog common	V_{EE} to +24 V
REF OUT	Indefinite short to common Momentary short to V_{CC}
Power dissipation (P_D)	825 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	60°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to 125°C
Operating voltage range:	
V_{CC} to digital common	+11.4 V dc to +16.5 V dc
V_{EE} to digital common	-11.4 V dc to -16.5 V dc
V_{LOGIC} to digital common	+4.5 V dc to +5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power dissipation	P_D	Three-stated outputs	1,2,3	01		575	mW
Input resistance	R_{IN}	10 V span, T_A = +25°C	1	01	3	7	kΩ
		20 V span, T_A = +25°C			6	14	
Internal reference 2/ output voltage	V_{REF}	Bipolar 20 V span, 2.0 mA external load, T_A = +25°C	1	01	9.9	10.1	V
Logic input high voltage (CE, $\overline{CS}$, R/$\overline{C}$, A_0)	V_{IH}		1,2,3	01	2.0		V
Logic input high voltage (CE, $\overline{CS}$, R/$\overline{C}$, A_0)	V_{IL}		1,2,3	01		0.8	V
Logic input current (CE, $\overline{CS}$, R/$\overline{C}$, A_0)	I_{LIN}	V_{IH} = 5.0 V, V_{IL} = 0.0 V	1,2,3	01	-10	+10	µA
Logic output high voltage (DB11-DB0)	V_{OH}	I_{SOURCE} = 500 µA	1,2,3	01	2.4		V
Logic output low voltage (DB11-DB0, STS)	V_{OL}	I_{SINK} = 1.6 mA	1,2,3	01		0.4	V
Three-state output leakage (DB11-DB0)	I_{OLT}	Outputs three-stated, V_{IH} = 5.0 V	1,2,3	01	-10	+10	µA
Power supply current	I_{LOGIC}	Outputs three-stated, REF OUT to REF IN through 50 Ω, V_{CC} = 16.5 V, V_{EE} = -16.5 V, V_{LOGIC} = 5.5 V	1,2,3	01		8	mA
	I_{CC}					14	
	I_{EE}					18	
Integral nonlinearity	INL	Major transitions, unipolar 10 V span, bipolar 20 V span	1	01	-0.5	+0.5	LSB
			2,3		-1.0	+1.0	
Differential nonlinearity 3/	DNL	All codes tested, unipolar 10 V span, bipolar 20 V span	1,2,3	01	12		Bits

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection 4/	PSR	Unipolar-10 V span 5/	1,2,3	01	-1	+1	LSB
		6/			-0.5	+0.5	
		7/			-1	+1	
Unipolar offset error	V_{OSE}	10 V span, T_A = +25°C	1	01	-2	+2	LSB
Unipolar offset drift	TC_{VOS}	10 V span	2,3	01	-1	+1	LSB
Bipolar offset error	B_{POE}	20 V span, T_A = +25°C	1	01	-3	+3	LSB
Bipolar offset drift	TCB_{POE}	20 V span	2,3	01	-2	+2	LSB
Full-scale calibration error	A_B	Bipolar 20 V span, T_A = +25°C	1	01	-0.125	+0.125	% of FSR
	A_U	Unipolar 10 V span, T_A = +25°C			-0.125	+0.125	
Full-scale calibration drift	TCA_E	Bipolar 20 V span	2,3	01	-7	+7	LSB
Signal to noise and distortion	S/(N+D)	f_{IN} = 10 kHz, f_{SAMPLE} = 100 kSPS	4,5,6	01	70		dB
Total harmonic distortion	THD	f_{IN} = 10 kHz, f_{SAMPLE} = 100 kSPS	4,5,6	01		-82	dB
Peak spurious or harmonic component		f_{IN} = 10 kHz, f_{SAMPLE} = 100 kSPS	4,5,6	01		-82	dB
Intermodulation 8/ distortion	IMD	Second order products	4,5,6	01		-80	dB
		Third order products				-80	
Functional tests		See 4.4.1b	7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Converter start timing section (see figure 4)							
Conversion time	t_C	8-bit cycle	9,10,11	01		8	µs
		12-bits cycle				10	
STS delay from CE	t_{DSC}		9	01		200	ns
			10,11			225	
CE pulse width	t_{HEC}		9,10,11	01	50		ns
$\overline{CS}$ to CE setup	t_{SSC}		9,10,11	01	50		ns
$\overline{CS}$ low during CE high	t_{HSC}		9,10,11	01	50		ns
R/$\overline{C}$ to CE setup	t_{SRC}		9,10,11	01	50		ns
R/$\overline{C}$ low during CE high	t_{HRC}		9,10,11	01	50		ns
A_O to CE setup	t_{SAC}		9,10,11	01	0		ns
A_O valid during CE high	t_{HAC}		9,10,11	01	50		ns
Read timing full control mode section (see figure 5)							
Access time	t_{DD}	See figures 8 and 9	9,10,11	01		150	ns
Data valid after CE low	t_{HD}	See figures 8 and 9	9	01	25		ns
			10,11		15		
Output float delay	t_{HL}	See figures 8 and 9	9,10,11	01		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read timing full control mode section - continued (see figure 5)							
$\overline{CS}$ to CE setup	t_{SSR}		9,10,11	01	50		ns
R/$\overline{C}$ to CE setup	t_{SRR}		9,10,11	01	0		ns
A_O to CE setup	t_{SAR}		9,10,11	01	50		ns
$\overline{CS}$ valid after CE low	t_{HSR}		9,10,11	01	0		ns
R/$\overline{C}$ high after CE low	t_{HRR}		9,10,11	01	0		ns
A_O valid after CE low	t_{HAR}		9,10,11	01	50		ns
Read timing stand alone mode (see figures 6 and 7)							
Data access time	t_{DDR}	See figures 8 and 9	9,10,11	01		150	ns
Low R/$\overline{C}$ pulse width	t_{HRL}		9,10,11	01	50		ns
STS delay from R/$\overline{C}$	t_{DS}		9	01		200	ns
			10,11			225	
Data valid after R/$\overline{C}$ low	t_{HDR}	See figures 8 and 9	9,10,11	01	25		ns
STS delay after data valid	t_{HS}		9,10,11	01	0.6	1.2	µs
High R/$\overline{C}$ pulse width	t_{HRH}		9,10,11	01	150		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

1/ Unless otherwise specified, T_{MIN} to T_{MAX}, V_{CC} = +15 V ±10% or +12 V ±5%, V_{LOGIC} = +5 V ±10%, V_{EE} = -15 V ±10% or -12 V ±5%; 12/8 connected to V_{LOGIC}, A_0 and $\overline{CS}$ at logic "0", CE at logic "1." 10 V unipolar-50 Ω resistor REF OUT to REF IN, 50 Ω resistor BIP OFF to ground. Analog input connected to 10 V_{IN}. 20 V bipolar-50 Ω resistor REF OUT to BIP OFF, 50 Ω resistor REF OUT to REF IN. Analog input connected to 20 V_{IN}.

2/ The reference should be buffered for operation on ±12 V supplies.

3/ Minimum resolution for which no missing codes are guaranteed.

4/ Change in the full-scale unipolar 10 V span as power supply voltage is varied from min to max specified value.

5/ Test conditions for PSRR: 13.5 V ≤ V_{CC} ≤ 16.5 V, V_{LOGIC} = 5 V, V_{EE} = -15 V; 11.4 V ≤ V_{CC} ≤ 12.6 V, V_{LOGIC} = 5 V, V_{EE} = -12 V.

6/ 4.5 V ≤ V_{LOGIC} ≤ 5.5 V, V_{CC} = 15 V, V_{EE} = -15 V.

7/ -16.5 V ≤ V_{EE} ≤ -13.5 V, V_{LOGIC} = 5 V, V_{CC} = 15 V; -12.6 V ≤ V_{EE} ≤ -11.4 V, V_{LOGIC} = 5 V, V_{CC} = 12 V.

8/ fa = 9.08 kHz, fb = 9.58 kHz with f_{SAMPLE} = 100 kHz.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 93 (see MIL-PRF-38535, appendix A).

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	V_{LOGIC}
2	$12/\overline{8}$
3	$\overline{CS}$
4	A_O
5	$R/\overline{C}$
6	CE
7	V_{CC}
8	REF_{OUT}
9	AC
10	REF_{IN}
11	V_{EE}
12	BIP OFF
13	10 V_{IN}
14	20 V_{IN}
15	DC
16	DBO
17	DB1
18	DB2
19	DB3
20	DB4
21	DB5
22	DB6
23	DB7
24	DB8
25	DB9
26	DB10
27	DB11
28	STS

FIGURE 1. Terminal connections.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_O	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12 bit conversion
1	0	0	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs and 4 trailing zeros

FIGURE 2. Truth table.

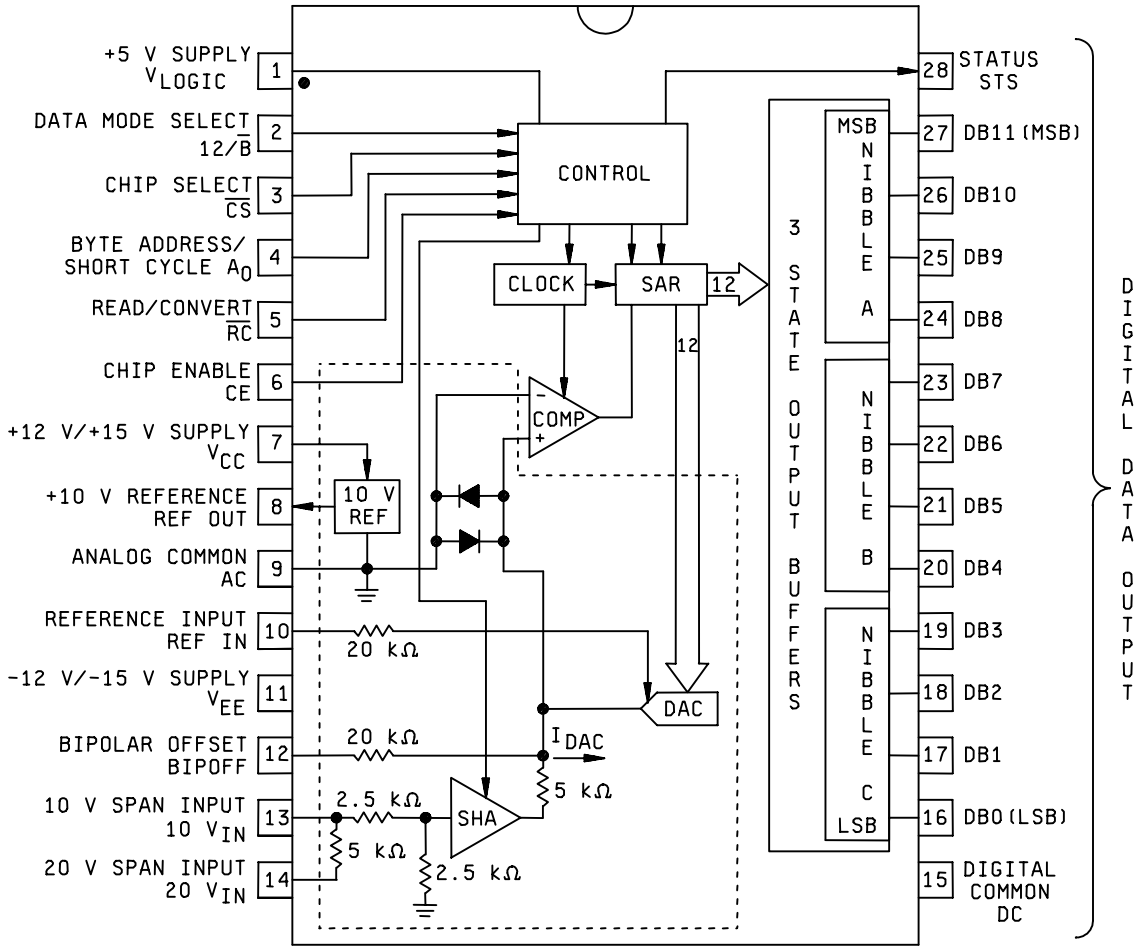


FIGURE 3. Functional block diagram.

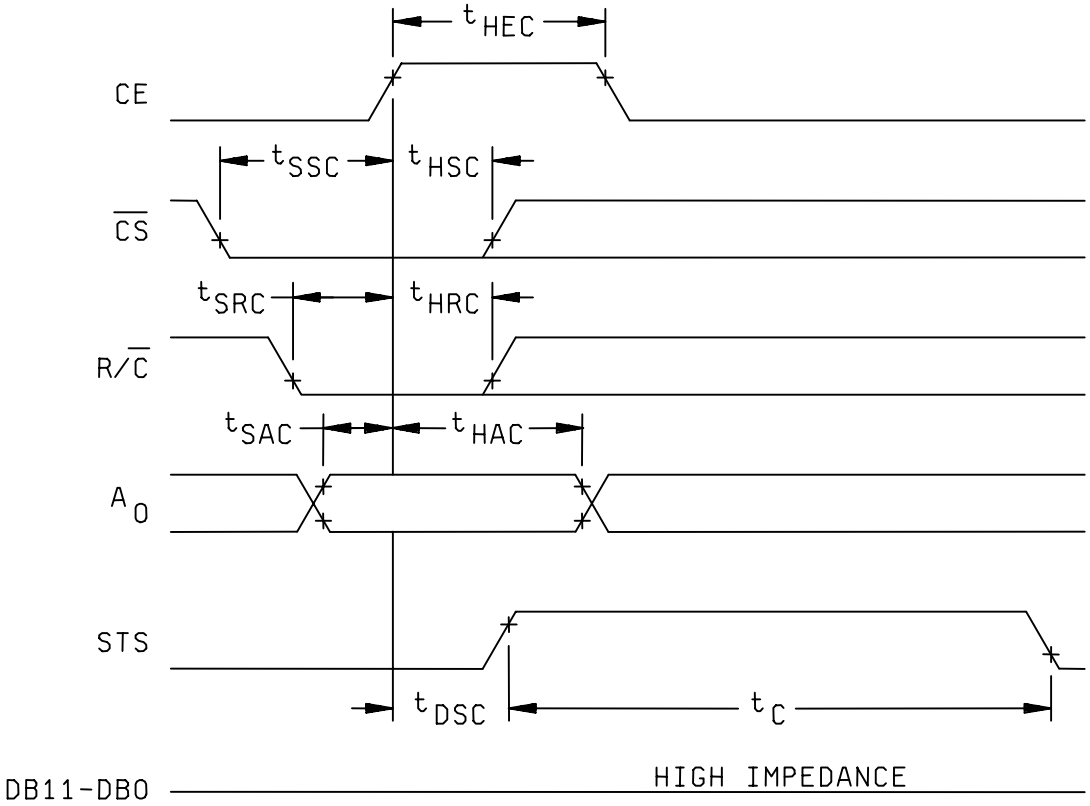


FIGURE 4. Converter start timing diagram.

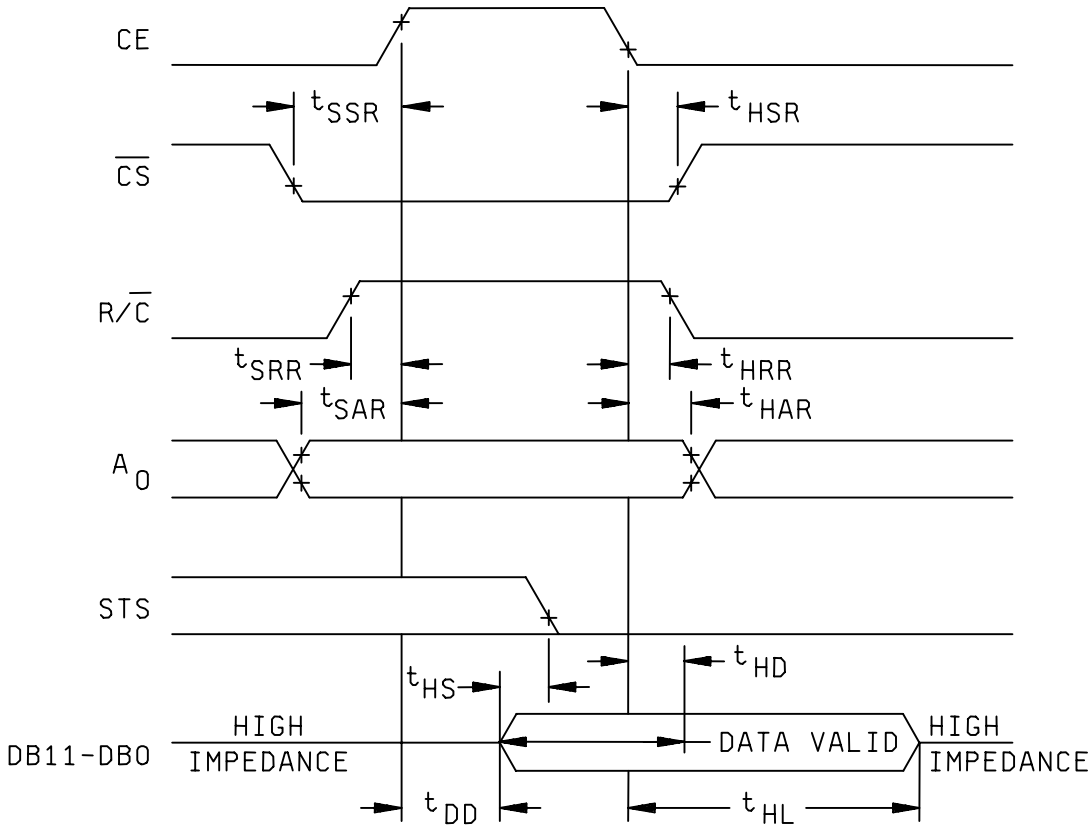


FIGURE 5. Read timing diagram.

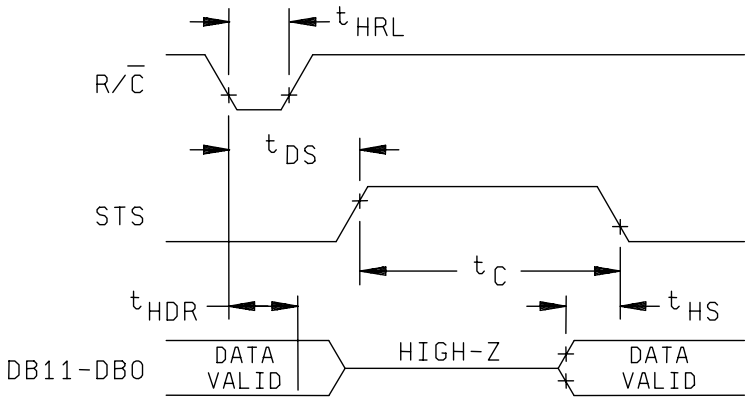


FIGURE 6. Stand-alone mode timing low pulse for R/C diagram.

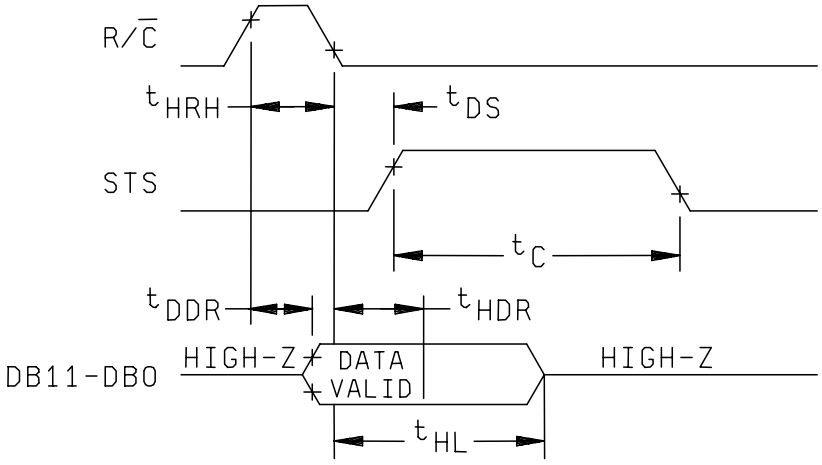


FIGURE 7. Stand-alone mode timing high pulse for R/C diagram.

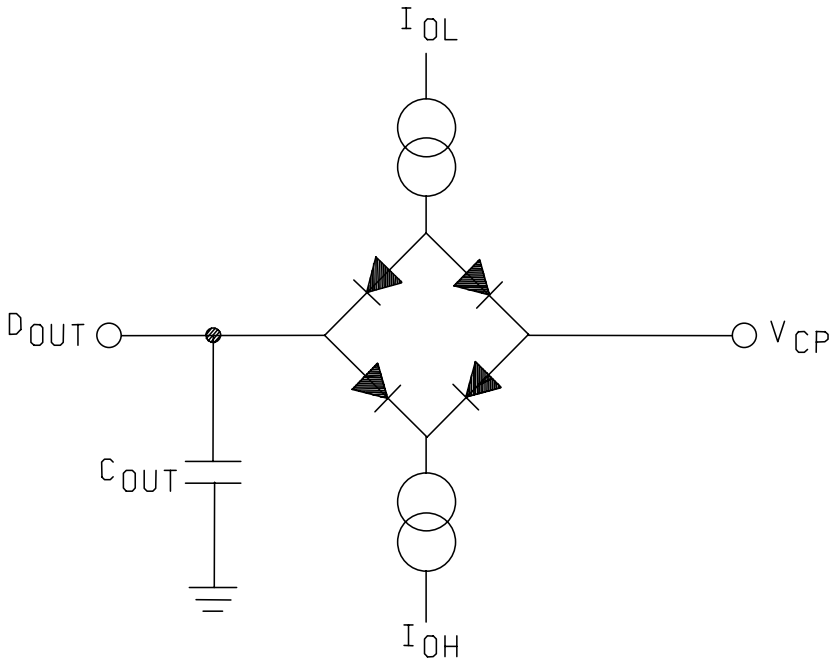


FIGURE 8. Load circuit for bus timing specifications.

Test	V_{CP}	C_{OUT}
Access time high Z to logic low	5 V	100 pF
Float time logic high to high Z	0 V	10 pF
Access time high Z to logic high	0 V	100 pF
Float time logic low to high Z	5 V	10 pF

FIGURE 9. Load conditions for bus timing specifications.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,9 1/	1,2,3,9 1/	1,2,3,9 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6,9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3
Group D end-point electrical parameters (see 4.4)	1	1	1,2,3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-03-07

Approved sources of supply for SMD 5962-93164 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9316401MXA	24355	AD1674TD/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.