

FEATURES

High-Definition Multimedia Interface (HDMI) 1.4a features supported

All mandatory and additional 3D video formats supported

Extended colorimetry, including sYCC601, Adobe RGB, Adobe YCC 601, xvYCC extended gamut color

CEC 1.4-compatible

HDMI receiver

165 MHz maximum TMDS clock frequency

24-bit output pixel bus

High-bandwidth Digital Content Protection (HDCP) 1.4 support with internal HDCP keys

HDCP repeater support

Up to 127 KSVs supported

Integrated CEC controller

Programmable HDMI equalizer

5 V detect and Hot Plug assert for HDMI port

Audio support

SPDIF (IEC 60958-compatible) digital audio

HDMI audio extraction support

Advanced audio mute feature

Supports multiplexed (TDM) I²S

General

Interrupt controller with two interrupt outputs

Standard identification (STDI) circuit

Highly flexible 24-bit pixel output interface

Internal EDID RAM

Any-to-any 3 × 3 color space conversion (CSC) matrix

2-layer PCB design supported

64-lead LQFP_EP, 10 mm × 10 mm package

APPLICATIONS

Projectors

Automotive

Video conferencing

HDTVs

AVR, HTiB

Soundbars

Video switches

FUNCTIONAL BLOCK DIAGRAM

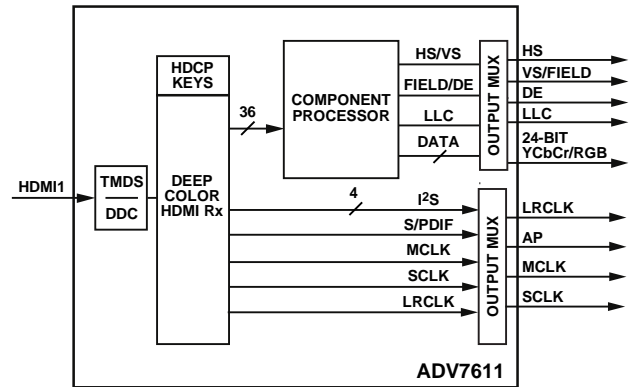


Figure 1.

08305-001

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Power-Up Sequence	11
Applications	1	Power-Down Sequence.....	11
Functional Block Diagram	1	Functional Overview.....	12
Revision History	2	HDMI Receiver.....	12
General Description	3	Component Processor	12
Detailed Functional Block Diagram	3	Other Features	12
Specifications.....	4	Time-Division Multiplexed (TDM) Mode	13
Electrical Characteristics	4	Pixel Input/Output Formatting	14
Data and I ² C Timing Characteristics.....	5	Pixel Data Output Modes Features	14
Absolute Maximum Ratings.....	8	Outline Dimensions	16
Package Thermal Performance.....	8	Ordering Guide	16
ESD Caution.....	8		
Pin Configuration and Function Descriptions.....	9		
Power Supply Sequencing.....	11		

REVISION HISTORY

11/10—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADV7611 is offered in automotive, professional (no HDCP), and industrial versions. The operating temperature range is -40°C to $+85^{\circ}\text{C}$.

The [UG-180](#) contains critical information that must be used in conjunction with the ADV7611.

The ADV7611 is a high quality, single input HDMI®-capable receiver. It incorporates an HDMI-capable receiver that supports all mandatory 3D TV defined in HDMI 1.4a. The ADV7611 supports formats up to UXGA 60 Hz at 8 bit.

It integrates a CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7611 has an audio output port for the audio data extracted from the HDMI stream. The HDMI receiver has an advanced mute controller that prevents audible extraneous noise in the audio output. Additionally, the ADV7611 can be set to output TDM I²S, which allows sending four multiplexed I²S channels.

The following audio formats are accessible:

- A stream from the I²S serializer (two audio channels)

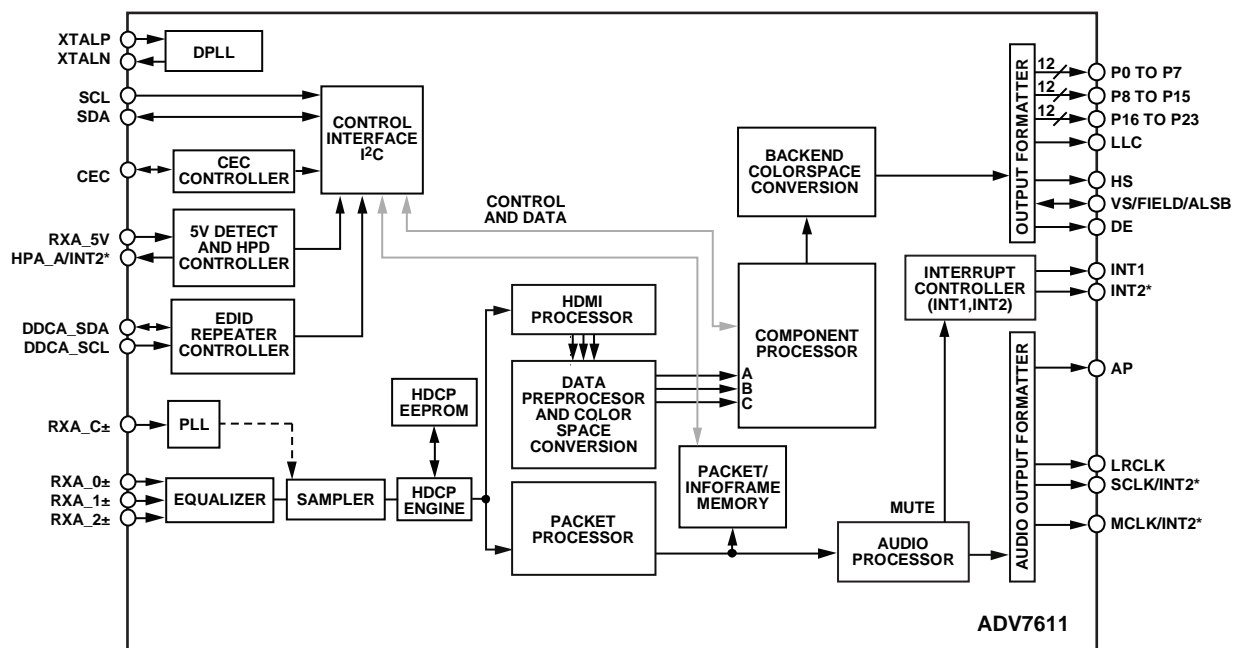
- A TDM stream from the I²S serializer (eight audio channels, time multiplexed), the maximum audio bit rate is 48 kHz
- A stream from the S/PDIF serializer (two uncompressed channels or N compressed channels, for example, AC3)
- DST stream

The HDMI port has dedicated 5 V detect and Hot Plug™ assert pins. The HDMI receiver also includes an integrated equalizer that ensures the robust operation of the interface with long cables.

The ADV7611 contains one main component processor (CP), that processes the video signals from the HDMI receiver. It provides features such as contrast, brightness and saturation adjustments, STDI detection block, free run, and synchronization alignment controls.

Fabricated in an advanced CMOS process, the ADV7611 is provided in a 10 mm × 10 mm, 64-lead surface-mount LQFP_EP, RoHS-compliant package and is specified over the -40°C to $+85^{\circ}\text{C}$ temperature range.

DETAILED FUNCTIONAL BLOCK DIAGRAM



*INT2 CAN BE ONLY OUTPUT ON ONE OF THE PINS: SCLK/INT2, MCLK/INT2, OR HPA_A/INT2.

Figure 2. Detailed Functional Block Diagram

09305-002

SPECIFICATIONS

At DVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.14 V to 3.46 V, CVDD = 1.71 V to 1.89 V, T_{MIN} to T_{MAX} = -40°C to +85°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS¹						
Input High Voltage	V _{IH}	XTALN and XTALP	1.2			V
	V _{IH}	Other digital inputs	2			V
Input Low Voltage	V _{IL}	XTALN and XTALP			0.4	V
	V _{IL}	Other digital inputs			0.8	V
Input Current	I _{IN}	RESET pin		±45	±60	µA
		Other digital inputs		±10		µA
Input Capacitance	C _{IN}				10	pF
DIGITAL INPUTS (5 V TOLERANT)^{1, 2}						
Input High Voltage	V _{IH}		2.6			V
Input Low Voltage	V _{IL}				0.8	V
Input Current	I _{IN}		-82		+82	µA
DIGITAL OUTPUTS¹						
Output High Voltage	V _{OH}		2.4			V
Output Low Voltage	V _{OL}				0.4	V
High Impedance Leakage Current	I _{LEAK}	VS/FIELD/ALSB pin		±35	±60	µA
		HPA_A/INT2 pin			±82	µA
Other			10			µA
Output Capacitance	C _{OUT}				20	pF
POWER REQUIREMENTS³						
Digital Core Power Supply	DVDD		1.71	1.8	1.89	V
Digital I/O Power Supply	DVDDIO		3.14	3.3	3.46	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Terminator Power Supply	TVDD		3.14	3.3	3.46	V
Comparator Power Supply	CVDD		1.71	1.8	1.89	V
Digital Core Supply Current	I _{DVDD}	UXGA 60 Hz at 8 bit		95.7	188.1	mA
Digital I/O Supply Current	I _{DVDDIO}	UXGA 60 Hz at 8 bit		12.9	178.5	mA
PLL Supply Current	I _{PVDD}	UXGA 60 Hz at 8 bit		30.7	36.9	mA
Terminator Supply Current	I _{TVDD}	UXGA 60 Hz at 8 bit		50.9	57.6	mA
Comparator Supply Current	I _{CVDD}	UXGA 60 Hz at 8 bit		95.8	114.4	mA
POWER-DOWN CURRENTS⁴						
Digital Core Supply Current	I _{DVDD_PD}	Power-Down Mode 1		0.2	0.5	mA
Digital I/O Supply Current	I _{DVDDIO_PD}	Power-Down Mode 1		1.3	1.7	mA
PLL Supply Current	I _{PVDD_PD}	Power-Down Mode 1		1.5	1.8	mA
Terminator Supply Current	I _{TVDD_PD}	Power-Down Mode 1		0.1	0.3	mA
Comparator Supply Current	I _{CVDD_PD}	Power-Down Mode 1		1.3	1.7	mA
Power-Up Time	t _{PWRUP}			25		ms

¹ Data guaranteed by characterization.

² The following pins are 5 V tolerant: DDCA_SCL, DDC_SDA, and RXA_5V.

³ Maximum current consumption values are recorded with maximum rated voltage supply levels, MoireX video pattern, and at maximum rated temperature.

⁴ Power-Down Mode 0 (IO map, Register 0x0C = 0x62), ring oscillator powered down (HDMI map, Register 0x48 = 0x01), and DDC pads off (HDMI map, Register 0x73 = 0x01).

DATA AND I²C TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND CRYSTAL						
Crystal Frequency, XTALP				28.63636		MHz
Crystal Frequency Stability					±50	ppm
LLC Frequency Range ¹			13.5		165	MHz
I ² C PORTS						
SCL Frequency					400	kHz
SCL Minimum Pulse Width High ²	t ₁		600			ns
SCL Minimum Pulse Width Low ²	t ₂		1.3			µs
Start Condition Hold Time ²	t ₃		600			ns
Start Condition Setup Time ²	t ₄		600			ns
SDA Setup Time ²	t ₅		100			ns
SCL and SDA Rise Time ²	t ₆				300	ns
SCL and SDA Fall Time ²	t ₇				300	ns
Stop Condition Setup Time ²	t ₈		0.6			µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark-Space Ratio ²	t ₉ :t ₁₀		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS ³						
Data Output Transition Time ^{2,4}	t ₁₁	End of valid data to negative clock edge		1.0	2.2	ns
	t ₁₂	Negative clock edge to start of valid data		0.0	0.3	ns
I ² S PORT, MASTER MODE						
SCLK Mark-Space Ratio ²	t ₁₅ :t ₁₆		45:55		55:45	% duty cycle
LRCLK Data Transition Time ²	t ₁₇	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time ²	t ₁₈	Negative SCLK edge to start of valid data			10	ns
I ² S Data Transition Time ^{5,2}	t ₁₉	End of valid data to negative SCLK edge			5	ns
I ² S Data Transition Time ^{5,2}	t ₂₀	Negative SCLK edge to start of valid data			5	ns
TDM SERIAL TIMING ⁶						
SCLK Mark-Space Ratio ²	t ₂₁ :t ₂₂		45:55		55:45	% duty cycle
LRCLK Data Transition Time ²	t ₂₃	End of valid data to negative SCLK edge			10	ns
LRCLK Data Transition Time ²	t ₂₄	Negative SCLK edge to start of valid data			10	ns
I ² S_TDM Data Transition Time ^{2,3}	t ₂₅	End of valid data to negative SCLK edge			5	ns
I ² S_TDM Data Transition Time ^{2,3}	t ₂₆	Negative SCLK edge to start of valid data			5	ns

¹ Maximum LLC frequency is limited by the clock frequency of UXGA 60 Hz at 8 bit.

² Data guaranteed by characterization.

³ With the DLL block on output clock bypassed.

⁴ DLL bypassed on clock path.

⁵ I²S is accessible via the AP pin.

⁶ I²S_TDM is accessible via the AP pin.

Timing Diagrams

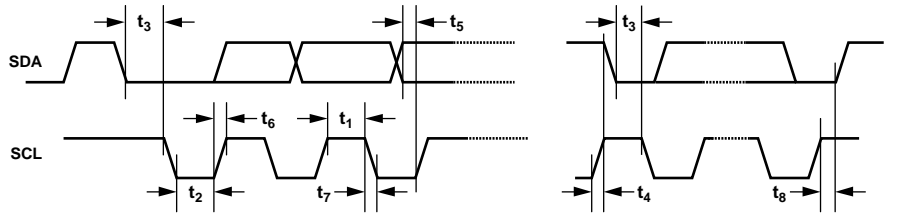


Figure 3. I²C Timing

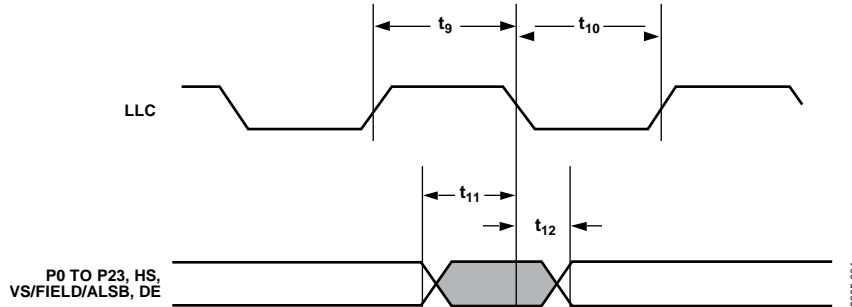
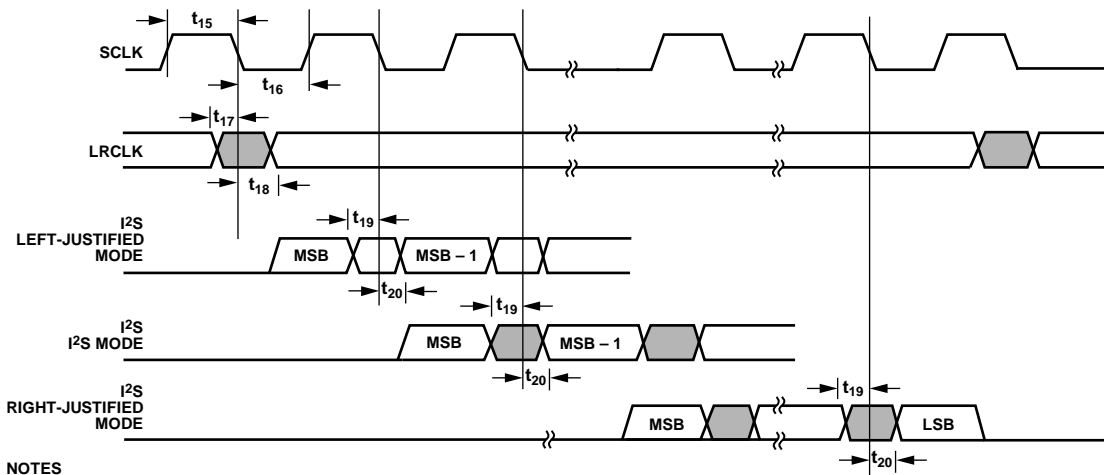


Figure 4. Pixel Port and Control SDR Output Timing



NOTES
1. I²S IS A SIGNAL ACCESSIBLE VIA THE AP PIN.

Figure 5. I²S Timing

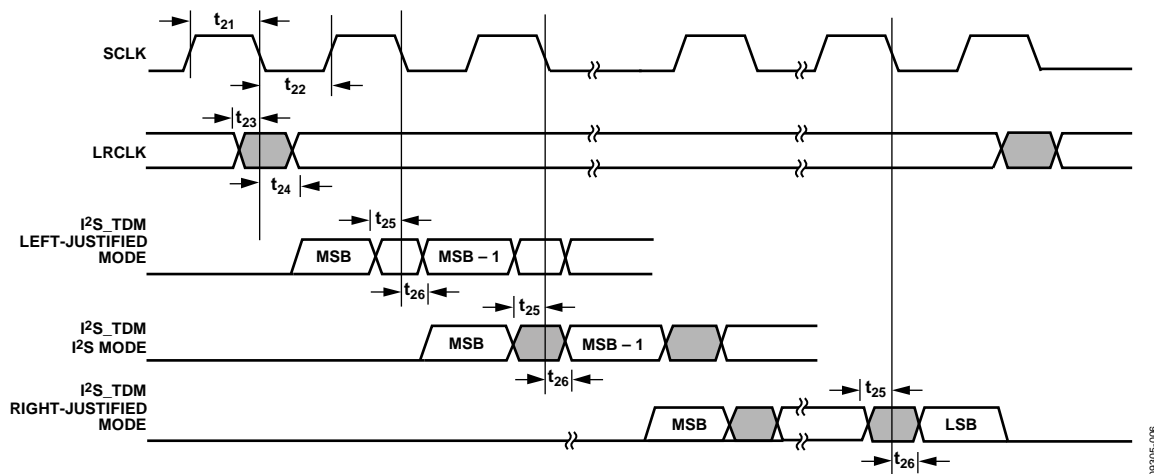


Figure 6. TDM Serial Timing

09305-006

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
CVDD to GND	2.2 V
TVDD to GND	4.0 V
Digital Inputs Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
5 V Tolerant Digital Inputs to GND ¹	5.3 V
Digital Outputs Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
XTALP, XTALN	GND – 0.3 V to PVDD + 0.3 V
SCL/SDA Data Pins to DVDDIO	DVDDIO – 0.3 V to DVDDIO + 3.6 V
Maximum Junction Temperature (T _{JMAX})	125°C
Storage Temperature Range	–60°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

¹ The following inputs are 3.3 V inputs but are 5 V tolerant: DDCA_SCL and DDCA_SDA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7611, the user is advised to turn off the unused sections of the part.

Due to the printed circuit board (PCB) metal variation, and, therefore, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature (T_{JMAX}) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_j = T_s + (\Psi_{JT} \times W_{TOTAL})$$

where:

T_s is the package surface temperature (°C).

$\Psi_{JT} = 0.4^\circ\text{C}/\text{W}$ for the 64-lead LQFP_EP.

$$W_{TOTAL} = ((PVDD \times I_{PVDD}) + (0.05 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}))$$

where 0.05 is 5% of the TVDD power that is dissipated on the part itself.

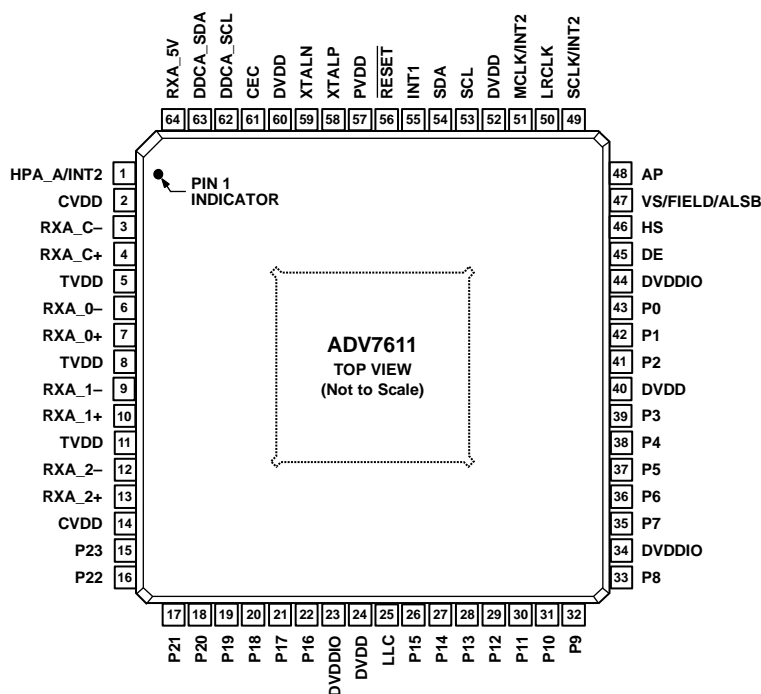
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. CONNECT EXPOSED PAD (PIN0) TO GROUND (BOTTOM).

Figure 7. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	GND	Ground	Ground.
1	HPA_A/INT2	Miscellaneous digital	A dual function pin that can be configured to output a Hot Plug assert signal (for HDMI Port A) or an Interrupt 2 signal.
2	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
3	RXA_C-	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
4	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
5	TVDD	Power	Terminator Supply Voltage (3.3 V).
6	RXA_0-	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
7	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
8	TVDD	Power	Terminator Supply Voltage (3.3 V).
9	RXA_1-	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
10	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
11	TVDD	Power	Terminator Supply Voltage (3.3 V).
12	RXA_2-	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
13	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
14	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
15	P23	Digital video output	Video Pixel Output Port.
16	P22	Digital video output	Video Pixel Output Port.
17	P21	Digital video output	Video Pixel Output Port.
18	P20	Digital video output	Video Pixel Output Port.
19	P19	Digital video output	Video Pixel Output Port.
20	P18	Digital video output	Video Pixel Output Port.
21	P17	Digital video output	Video Pixel Output Port.
22	P16	Digital video output	Video Pixel Output Port.
23	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).

ADV7611

Pin No.	Mnemonic	Type	Description
24	DVDD	Power	Digital Core Supply Voltage (1.8 V).
25	LLC	Digital video output	Line-Locked Output Clock for the Pixel Data (Range is 13.5 MHz to 162.5 MHz).
26	P15	Digital video output	Video Pixel Output Port.
27	P14	Digital video output	Video Pixel Output Port.
28	P13	Digital video output	Video Pixel Output Port.
29	P12	Digital video output	Video Pixel Output Port.
30	P11	Digital video output	Video Pixel Output Port.
31	P10	Digital video output	Video Pixel Output Port.
32	P9	Digital video output	Video Pixel Output Port.
33	P8	Digital video output	Video Pixel Output Port.
34	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
35	P7	Digital video output	Video Pixel Output Port.
36	P6	Digital video output	Video Pixel Output Port.
37	P5	Digital video output	Video Pixel Output Port.
38	P4	Digital video output	Video Pixel Output Port.
39	P3	Digital video output	Video Pixel Output Port.
40	DVDD	Power	Digital Core Supply Voltage (1.8 V).
41	P2	Digital video output	Video Pixel Output Port.
42	P1	Digital video output	Video Pixel Output Port.
43	P0	Digital video output	Video Pixel Output Port.
44	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
45	DE	Miscellaneous digital	DE (data enable) is a signal that indicates active pixel data.
46	HS	Digital video output	HS is a horizontal synchronization output signal.
47	VS/FIELD/ALSB	Digital input/output	VS is a vertical synchronization output signal. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin. The ALSB allows selection of the I ² C address.
48	AP	Miscellaneous digital	Audio Output Pin. Pin can be configured to output S/PDIF digital audio output (S/PDIF) or time-division-multiplexed I ² S.
49	SCLK/INT2	Miscellaneous digital	A dual function pin that can be configured to output an audio serial clock or an Interrupt 2 signal.
50	LRCLK	Miscellaneous digital	Audio Left/Right Clock.
51	MCLK/INT2	Miscellaneous digital	A dual function pin that can be configured to output an audio master clock or an Interrupt 2 signal.
52	DVDD	Power	Digital Core Supply Voltage (1.8 V).
53	SCL	Miscellaneous digital	I ² C Port Serial Clock Input. SCL is the clock line for the control port.
54	SDA	Miscellaneous digital	I ² C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
55	INT1	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user configuration.
56	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7611 circuitry.
57	PVDD	Power	PLL Supply Voltage (1.8 V).
58	XTALP	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7611.
59	XTALN	Miscellaneous analog	Crystal Input. Input pin for 28.63636 MHz crystal.
60	DVDD	Power	Digital Core Supply Voltage (1.8 V).
61	CEC	Digital input/output	Consumer Electronic Control Channel.
62	DDCA_SCL	HDMI input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
63	DDCA_SDA	HDMI input	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant.
64	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The recommended power-up sequence of the ADV7611 is to power up the 3.3 V supplies first, followed by the 1.8 V supplies. Reset should be held low while the supplies are powered up.

Alternatively, the ADV7611 may be powered up by asserting all supplies simultaneously. In this case, care must be taken while the supplies are being established to ensure that a lower rated supply does not go above a higher rated supply level.

POWER-DOWN SEQUENCE

The ADV7611 supplies may be deasserted simultaneously as long as a higher rated supply does not go below a lower rated supply.

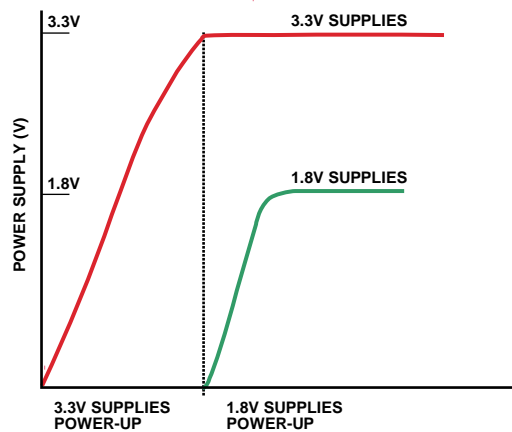


Figure 8. Recommended Power-Up Sequence

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The receiver supports all mandatory and many optional 3D formats. It supports HDTV formats up to UXGA at 8 bit.

The HDMI-compatible receiver on the ADV7611 incorporates programmable equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance.

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the ADV7611 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 protocol.

The ADV7611 has a synchronization regeneration block used to regenerate the DE based on the measurement of the video format being displayed and to filter the horizontal and vertical synchronization signals to prevent glitches. The HDMI receiver also supports TERC4 error detection, used for detection of corrupted HDMI packets following a cable disconnect.

The HDMI receiver contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, the audio signal can be ramped to prevent audio clicks or pops. Audio output can be formatted to LPCM and IEC 61937.

The HDMI receiver features include:

- 162.5 MHz (UXGA at 8 bit) maximum TMDS clock frequency
- 3D format support defined in HDMI 1.4a specification
- Integrated equalizer for cable lengths up to 30 meters
- HDCP 1.4
- Internal HDCP keys
- PCM audio packet support
- TDM I²S audio packet support
- Repeater support
- Internal EDID RAM
- Hot Plug assert output pin for an HDMI port
- CEC controller

COMPONENT PROCESSOR

The ADV7611 has an any-to-any 3 × 3 CSC matrix. The CSC block is placed at the back of the CP section. CSC enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

CP features include:

- 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and other formats
- Manual adjustments including gain (contrast) and offset (brightness), hue, and saturation
- Free run output mode that provides stable timing when no video input is present
- 162.5 MHz processing rate
- Contrast, brightness, hue, and saturation controls
- Standard identification enabled by STDI block
- RGB that can be color space converted to YCrCb and decimated to a 4:2:2 format for video-centric back end IC interfacing
- DE output signal supplied for direct connection to an HDMI/DVI transmitter

OTHER FEATURES

The ADV7611 has HS, VS, FIELD, and DE output signals with programmable position, polarity, and width.

The ADV7611 has programmable interrupt request output pins, including INT1 and INT2 (INT2 is accessible only via one of following pins: MCLK/INT2, SCLK/INT2, or HPA_A/INT2). It also features a low power-down mode. The I²C address of the main map is 0x98 after reset. This can be changed after reset to 0x9A if pullup is attached to VS/FIELD/ALSB pin and I²C command SAMPLE_ALSB is issued. Refer to the Register Access and Serial Ports Description section in the [UG-180](#).

The ADV7611 is provided in a 10 mm × 10 mm, RoHS-compliant LQFP_EP package, and is specified over the -40°C to +85°C temperature range.

For more detailed product information about the ADV7611, contact your local Analog Devices, Inc., sales office.

TIME-DIVISION MULTIPLEXED (TDM) MODE

The ADV7611 can output TDM serial data mode on the the AP pin. The configuration is shown in Figure 9 where the eight I²S channels are packed into one TDM stream.

These slots can be extracted using programmable logic and output to the commonly used I²S format.

It should be noted that due to the high SCLK frequency, TDM mode is available only for a maximum audio bit rate of 48 kHz.

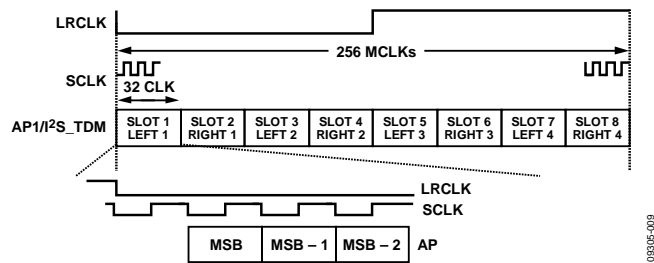


Figure 9. TDM (8-Channel I²S Mode)

09305-009

PIXEL INPUT/OUTPUT FORMATTING

The output section of the ADV7611 is highly flexible. The pixel output bus can support up to 24-bit 4:4:4 YCrCb. The pixel data supports both single and double data rates modes. In SDR mode, a 16-/24-bit 4:2:2 or 24-bit 4:4:4 output is possible. In DDR mode, the pixel output port can be configured in an 8-/12-bit 4:2:2 YCrCb or 24-bit 4:4:4 RGB.

Bus rotation is supported. Table 5 and Table 6 outline the different output formats that are supported. All output modes are controlled via I²C.

PIXEL DATA OUTPUT MODES FEATURES

The output pixel port features include:

- 8-/12-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD output signals
- 16-/24-bit YCrCb with embedded time codes and/or HS and VS/FIELD pin timing
- 24-bit YCrCb/RGB with embedded time codes and/or HS and VS/FIELD pin timing
- DDR 8-/12-bit 4:2:2 YCrCb
- DDR 24-bit 4:4:4 RGB

Table 5. SDR 4:2:2 and 4:4:4 Output Modes

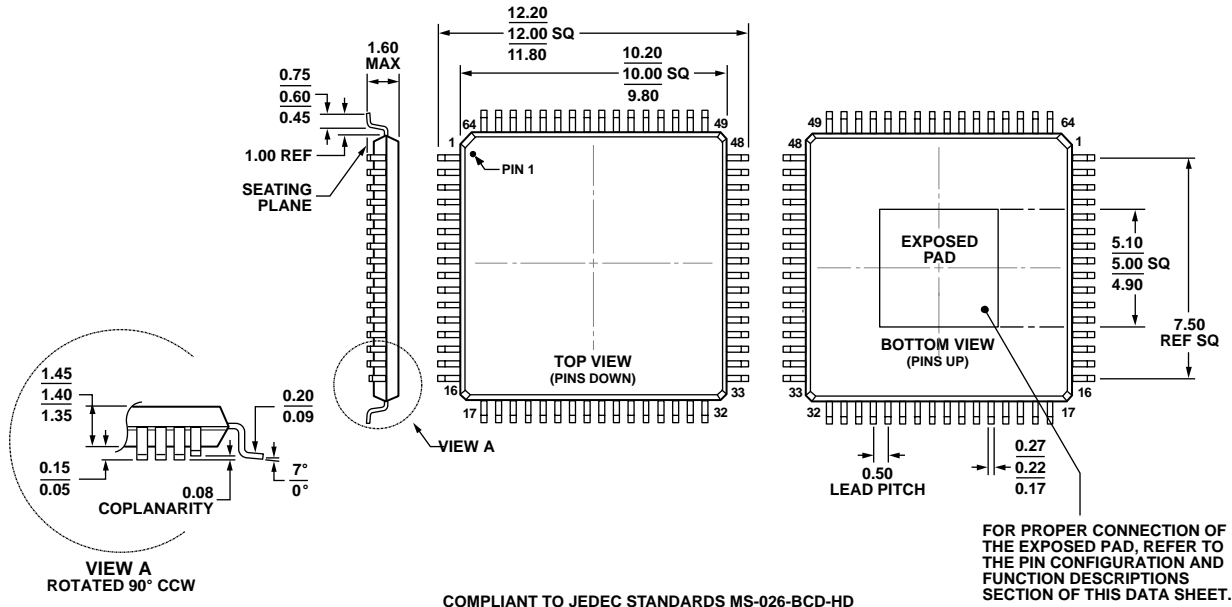
OP_FORMAT_SEL[7:0]	SDR 4:2:2				SDR 4:4:4
	0x0	0x0A	0x80	0x8A	0x40
Pixel Output	8-Bit SDR ITU-R BT.656 Mode 0	12-Bit SDR ITU-R BT.656 Mode 2	16-Bit SDR ITU-R BT.656 4:2:2 Mode 0	24-Bit SDR ITU-R BT.656 4:2:2 Mode 2	24-Bit SDR 4:4:4 Mode 0
P23	High-Z	Y3, Cb3, Cr3	High-Z	Y3	R7
P22	High-Z	Y2, Cb2, Cr2	High-Z	Y2	R6
P21	High-Z	Y1, Cb1, Cr1	High-Z	Y1	R5
P20	High-Z	Y0, Cb0, Cr0	High-Z	Y0	R4
P19	High-Z	High-Z	High-Z	Cb3, Cr3	R3
P18	High-Z	High-Z	High-Z	Cb2, Cr2	R2
P17	High-Z	High-Z	High-Z	Cb1, Cr1	R1
P16	High-Z	High-Z	High-Z	Cb0, Cr0	R0
P15	Y7, Cb7, Cr7	Y11, Cb11, Cr11	Y7	Y11	G7
P14	Y6, Cb6, Cr6	Y10, Cb10, Cr10	Y6	Y10	G6
P13	Y5, Cb5, Cr5	Y9, Cb9, Cr9	Y5	Y9	G5
P12	Y4, Cb4, Cr4	Y8, Cb8, Cr8	Y4	Y8	G4
P11	Y3, Cb3, Cr3	Y7, Cb7, Cr7	Y3	Y7	G3
P10	Y2, Cb2, Cr2	Y6, Cb6, Cr6	Y2	Y6	G2
P9	Y1, Cb1, Cr1	Y5, Cb5, Cr5	Y1	Y5	G1
P8	Y0, Cb0, Cr0	Y4, Cb4, Cr4	Y0	Y4	G0
P7	High-Z	High-Z	Cb7, Cr7	Cb11, Cr11	B7
P6	High-Z	High-Z	Cb6, Cr6	Cb10, Cr10	B6
P5	High-Z	High-Z	Cb5, Cr5	Cb9, Cr9	B5
P4	High-Z	High-Z	Cb4, Cr4	Cb8, Cr8	B4
P3	High-Z	High-Z	Cb3, Cr3	Cb7, Cr7	B3
P2	High-Z	High-Z	Cb2, Cr2	Cb6, Cr6	B2
P1	High-Z	High-Z	Cb1, Cr1	Cb5, Cr5	B1
P0	High-Z	High-Z	Cb0, Cr0	Cb4, Cr4	B0

Table 6. DDR 4:2:2 and 4:4:4 Output Modes

OP_FORMAT_SEL[7:0]	DDR 4:2:2 Mode (Clock/2)		DDR 4:2:2 Mode (Clock/2)		DDR 4:4:4 Mode (Clock/2) ^{1,2}	
	0x20		0x2A		0x60	
Pixel Output	8-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 0		12-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 2		24-Bit DDR RGB (Clock/2 Output)	
	Clock Rise	Clock Fall	Clock Rise	Clock Fall	Clock Rise	Clock Fall
P23	High-Z	High-Z	Cb3, Cr3	Y3	R7-0	R7-1
P22	High-Z	High-Z	Cb2, Cr2	Y2	R6-0	R6-1
P21	High-Z	High-Z	Cb1, Cr1	Y1	R5-0	R5-1
P20	High-Z	High-Z	Cb0, Cr0	Y0	R4-0	R4-1
P19	High-Z	High-Z	High-Z	High-Z	R3-0	R3-1
P18	High-Z	High-Z	High-Z	High-Z	R2-0	R2-1
P17	High-Z	High-Z	High-Z	High-Z	R1-0	R1-1
P16	High-Z	High-Z	High-Z	High-Z	R0-0	R0-1
P15	Cb7, Cr7	Y7	Cb11, Cr11	Y11	G7-0	G7-1
P14	Cb6, Cr6	Y6	Cb12, Cr12	Y12	G6-0	G6-1
P13	Cb5, Cr5	Y5	Cb9, Cr9	Y9	G5-0	G5-1
P12	Cb4, Cr4	Y4	Cb8, Cr8	Y8	G4-0	G4-1
P11	Cb3, Cr3	Y3	Cb7, Cr7	Y7	G3-0	G3-1
P10	Cb2, Cr2	Y2	Cb6, Cr6	Y6	G2-0	G2-1
P9	Cb1, Cr1	Y1	Cb5, Cr5	Y5	G1-0	G1-1
P8	Cb0, Cr0	Y0	Cb4, Cr4	Y4	G0-0	G0-1
P7	High-Z	High-Z	High-Z	High-Z	B7-0	B7-1
P6	High-Z	High-Z	High-Z	High-Z	B6-0	B6-1
P5	High-Z	High-Z	High-Z	High-Z	B5-0	B5-1
P4	High-Z	High-Z	High-Z	High-Z	B4-0	B4-1
P3	High-Z	High-Z	High-Z	High-Z	B3-0	B3-1
P2	High-Z	High-Z	High-Z	High-Z	B2-0	B2-1
P1	High-Z	High-Z	High-Z	High-Z	B1-0	B1-1
P0	High-Z	High-Z	High-Z	High-Z	B0-0	B0-1

¹-0 = even samples.²-1 = odd samples.

OUTLINE DIMENSIONS



ORDERING GUIDE

Model ¹	Notes	Temperature Range	Package Description	Package Option
ADV7611BSWZ		-40°C to +85°C	64-Lead LQFP_EP	SW-64-2
ADV7611BSWZ-P	²	-40°C to +85°C	64-Lead LQFP_EP	SW-64-2
ADV7611BSWZ-P-RL	³	-40°C to +85°C	64-Lead LQFP_EP	SW-64-2

¹ Z = RoHS Compliant Part.

² Non-HDCP version.

³ 13" Tape and Reel.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors). HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries.