Precision Analog Microcontroller
12-Bit ADCs and DACs, ARM7TDMI® Core

Silicon Anomaly List — ADuC7019/ADuC702x

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7019/ADuC702x MicroConverter®. The anomalies listed apply to all ADuC7019/702x packaged material branded as follows:

First Line ADuC7019 or ADuC702x (where: x = 0 to 7)
Third Line I30 (revision identifier)

Analog Devices, Inc. is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7019/ADuC702x FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		All silicon branded I30	Release	Rev. B	5

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

ANOMALIES

ADuC7019/ADuC702x Functionality Issues

1. ADC Conversion Start Mode [er017]:

Background: ADCCON [2:0] allow the user to select one of six ADC conversion start modes of operation, namely:

- External pin (P2.0) triggered ADC conversion
- Timer1 overflow
- Timer0 overflow
- Single software conversion
- Continuous software conversion
- PLA triggered ADC conversion

Issue: The active-low, external pin (P2.0) triggered conversion is always active, even if it is not selected via ADCCON [2:0]. This is the case if the function of P2.0 is configured as a $\overline{\text{CONV}}_{\text{START}}$ input or if P2.0 is configured as any other function, for example, SOUT, PLAO[5], or GPIO. This means that if a falling edge is seen on P2.0, a single ADC conversion is triggered if ADCCON [7] is enabled. If an ADC conversion cycle is already in progress, this conversion stops and a new ADC conversion cycle begins in response to a falling edge on P2.0.

Workaround: Pending.

Related Issues: ADCCON [7], the ADC enable conversion mode bit, is fully functional, allowing the user to disable any of the active ADC conversion modes except continuous conversion (see the ADuC7019/7020/7021/7022/7024/7025/7026/7027 data sheet).

2. MMR Default Values [er018]:

Background: The on-chip factory firmware allows downloading to the ADuC7019/ADuC702x parts through the UART or I²C® interfaces. After kernel execution, in normal mode or after downloading and jumping to user code, the MMR default values should be as described in the datasheet (see the ADuC7019/7020/7021/7022/7024/7025/7026/7027 data sheet).

Issue: When downloading occurs via one of these interfaces and a software RUN command is sent (as described in AN-724 or AN-806), the following MMRs are modified by the factory firmware:

UART loader (standard parts)	I²C loader (I models)
COMTX	I2C0SRX
COMRX	I2C0STX
COMDIV0	I2C0CFG
COMCON0	I2C0ID0/1/2/3
COMDIV2	I2C0STA
GP1CON	GP1CON
FEEADR	FEEADR

Workaround: GP1CON needs to be configured to use P1.0 and P1.1 as GPIO.
COMDIV2 must be cleared to use the UART without the fractional divider on standard parts.

Related Issues: No MMRs are modified as a result of running user code from a power cycle, toggling of the reset pin, or a software reset.

3. On-Chip Loader's Protection Command [er019]:

Background: The on-chip factory firmware residing in 2 kB of Flash/EE memory allows the downloading of user code to user space in Flash/EE via a serial port (either UART or I²C, depending on the model). After downloading code, it also allows protection of the Flash/EE user space through the use of a 32-bit key.

Issue: The protection key is a 32-bit value that should be entered in FEEADR and FEEDAT during the protection sequence. The loader ignores the 16 MSB of the key and writes only the 16 LSB in both FEEADR and FEEDAT.

Workaround: None.

Related Issues: This does not affect writing keys via JTAG or user code.

4. On-Chip Loader's Write/Verify Commands [er020]:

Background:	The on-chip factory firmware residing in 2 kB of Flash/EE memory allows the downloading of user code from Intel HEX files to user space in Flash/EE memory via a serial port (either UART or I^2C, depending on the model). After downloading, it also allows verification that the Flash/EE memory has been programmed properly.
Issue:	Both the write command and verify command, as described in AN-724 and AN-806, cause issues with odd addresses: • If the address of the first byte of the data packet to be programmed is odd, the data at the previous address becomes corrupted. • If the address of the last byte of the data packet to be programmed is even, this byte is not written into Flash/EE memory.
Workaround:	ARMWSD Version 6.8 and higher ensures that the data starts and terminates on half word boundaries. Dummy bytes (0xFF) are added to data packets that do not start/stop on half word boundaries. Users employing their own software for downloading should also take this precaution.
Related Issues:	None.

5. I^2C Slave Not Releasing the Bus [er021]:

Background:	During a read from the master to the slave, if the slave's FIFO is empty, the slave generates a NACK in response to the master's request. Then it releases the bus, allowing the master to generate a STOP condition.
Issue:	Following generation of a no acknowledge, the ADuC7019/ADuC702x may not release the bus due to the generation of a FIFO transmit empty interrupt.
Workaround:	Following the generation of a transmit FIFO empty interrupt, the bus can be released by any of the following: • Placing valid data in the transmit FIFO • Placing dummy data in the transmit FIFO, followed by a transmit FIFO flush • Resetting the slave interface by disabling/enabling the slave
Related Issues:	None.

SECTION 1. ADuC7019/ADuC702X FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	External reference	Fixed
er002	ADC wrap around	Fixed
er003	Flash/EE controller	Fixed
er004	Code execution, 1 kB boundary issue	Fixed
er005	Clocking system	Fixed
er006	Wake-up timer operation	Fixed
er007	I^2C transmit FIFO flush operation	Fixed
er008	Use of I^2C in master mode	Fixed
er009	Block interconnection in PLA peripheral	Fixed
er010	Baud rate generation	Fixed
er011	Temperature sensor operation	Fixed
er012	PLA clock source pins	Fixed
er013	ADC power-up time	Feature
er014	PWM sync interrupt	Fixed
er015	Watchdog timer operation	Fixed
er016	External memory bus operation	Fixed
er017	*ADC conversion start mode*	*Open*
er018	*MMR default values*	*Open*
er019	*On-chip loader's protection command*	*Open*
er020	*On-chip loader's write/verify commands*	*Open*
er021	*I^2C slave not releasing the bus*	*Open*

SECTION 2. ADuC7019/ADuC702x PERFORMANCE RELATED ISSUES

Reference Number	Description	Status
pr001	ADC linearity	Fixed
pr002	DAC gain error	Fixed
pr003	Execution speed	Fixed
pr004	Flash retention specification	Fixed

SECTION 3. ADuC7019/ADuC702x SILICON FUTURE ENHANCEMENTS

Reference Number	Description	Status
fe001	I^2C address matching	Fixed
fe002	I^2C start and stop condition identification	Fixed
fe003	External clock input pin	Fixed

S05883–0–3/06(B)