8-Bit, 100 MSPS+ TxDAC® D/A Converter

AD9708*

FEATURES
Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
8-Bit Resolution
Linearity: 1/4 LSB DNL
1/4 LSB INL
Differential Current Outputs
SINAD @ 5 MHz Output: 50 dB
Power Dissipation: 175 mW @ 5 V to 45 mW @ 3 V
Power-Down Mode: 20 mW @ 5 V
On-Chip 1.20 V Reference
Single +5 V or +3 V Supply Operation
Packages: 28-Lead SOIC and 28-Lead TSSOP
Edge-Triggered Latches
Fast Settling: 35 ns Full-Scale Settling to 0.1%

APPLICATIONS
Communications
Signal Reconstruction
Instrumentation

PRODUCT DESCRIPTION

The AD9708 is the 8-bit resolution member of the TxDAC series of high performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, which consists of pin compatible 8-, 10-, 12-, and 14-bit DACs, was specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. The AD9708 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9708's flexible single-supply operating range of +2.7 V to +5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to 45 mW, without a significant degradation in performance, by lowering the full-scale current output. In addition, a power-down mode reduces the standby power dissipation to approximately 20 mW.

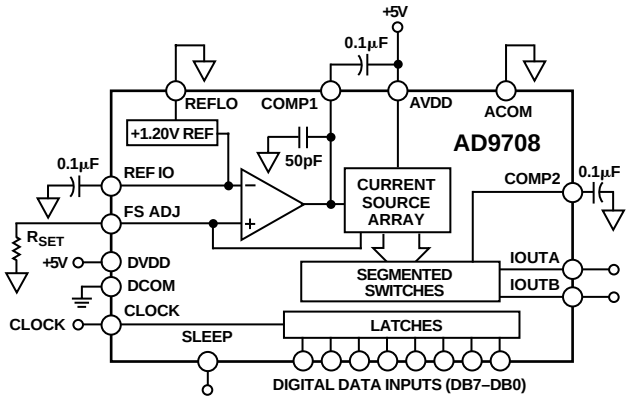
The AD9708 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3 V and +5 V CMOS logic families.

The AD9708 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance.

TxDAC is a registered trademark of Analog Devices, Inc.
*Patent pending.

REV. B

FUNCTIONAL BLOCK DIAGRAM



Differential current outputs are provided to support single-ended or differential applications. The current outputs may be directly tied to an output resistor to provide two complementary, single-ended voltage outputs. The output voltage compliance range is 1.25 V.

The AD9708 contains a 1.2 V on-chip reference and reference control amplifier, which allows the full-scale output current to be simply set by a single resistor. The AD9708 can be driven by a variety of external reference voltages. The AD9708's full-scale current can be adjusted over a 2 mA to 20 mA range without any degradation in dynamic performance. Thus, the AD9708 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9708 is available in 28-lead SOIC and 28-lead TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9708 is a member of the TxDAC product family, which provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost.
2. Manufactured on a CMOS process, the AD9708 uses a proprietary switching technique that enhances dynamic performance well beyond 8- and 10-bit video DACs.
3. On-chip, edge-triggered input CMOS latches readily interface to +3 V and +5 V CMOS logic families. The AD9708 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of +2.7 V to +5.5 V and a wide full-scale current adjustment span of 2 mA to 20 mA allows the AD9708 to operate at reduced power levels (i.e., 45 mW) without any degradation in dynamic performance.
5. A temperature compensated, 1.20 V bandgap reference is included on-chip providing a complete DAC solution. An external reference may be used.
6. The current output(s) of the AD9708 can easily be configured for various single-ended or differential applications.

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AD9708–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	8			Bits
MONOTONICITY	GUARANTEED OVER SPECIFIED TEMPERATURE RANGE			
DC ACCURACY[1]				
Integral Linearity Error (INL)	–1/2	±1/4	+1/2	LSB
Differential Nonlinearity (DNL)	–1/2	±1/4	+1/2	LSB
ANALOG OUTPUT				
Offset Error	–0.025		+0.025	% of FSR
Gain Error (Without Internal Reference)	–10	±2	+10	% of FSR
Gain Error (With Internal Reference)	–10	±1	+10	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	–1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.08	1.20	1.32	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth (w/o C_{COMP1})[4]		1.4		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD[5]	2.7	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})		25	30	mA
Digital Supply Current (I_{DVDD})[6]		3	6	mA
Supply Current Sleep Mode (I_{AVDD})			8.5	mA
Power Dissipation[6] (5 V, I_{OUTFS} = 20 mA)		140	175	mW
Power Dissipation[7] (5 V, I_{OUTFS} = 20 mA)		190		mW
Power Dissipation[7] (3 V, I_{OUTFS} = 2 mA)		45		mW
Power Supply Rejection Ratio—AVDD	–0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio—DVDD	–0.025		+0.025	% of FSR/V
OPERATING RANGE	–40		+85	°C

NOTES
[1]Measured at IOUTA, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.
[3]Use an external buffer amplifier to drive any external load.
[4]Reference bandwidth is a function of external cap at COMP1 pin.
[5]For operation below 3 V, it is recommended that the output current be reduced to 12 mA or less to maintain optimum performance.
[6]Measured at f_{CLOCK} = 50 MSPS and f_{OUT} = 1.0 MHz.
[7]Measured as unbuffered voltage output into 50 Ω R_{LOAD} at IOUTA and IOUTB, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, Single-Ended Output, IOUTA, 50 Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	100	125		MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/$\sqrt{Hz}$
Output Noise (I_{OUTFS} = 2 mA)		30		pA/$\sqrt{Hz}$
AC LINEARITY TO NYQUIST				
Signal-to-Noise and Distortion Ratio				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		50		dB
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		50		dB
f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		48		dB
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		50		dB
f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		45		dB
Total Harmonic Distortion				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		–67		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz		–67	–62	dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		–59		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		–64		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		–48		dBc
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		68		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 1.00 MHz	62	68		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 12.51 MHz		63		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 5.01 MHz		67		dBc
f_{CLOCK} = 100 MSPS; f_{OUT} = 25.01 MHz		50		dBc

NOTES
[1]Measured single ended into 50 Ω load.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	3.5			ns

Specifications subject to change without notice.

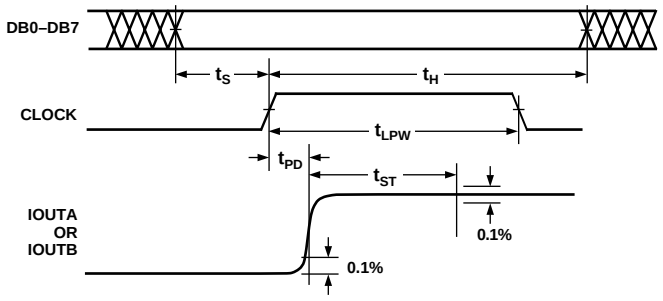


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	ACOM	–0.3	+6.5	V
DVDD	DCOM	–0.3	+6.5	V
ACOM	DCOM	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLOCK, SLEEP	DCOM	–0.3	DVDD + 0.3	V
Digital Inputs	DCOM	–0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	–1.0	AVDD + 0.3	V
COMP1, COMP2	ACOM	–0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	–0.3	AVDD + 0.3	V
REFLO	ACOM	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead 300 mil SOIC

θ_{JA} = 71.4°C/W

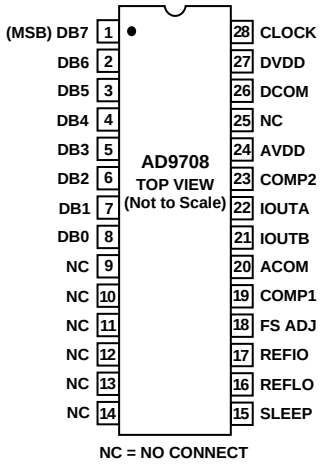
θ_{JC} = 23°C/W

28-Lead TSSOP

θ_{JA} = 97.9°C/W

θ_{JC} = 14.0°C/W

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DB7	Most Significant Data Bit (MSB).
2–7	DB6–DB1	Data Bits 1–6.
8	DB0	Least Significant Data Bit (LSB).
9–14, 25	NC	No Internal Connection.
15	SLEEP	Power-Down Control Input. Active High. Contains active pull-down circuit, thus may be left unterminated if not used.
16	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., Tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., Tie REFLO to ACOM). Requires 0.1 µF capacitor to ACOM when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust.
19	COMP1	Bandwidth/Noise Reduction Node. Add 0.1 µF to AVDD for optimum performance.
20	ACOM	Analog Common.
21	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1 µF capacitor.
24	AVDD	Analog Supply Voltage (+2.7 V to +5.5 V).
26	DCOM	Digital Common.
27	DVDD	Digital Supply Voltage (+2.7 V to +5.5 V).
28	CLOCK	Clock Input. Data latched on positive edge of clock.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options*
AD9708AR	–40°C to +85°C	28-Lead 300 Mil SOIC	R-28
AD9708ARU	–40°C to +85°C	28-Lead TSSOP	RU-28
AD9708-EB	Evaluation Board		

*R = Small Outline IC; RU = Thin Small Outline IC.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9708 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.