

## Matched N-Channel Pairs

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	$g_{fs}$ Min (mS)	$I_G$ Typ (pA)	$ V_{GS1} - V_{GS2} $ Typ (mV)
U430	-1 to -4	-25	10	-15	25
U431	-2 to -6	-25	10	-15	25

### FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 15 pA
- Low Noise
- High CMRR: 75 dB

### BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals

### APPLICATIONS

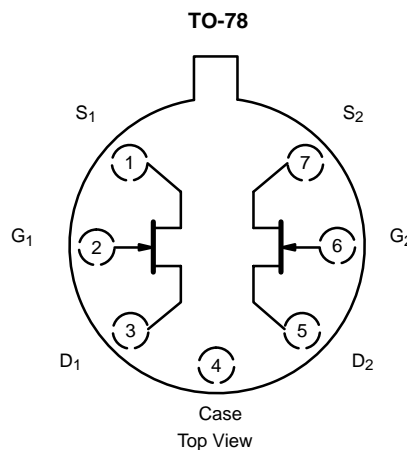
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

### DESCRIPTION

The U430/431 are matched JFET pairs assembled in a TO-78 package. These devices offer good power gain even at frequencies beyond 250 MHz.

The TO-78 package is available with full military processing (see Military Information).

For similar products, see the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.



### ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage ..... -25 V  
 Gate Current ..... 10 mA  
 Lead Temperature ( $1/16$ " from case for 10 sec.) ..... 300 °C  
 Storage Temperature ..... -65 to 200 °C  
 Operating Junction Temperature ..... -55 to 150 °C

Power Dissipation : Per Side<sup>a</sup> ..... 300 mW  
 Total<sup>b</sup> ..... 500 mW

Notes  
 a. Derate 2.4 mW/°C above 25 °C  
 b. Derate 4 mW/°C above 25 °C

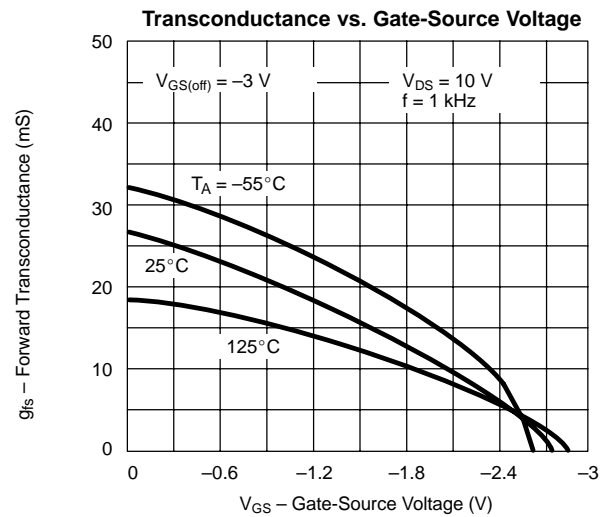
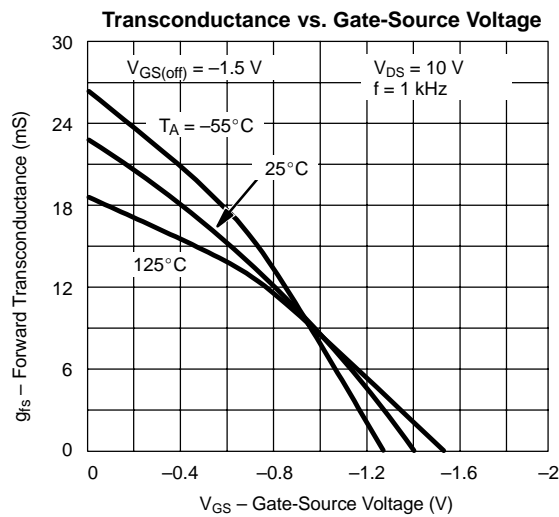
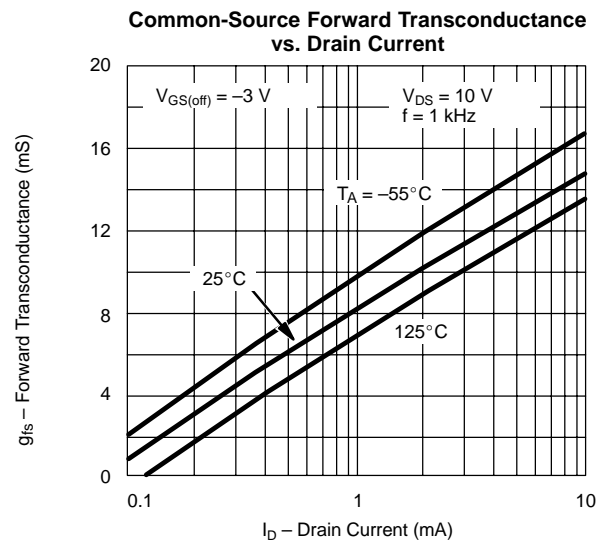
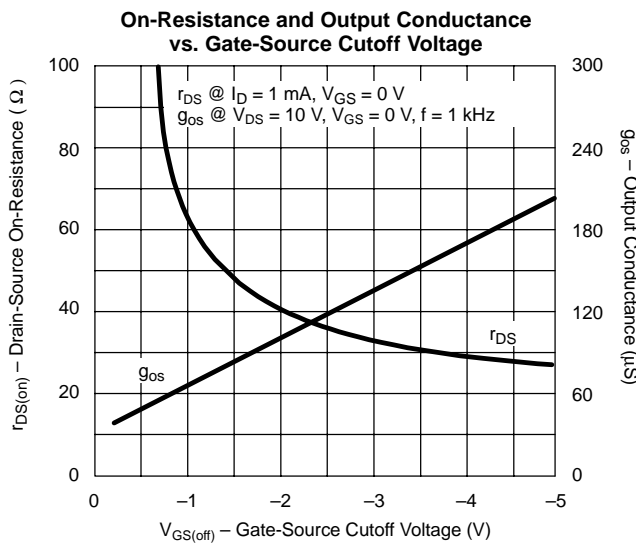
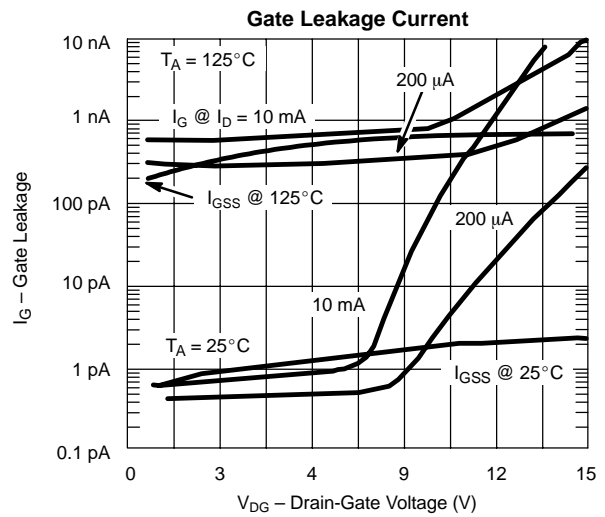
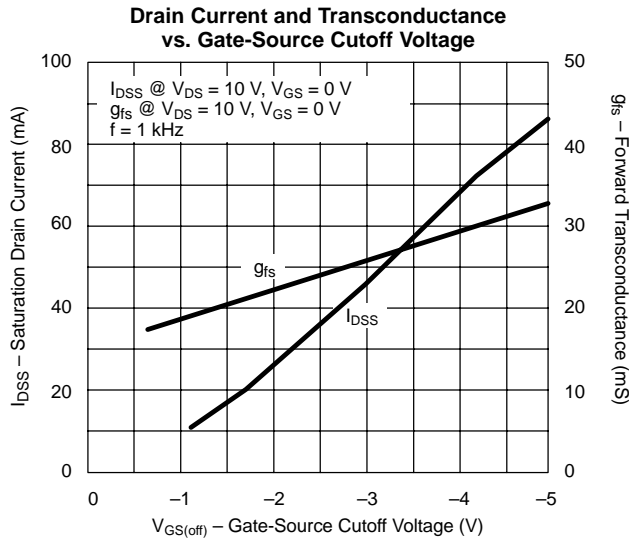
SPECIFICATIONS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Typ <sup>b</sup>	Limits				Unit
				U430		U431		
				Min	Max	Min	Max	
<b>Static</b>								
Gate-Source Breakdown Voltage	V <sub>(BR)GSS</sub>	I <sub>G</sub> = -1 μA, V <sub>DS</sub> = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA		-1	-4	-2	-6	
Saturation Drain Current <sup>d</sup>	I <sub>DSS</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V		12	30	24	60	mA
Gate Reverse Current	I <sub>GSS</sub>	V <sub>GS</sub> = -15 V, V <sub>DS</sub> = 0 V			-150		-150	pA
			T <sub>A</sub> = 150 °C	-10			-150	nA
Gate Operating Current	I <sub>G</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA						pA
			T <sub>A</sub> = 150 °C	-10				nA
Gate-Source Forward Voltage	V <sub>GS(F)</sub>	I <sub>G</sub> = 10 mA, V <sub>DS</sub> = 0 V	0.8		1		1	V
<b>Dynamic</b>								
Common-Source Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA, f = 1 kHz	15	10		10		mS
Common-Source Output Conductance <sup>b</sup>	g <sub>os</sub>		100		250		250	μS
Common-Source Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = -10 V, V <sub>DS</sub> = 0 V, f = 1 MHz	4.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C <sub>rss</sub>		2		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA f = 100 Hz	6					nV/ √Hz
<b>High Frequency</b>								
Common-Source Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA f = 100 MHz	14					mS
Common-Source Output Conductance	g <sub>os</sub>		0.13					
Power-Match Source Admittance	g <sub>ig</sub>		12					
<b>Matching</b>								
Differential Gate-Source Voltage	V <sub>GS1</sub> - V <sub>GS2</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 10 mA	25					mV
Saturation Drain Current Ratio <sup>c</sup>	$\frac{I_{DSS1}}{I_{DSS2}}$	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V	0.95	0.9	1	0.9	1	
Transconductance Ratio <sup>c</sup>	$\frac{g_{fs1}}{g_{fs2}}$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 mA, f = 1 kHz	0.95	0.9	1	0.9	1	
Gate-Source Cutoff Voltage Ratio <sup>c</sup>	$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 nA	0.95	0.9	1	0.9	1	
Differential Gate Current	I <sub>G1</sub> - I <sub>G2</sub>	V <sub>DG</sub> = 10 V, I <sub>D</sub> = 5 mA	-2					pA
Common Mode Rejection Ratio	CMRR	V <sub>DG</sub> = 5 to 10 V, I <sub>D</sub> = 10 mA	75					dB

Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
- c. Assumes smaller value in the numerator.

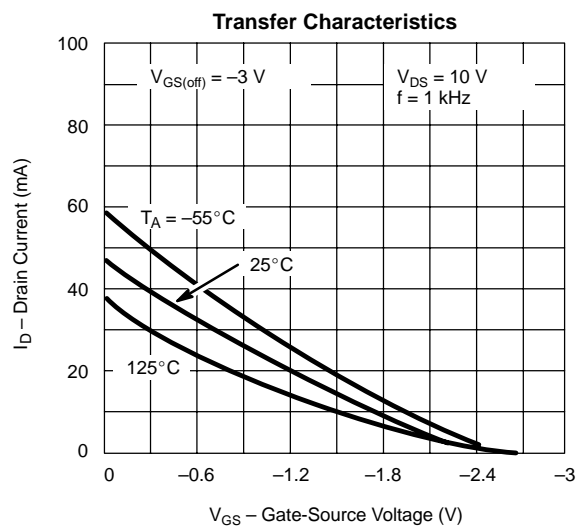
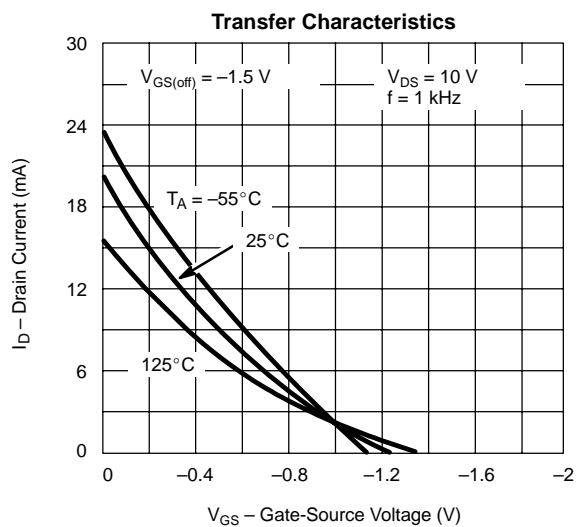
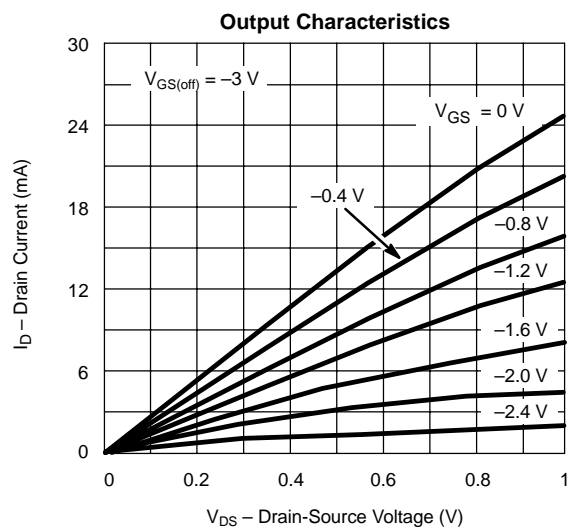
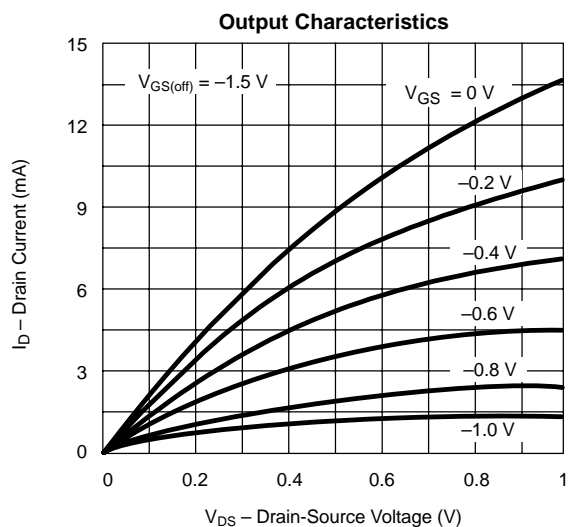
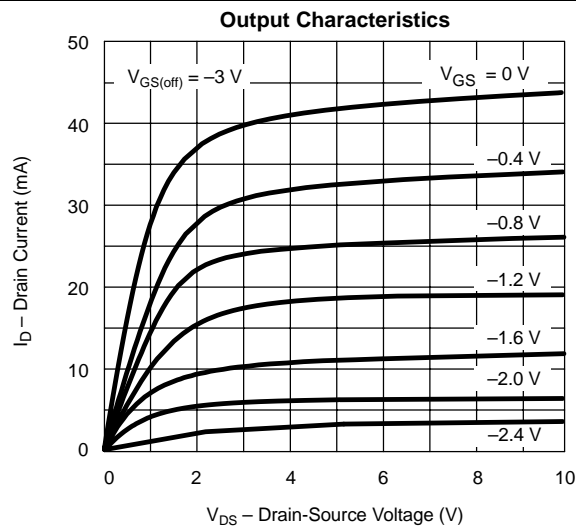
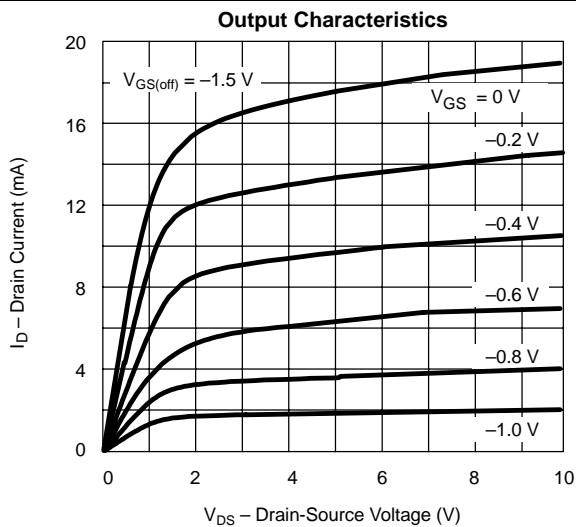
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**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

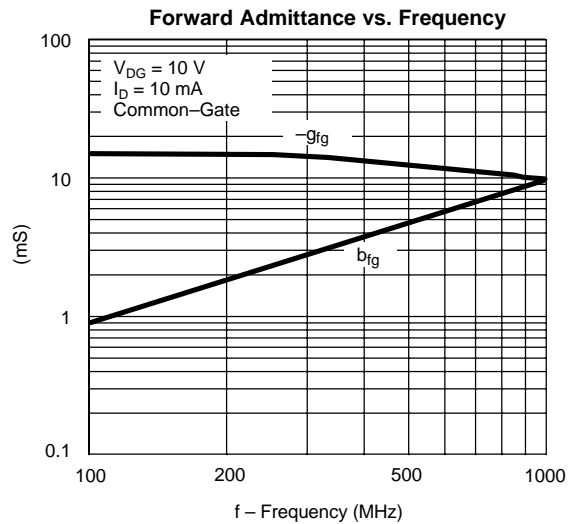
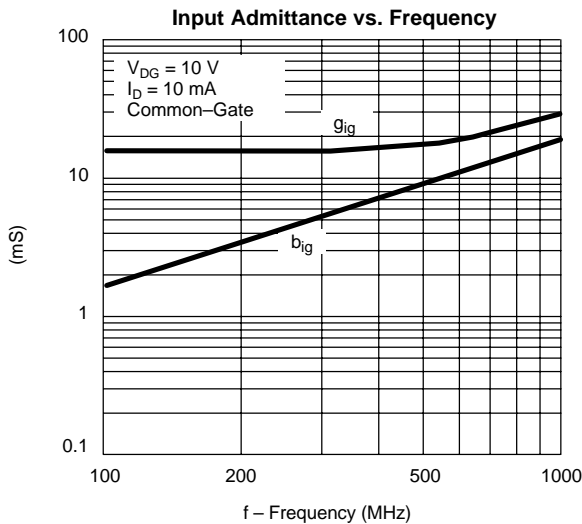
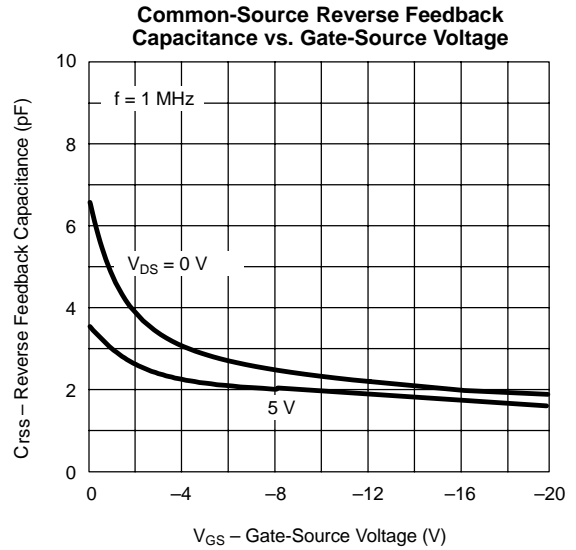
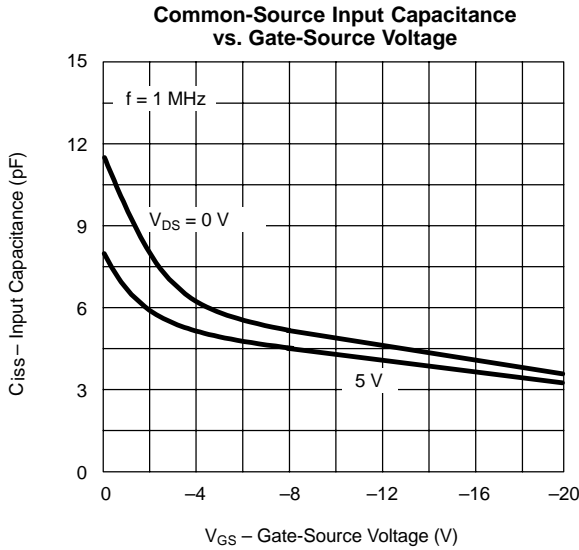
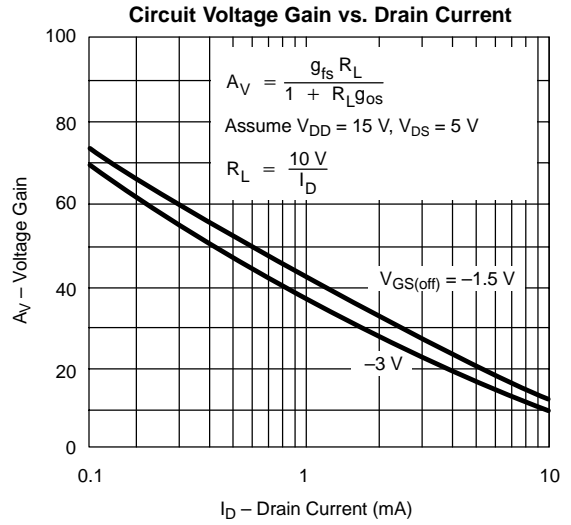
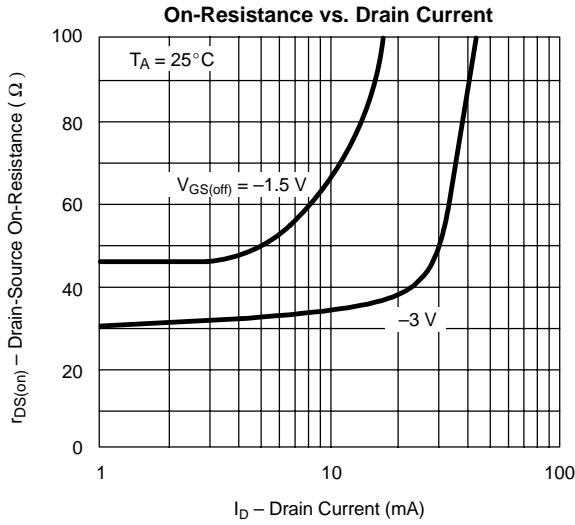




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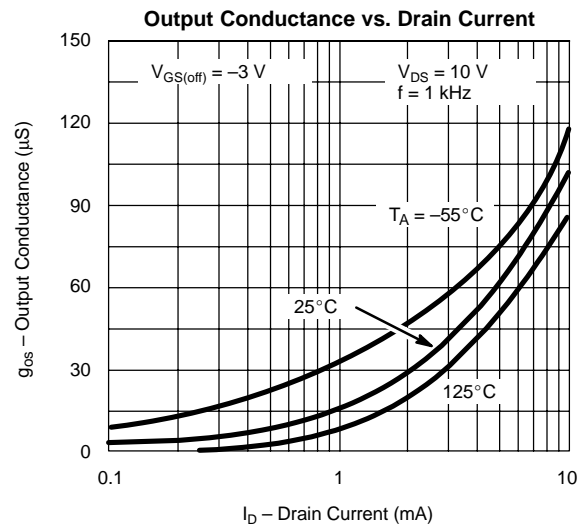
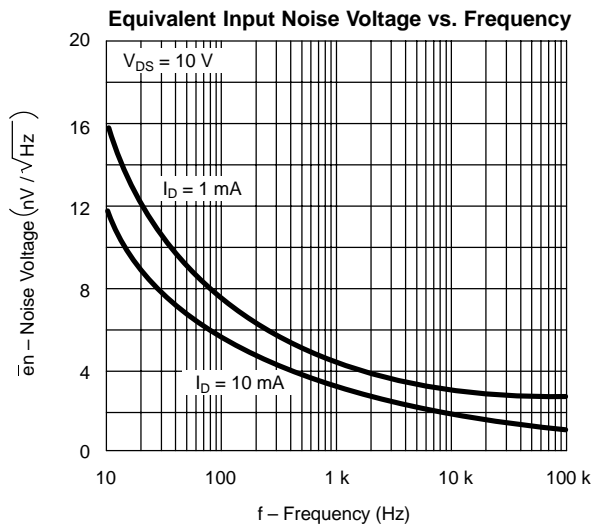
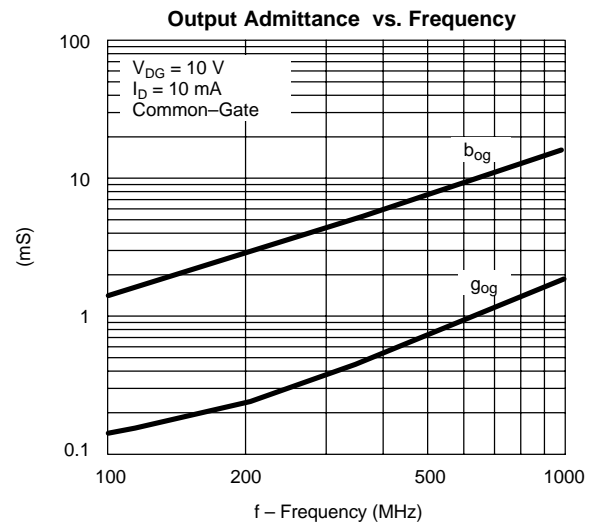
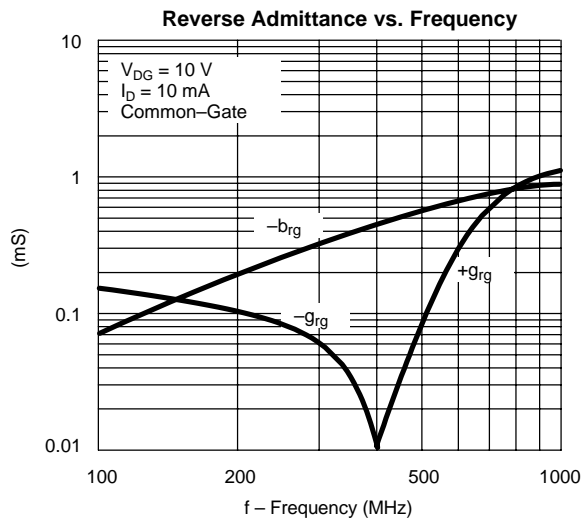


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