

74AC521 • 74ACT521 8-Bit Identity Comparator

General Description

The AC/ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Features

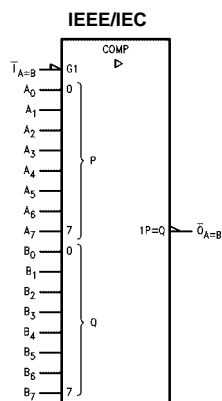
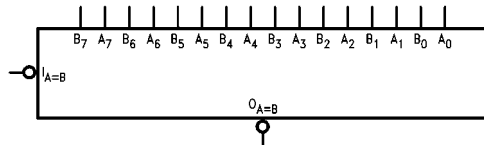
- I_{CC} reduced by 50%
- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- ACT521 has TTL-compatible inputs

Ordering Code:

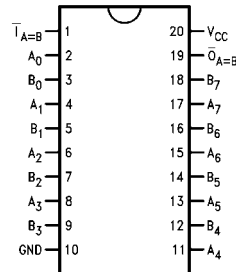
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74AC521SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74AC521SJ | M20D | Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74AC521MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74AC521PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74ACT521SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
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| 74ACT521PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering table.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|--------------------------------|---------------------------|
| A ₀ -A ₇ | Word A Inputs |
| B ₀ -B ₇ | Word B Inputs |
| $\overline{I}_{A=B}$ | Expansion or Enable Input |
| $\overline{O}_{A=B}$ | Identity Output |

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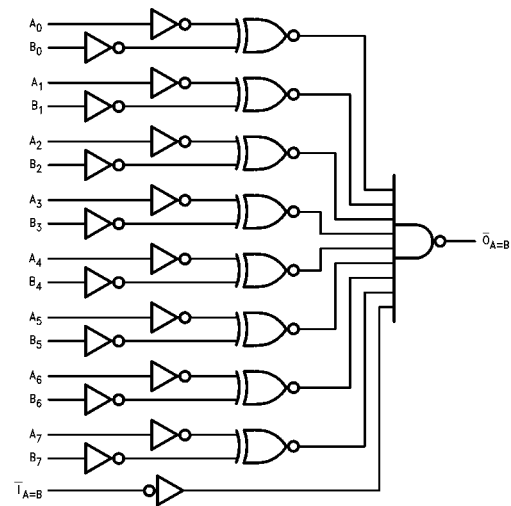
Truth Table

| Inputs | | Outputs |
|-----------------|----------------|-----------------|
| $\bar{I}_{A=B}$ | A, B | $\bar{O}_{A=B}$ |
| L | A = B (Note 1) | L |
| L | A \neq B | H |
| H | A = B (Note 1) | H |
| H | A \neq B | H |

H = HIGH Voltage Level
L = LOW Voltage Level

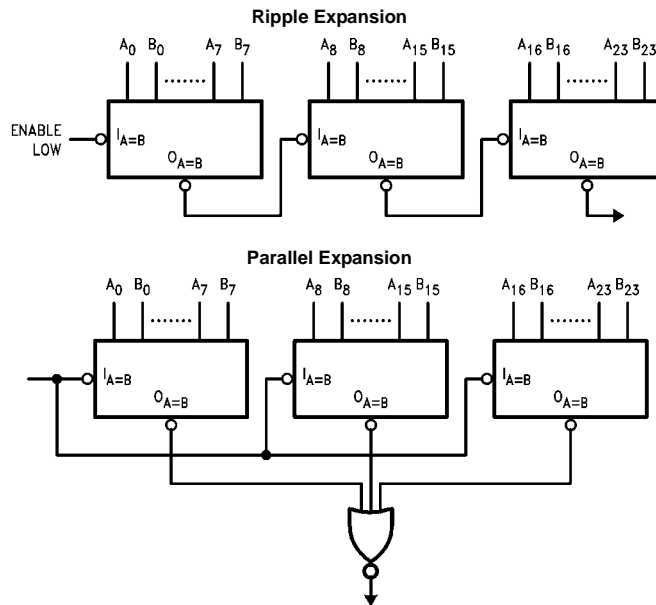
Note 1: A₀ = B₀, A₁ = B₁, A₂ = B₂, etc.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Applications



Absolute Maximum Ratings(Note 2)

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source | |
| or Sink Current (I_O) | ± 50 mA |
| DC V_{CC} or Ground Current | |
| per Output Pin (I_{CC} or I_{GND}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Junction Temperature (T_J) | |
| PDIP | 140°C |

Recommended Operating Conditions

| | |
|---|----------------|
| Supply Voltage (V_{CC}) | |
| AC | 2.0V to 6.0V |
| ACT | 4.5V to 5.5V |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| AC Devices | |
| V_{IN} from 30% to 70% of V_{CC} | |
| V_{CC} @ 3.3V, 4.5V, 5.5V | 125 mV/ns |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| ACT Devices | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | Units | Conditions | |
|----------------------|--------------------------------------|-----------------|---------------------------|-------------------|---|---------------|--|---|
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | 3.0 | 1.5 | 2.1 | 2.1 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 4.5 | 2.25 | 3.15 | 3.15 | | | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | 3.0 | 1.5 | 0.9 | 0.9 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 4.5 | 2.25 | 1.35 | 1.35 | | | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 4.5 | 4.49 | 4.4 | 4.4 | | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | | 3.0 | | 2.56 | 2.46 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 3)}$ |
| | | | 4.5 | | 3.86 | 3.76 | | |
| | | | 5.5 | | 4.86 | 4.76 | | |
| V_{OL} | Maximum LOW Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu\text{A}$ | |
| | | 4.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | | 3.0 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 3)}$ |
| | | | 4.5 | | 0.36 | 0.44 | | |
| | | | 5.5 | | 0.36 | 0.44 | | |
| I_{IN} (Note 5) | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CC}, \text{GND}$ | |
| I_{OLD} | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V \text{ Max}$ | |
| I_{OHD} | Output Current (Note 4) | 5.5 | | | -75 | mA | $V_{OHD} = 3.85V \text{ Min}$ | |
| I_{CC} (Note 5) | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND | |

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

DC Electrical Characteristics for ACT

| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -40°C to +85°C | | Units | Conditions |
|------------------|--|------------------------|------------------------|-------------------|---------------------------------|------|--|---|
| | | | Typ | Guaranteed Limits | | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | V _{OUT} = 0.1V or V _{CC} - 0.1V | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V _{IL} | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | V _{OUT} = 0.1V or V _{CC} - 0.1V | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V _{OH} | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | I _{OUT} = -50 μA | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | | 4.5 | | 3.86 | 3.76 | V | V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 6) |
| | | | 5.5 | | 4.86 | 4.76 | | |
| V _{OL} | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | I _{OUT} = 50 μA | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | | 4.5 | | 0.36 | 0.44 | V | V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 6) |
| | | | 5.5 | | 0.36 | 0.44 | | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | V _I = V _{CC} , GND | |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.5 | mA | V _I = V _{CC} - 2.1V | |
| I _{OLD} | Minimum Dynamic Output Current (Note 7) | 5.5 | | | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current (Note 7) | 5.5 | | | -75 | mA | V _{OHD} = 3.85V Min | |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | V _{IN} = V _{CC} or GND | |

Note 6: All outputs loaded; thresholds on input associated with output under test.

Note 7: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

| Symbol | Parameter | V _{CC} (V) (Note 8) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
|------------------|---|------------------------------------|--|---|-------------|---|-------------|-------|
| | | | Min | Typ | Max | Min | Max | |
| | | | t _{PLH} | Propagation Delay A _n or B _n to $\overline{O}_{A=B}$ | 3.3 5.0 | 3.5 2.5 | 7.0 5.0 | |
| t _{PHL} | Propagation Delay A _n or B _n to $\overline{O}_{A=B}$ | 3.3 5.0 | 4.5 3.0 | 7.5 5.5 | 11.5 8.5 | 3.5 2.5 | 12.5 9.0 | ns |
| t _{PLH} | Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | 3.3 5.0 | 3.0 2.5 | 5.5 4.0 | 8.0 6.0 | 2.5 2.0 | 9.0 7.0 | ns |
| t _{PHL} | Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$ | 3.3 5.0 | 3.0 2.0 | 5.5 4.0 | 8.0 6.0 | 2.5 2.0 | 9.0 7.0 | ns |

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

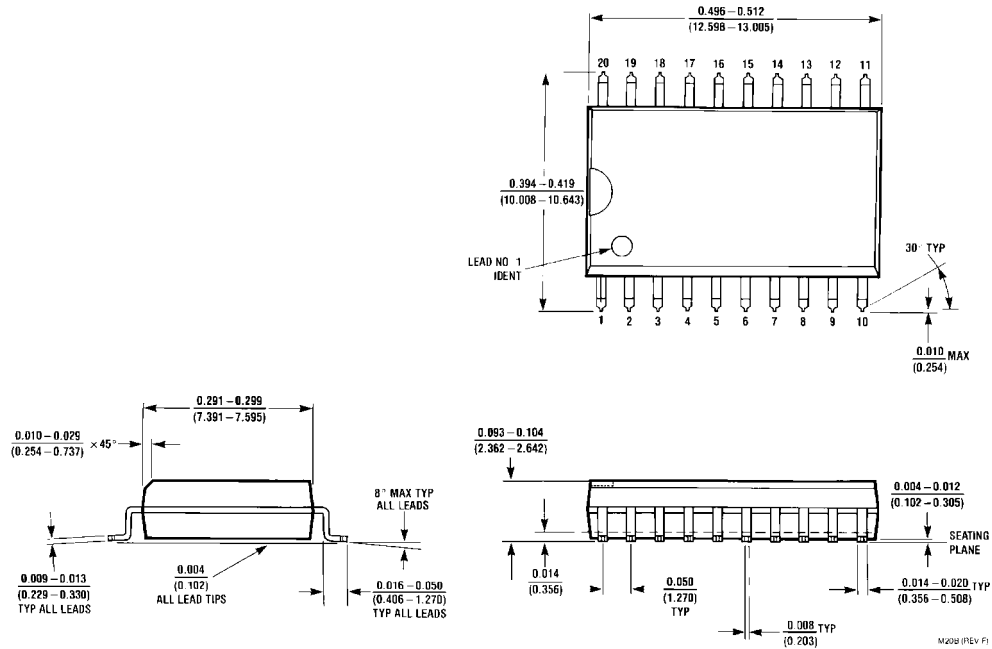
| AC Electrical Characteristics for ACT | | | | | | | | |
|---------------------------------------|---|------------------------------------|--|-----|------|---|------|-------|
| Symbol | Parameter | V _{CC} (V) (Note 9) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay A _n or B _n to $\overline{O}_{A=B}$ | 5.0 | 3.0 | 5.5 | 9.0 | 2.5 | 9.5 | ns |
| t _{PHL} | Propagation Delay A _n or B _n to $\overline{O}_{A=B}$ | 5.0 | 3.0 | 6.0 | 10.0 | 2.5 | 11.0 | ns |
| t _{PLH} | Propagation Delay $\overline{A=B}$ to $\overline{O}_{A=B}$ | 5.0 | 2.0 | 4.0 | 6.5 | 2.0 | 7.0 | ns |
| t _{PHL} | Propagation Delay $\overline{A=B}$ to $\overline{O}_{A=B}$ | 5.0 | 2.5 | 5.0 | 7.5 | 2.0 | 8.0 | ns |

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

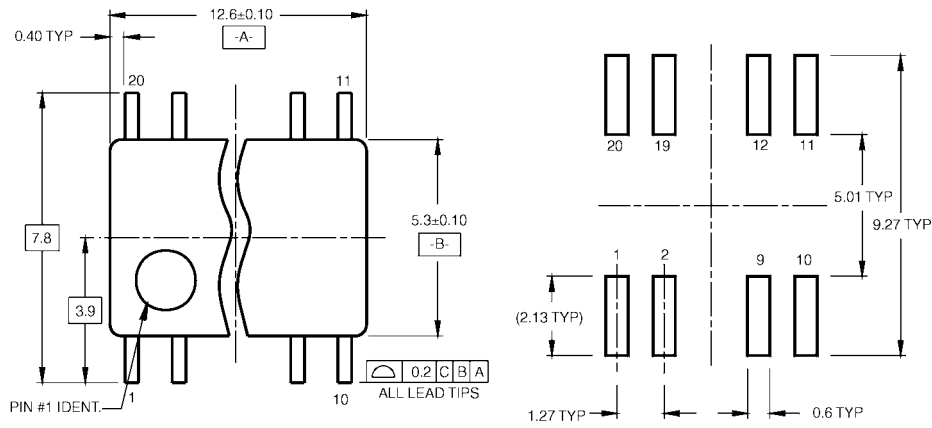
| Symbol | Parameter | Typ | Units | Conditions |
|-----------------|-------------------------------|-----|-------|------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN |
| C _{PD} | Power Dissipation Capacitance | 40 | pF | V _{CC} = 5.0V |

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

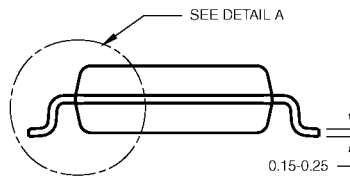
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

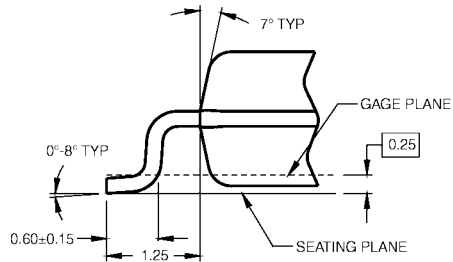


DIMENSIONS ARE IN MILLIMETERS



- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

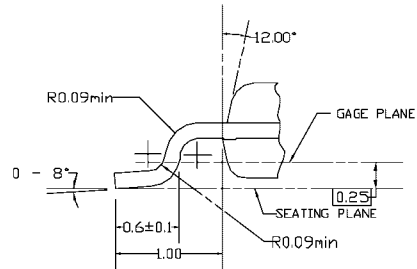
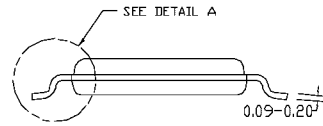
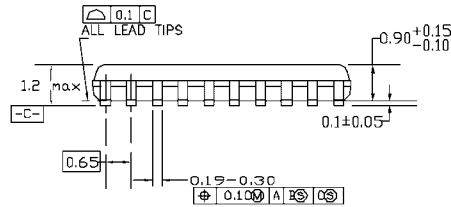
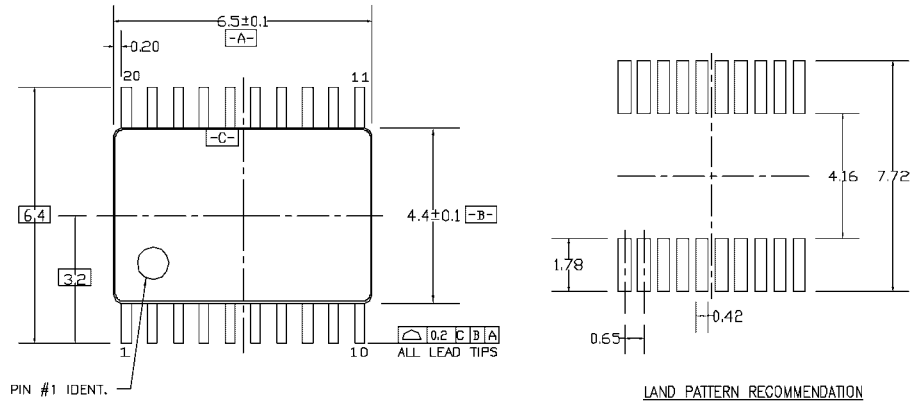
M20DRevB1



DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

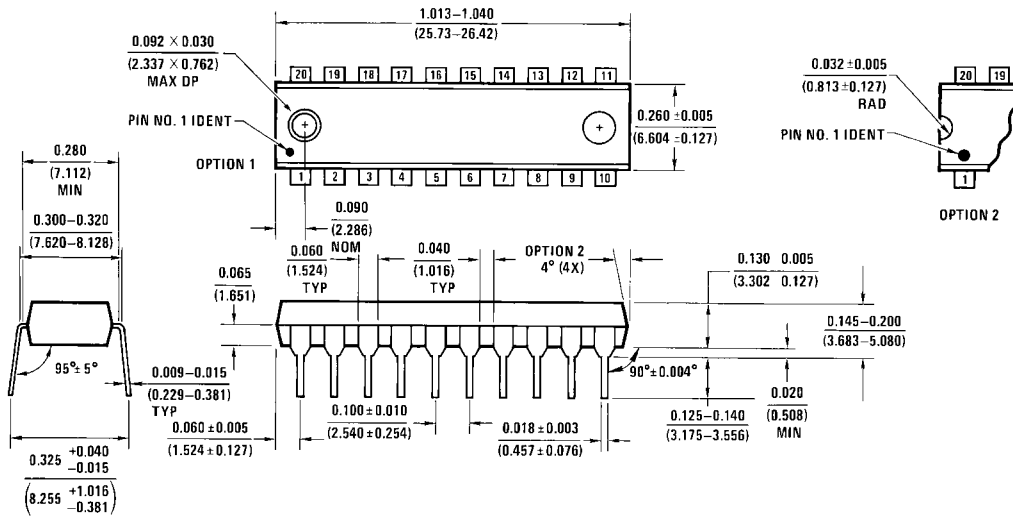
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

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