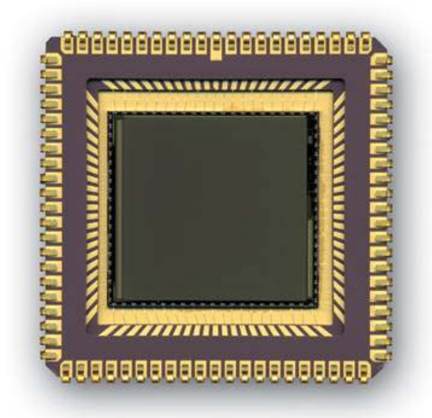
STAR-1000

1 M Pixel
Radiation - Hard
CMOS image sensor



Datasheets

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Document history record

Issue	Date	Description of changes
6.1	4th April, 2003	p6: Table 1: image sensor specs updated. p8: Spectral response curve and photovoltaic response curve added. p18: Package drawing added. p19: Appendix A added. p20: Appendix B added.
6.2	23rd April, 2003	p6: Table 1: image sensor specs updated. p8: Photovoltaic response curve updated. p17: Table 9: VDD_ANA connected internally…
6.3	8th July, 2003	p6: Table 2: values updated. p9: Table 3 and 4 added. p13: Pin connection drawing added. p14: Table 7 updated. p16: Notes added. p17: Package drawing updated. p18: Die alignment added.
6.4	27th September 2004	p1: Layout changed. p7: Table 2 updated. p10: Table 3 updated. p12: Table 5: f: R changed into LD_Y p17: Table 7: Pin 58. Description added. p20: Figure 5 updated.
6.5	4th January 2005	Added equivalent Cypress part numbers and Cypress logo. Added Cypress Document # 38-05714 Rev ** in the document footer.

1. Sensor description

The STAR-1000 is a CMOS image sensor with 1024 by 1024 pixels on a 15-µm pitch. It features on-chip Fixed Pattern Noise (FPN) correction, a programmable gain amplifier and a 10-bit Analog to Digital Converter (ADC).

All circuits are designed using the radiation tolerant design rules for CMOS image sensors to allow a high tolerance against total dose effects.

Registers that can be directly accessed by the external controller contain the X- and Y-addresses of the pixels to be read. This architecture provides flexible operation and allows different operation modes like (multiple) windowing, sub sampling, etc.

The image sensor contains five sections: the pixel array, the X-and Y addressing logic, the column amplifiers, the output amplifier and the ADC. Figure 1 shows an outline diagram of the sensor, including an indication of the main control signals. The following paragraphs explain in more detail the function and operation of the different imager parts.

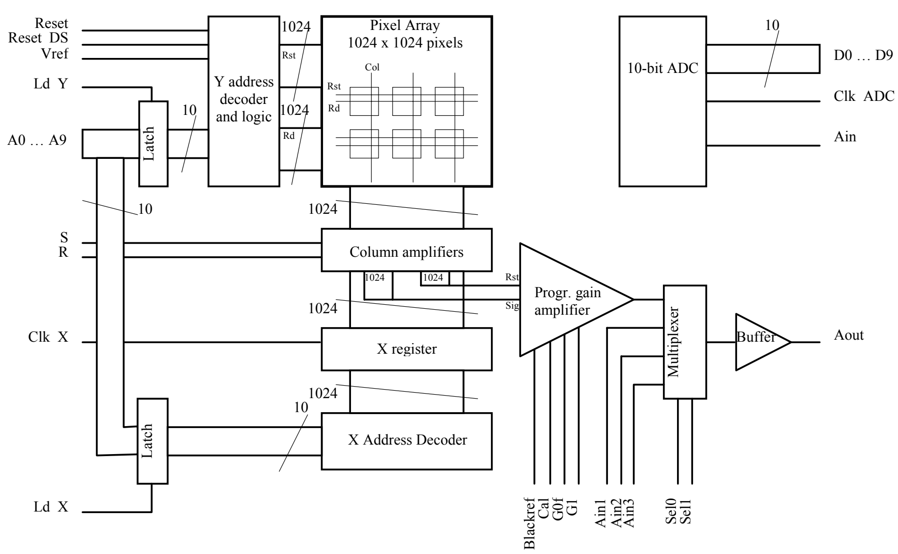


Figure 1: Image sensor outline diagram

Part Numbers	**Color or B/W**
STAR-1000 CYIISM1000AA-HFC -(PRELIMINARY)	B&W

1.1. The pixel array

The pixel array contains 1024 by 1024 active pixels at 15µm pitch. Each pixel contains one photo diode and three transistors (Figure 2).

The photo diode is always in reverse bias. At the beginning of the integration cycle a pulse is applied to the reset line (gate of T1) bringing the cathode of D1 to the reset voltage level. During the integration period photon-generated electrons accumulate

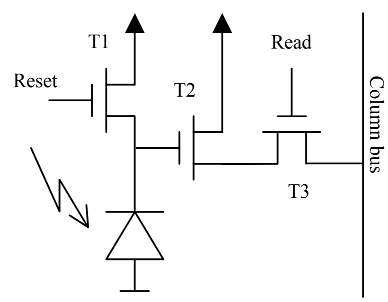


Figure 2: Active pixel electrical diagram

on the diode capacitance, reducing the voltage on the gate of T2. The real illumination-dependent signal is the different between the reset level and the output level after integration. This difference is made in the column amplifiers. T2 acts as a source follower and T3 allows connection of the pixel signal (reset level and output level) to the vertical output bus.

The reset-lines and the read-lines of the pixels in a row are connected together to the Y-decoder logic; the outputs of the pixels in a column are connected together to a column amplifier.

1.2. Addressing logic

The addressing logic allows direct addressing of rows and columns. Instead of the one-hot shift registers that are often used, address decoders are implemented. One can select a line by presenting the required address to the address input of the device and latching it to the Y-decoder logic. Presenting the X-address to the device address input and latching it to the X-address decoder can select a column.

A typical line read out sequence will first select a line by applying the Y-address to the Y-decoder. Activation of the "LD_Y" input on the Y-logic will connect the pixel outputs of the selected line to the column amplifiers. The individual column amplifier outputs can be connected to the output amplifier by applying the respective X-addresses to the X address decoder. Applying the appropriate Y-address to the Y-decoder and activating the "Reset" input reset a line. The integration time of a row is the time between the last reset of this row and time when it is selected for read-out.

The Y-decoder logic has two different reset inputs: "RESET" and "RESET_DS". Activation of "RESET" will reset the pixel to the Vdd level; activation of "RESET_DS" will reset the pixel to the voltage level on the "VREF" input. This feature allows the application of the so-called dual slope integration (see APPENDIX B). If dual slope integration is not needed "VREF" can be tied to Vdd and "RESET_DS" must never be activated.

1.3. The column amplifiers

All outputs from the pixels in a column are connected in parallel to a column amplifier. This amplifier samples the output voltage and the reset level of the pixel whose row is selected at that moment and presents these voltage levels to the output amplifier. As a result the pixels are always reset immediately after read-out as part of the sample procedure and the maximum integration time of a pixel is the time between two read cycles.

1.4. The output amplifier and analog multiplexer

The output amplifier combines subtraction of pixel signal level from reset level with a programmable gain amplifier. Since the amplifier is AC coupled it also contains a provision to maintain and restore the proper DC level.

An analogue signal multiplexer feeds the pixel signal to the final unity gain buffer to provide the required drive capability. Apart from the pixel signal also three other external analogue signals can be fed to the output buffer. All these signals can be digitalised by the on-chip ADC if the output of this buffer is externally connected to the input of the ADC.

The purpose of the additional analogue inputs ("A_IN1", "A_IN2" and "A_IN3") is to allow a possibility to process other analogue signals through the image sensors signal path. These signals can thus be converted by the ADC and processed by the image controller FPGA. The additional analogue inputs are intended for low frequency or DC signals and have a reduced bandwidth, compared with the image signal path.

1.5. The ADC

The image sensor has a 10-bit ADC that is electrically separated from the rest of the image sensor circuits and can be powered down if an external ADC is used. The conversion takes place at the falling edge of the clock and the output pins can be disabled to allow operation of the device in a bus structure.

2. Image sensor specifications

2.1. General specifications

Table 1: General specification of the STAR-1000 sensor

Parameter	Specification	Comment
Detector technology	CMOS Active Pixel Sensor	
Pixel structure	3-transistor active pixel	Radiation-tolerant pixel design.
Photodiode	High fill factor photodiode	Using N-well technique
Sensitive area format	1024 x 1024 pixels	
Pixel size	15 x15 μm^2	
Pixel output rate	12 MHz	Speed can be exchanged for power consumption
Windowing	X- and Y- addressing random programmable	
Electronic shutter	Electronic rolling shutter. Range: 1 : 1024	Integration time is variable in time steps equal to the row readout time.
Total Dose Radiation tolerance	> 230Krad (Si)	Pixel test structures with a similar design have shown total dose tolerance up to several Mrad. Radiation tests on similar image sensor were performed up to 230 Krad.
Expected Equivalent fluence at 10 MeV	3.10^{10} proton/cm^2	TBD.
SEL threshold	> 28 MeV cm^3 mg^{-1}	A similar design was tested up to 28 MeV without any latch up noticeable. No other evaluations have been done yet.

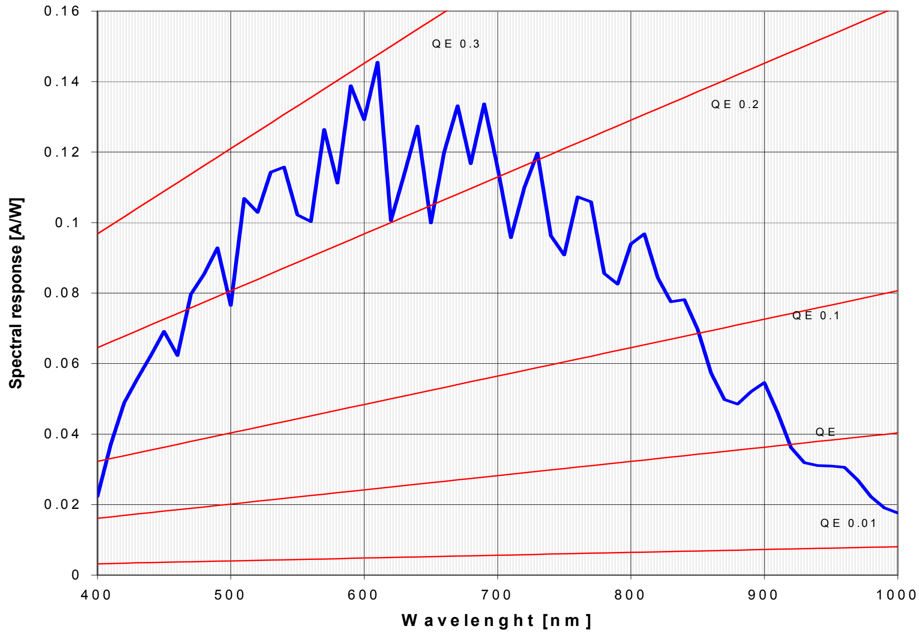
2.2. Electro-optical specifications

Table 2: Electro-optical specifications of the STAR-1000 sensor

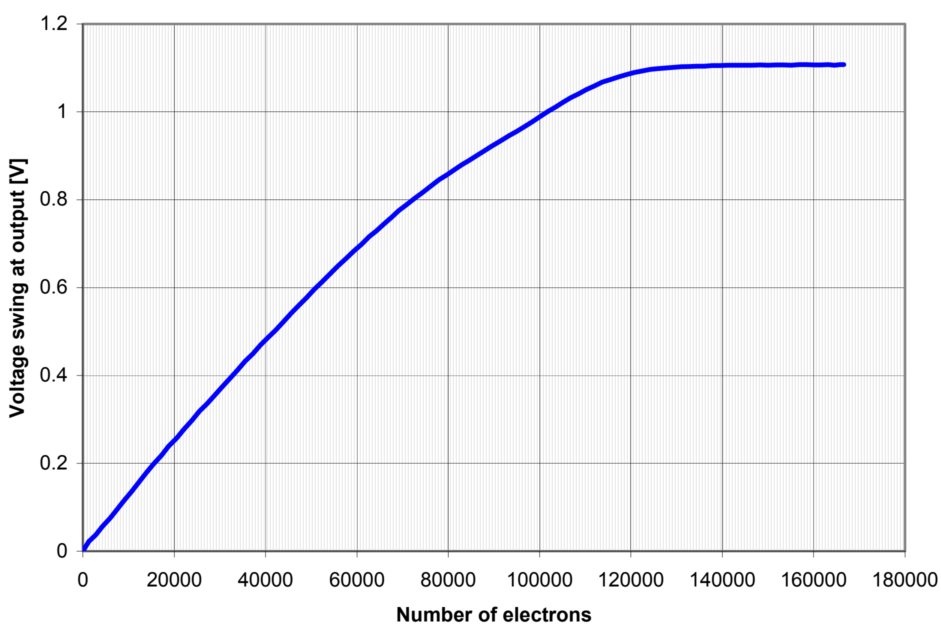
Parameter	Value		Comment
	Typical value	Unit	
Spectral range	400 - 1000	nm	
Quantum efficiency x fill factor	20%		Average over the visual range. See spectral response curve.
Full well capacity	135.000	e-	

Parameter	Value		Comment
	Typical value	Unit	
Saturation capacity to meet non-linearity within ± 5%	99.000	e-	
Output signal swing	1.1	V	
Conversion gain	11.4	µV/e-	
kTC noise	35	e-	
Dynamic Range	72	dB	
Fixed Pattern Noise	Local: 1σ < 0.30% Global: 1 σ <0.56% of full well		
Photo Response Non-uniformity at Qsat/2 (RMS)	Local: 1σ < 0.67% Global: σ <3.93% of full well		
Average Dark Current at 293 K	223	pA/cm^2	
Dark current signal	3135	e- / s	
DSNU signal	1.055 % of Vsat		
Optical cross-talk at 600 nm	Vertical: 16 % Horizontal: 17.5 %		
Anti-blooming capacity	x 1000		
Output amplifier gain	x1, x2.47, x4.59 and x8.64		Controlled by 2 bits
Analogue input bandwidth	9.5	MHz	
Analogue input signal range	0.1 to 4.9	V	
Analog-Digital converter	10	Bit	Radiation-tolerant version of the ADC on Ibis4 and other image sensors.
ADC Differential Non-Linearity (DNL)	<= ±3.5	LSB	
ADC Integral Non-Linearity (INL)	<= ±5.8	LSB	Integral non-linearity of ADC is better than linearity of image sensor.
Supply voltage	5	V	Digital input signals are 3.3 V compatible
Power Dissipation	< 350 < 100	mW	With internal ADC powered. Without internal ADC powered. Both values measured at nominal speed (12 MHz).

2.3. Spectral response curve



2.4. Photo-voltaic response



2.5. Absolute maximum ratings

Table 3:Absolute maximum ratings

Characteristics	Symbol	Limits		Units	Remarks
		Min	Max		
Any supply voltage		-0.5	+7	V	
Voltage on any input terminal		-0.5	Vdd + 0.5	V	
Operating temperature		0	+60	°C	Temperature range to be confirmed by evaluation testing
Storage temperature		-10	+60	°C	Not longer than 1 hour. Temperature range to be confirmed by evaluation testing
Soldering temperature		NA	260 (TBC)	°C	Maximum solder temperature to be confirmed by evaluation testing

2.6. DC operating conditions

Table 4: DC operating conditions

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
VDDA	Analog supply of the image core.		5		V
VDDD	Digital supply of the image core.		5		V
VDD_ADC_ANA	Analog supply of the ADC circuitry.		5		V
VDD_ADC_DIG	Digital supply of the ADC circuitry.		5		V
VDD_DIG_OUT	Power supply of ADC digital output stage.		5		V
VRES	Reset level for RESET signal.		5		V
VREF	Reset level for RESET_DS signal.	4		5	V
GNDA	Analog ground of the image core.		0		V
GNDD	Digital ground of the image core.		0		V
GND_ADC_ANA	Analog ground of the ADC circuitry.		0		V
GND_ADC_DIG	Digital ground of the ADC circuitry.		0		V
V_{IH}	Logical '1' input voltage.	1.8		VDDD	V
V_{IL}	Logical '0' input voltage.	0		1	V
V_{OH}	Logical '1' output voltage.	4.25		VDDD	V
V_{OL}	Logical '0' output voltage.			1	V

3. Timing and control signals

The pixels addressing is done by direct addressing of rows and columns. This approach has the advantage of full flexibility when accessing the pixel array: multiple windowing and sub-sampled read-out are possible by proper programming.

The following paragraphs clarify the timing for row- and column readout.

3.1. Row selection and reset timing

Figure 3 shows the timing of the line sequence control signals. The timing constraints are given in table 5.

The address, presented at the address IO pins (A0…A9) is latched in with the LD-Y pulse (active low). After latching; the external controller can already produce a new address.

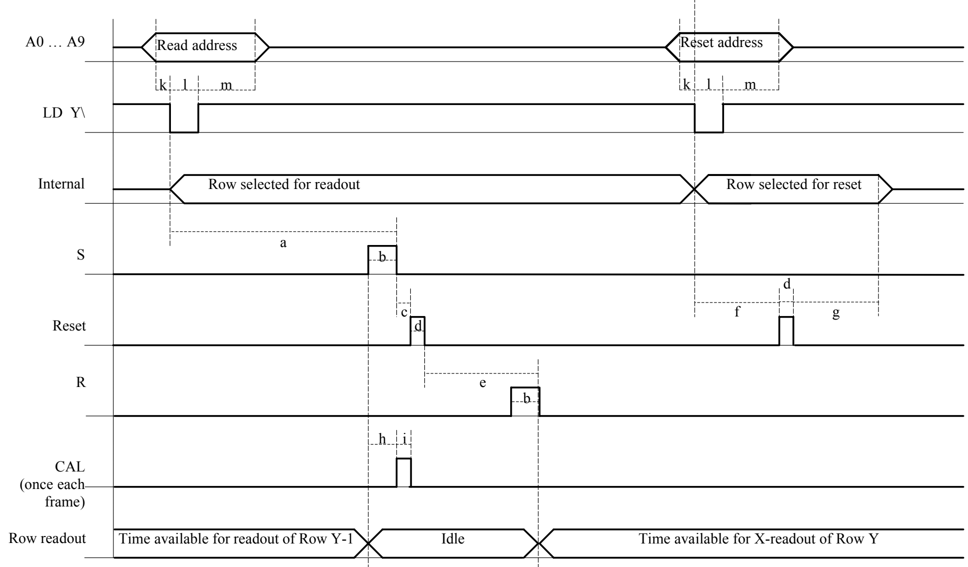


Figure 3: Line selection and reset sequence

Latching in a Y-address selects the addressed row and connects the pixel outputs of that row to the column amplifiers. Through the sequence of the S and R pulse and the Reset pulse in-between the pixel output signal and reset level are sampled and produced at the output of the column amplifier (to do the FPN double sampling correction).

At this time horizontal read-out of the selected row can start and another row can be reset to effectuate reduced integration time (electronic rolling shutter).

Table 5 shows the timing constraints for the horizontal or line-select timing.

Table 5: Timing constraints of line sequence

Symbol	Min.	Typ.	Description
a	3.6 µs		Delay between selection of a new row and falling edge on S. Minimal value: For maximum speed a new row can already be selected during X-readout of the previous row.
b	0.4 µs		Duration of S and R pulse.
c	0	100 ns	Delay between falling edge of S and rising edge of Reset.
d	200 ns		Minimum duration of Reset pulse.
e	1.6 µs		Delay between falling edge of Reset and falling edge of R.
f	0	100 ns	Minimum delay between falling edge on LD_Y and rising edge of Reset.
g		100 ns	Minimum required extension of Y-address after falling edge of reset pulse.
h	100 ns	200 ns	Position of Cal pulse after rising edge of S. The cal pulse must only be given once per frame.
i	100 ns	1 µs	Duration of Cal pulse.
k	10 ns		Address set-up time.
l	20 ns		Load register value.
m	10 ns		Address stable after load.

3.2. Pixel read-out timing

Figure 4 shows the timing of the pixel readout sequence. The external digital controller presents a column address that is latched in by the rising edge of the LD_X pulse. After decoding the X-address the column selection is clocked in the X-register

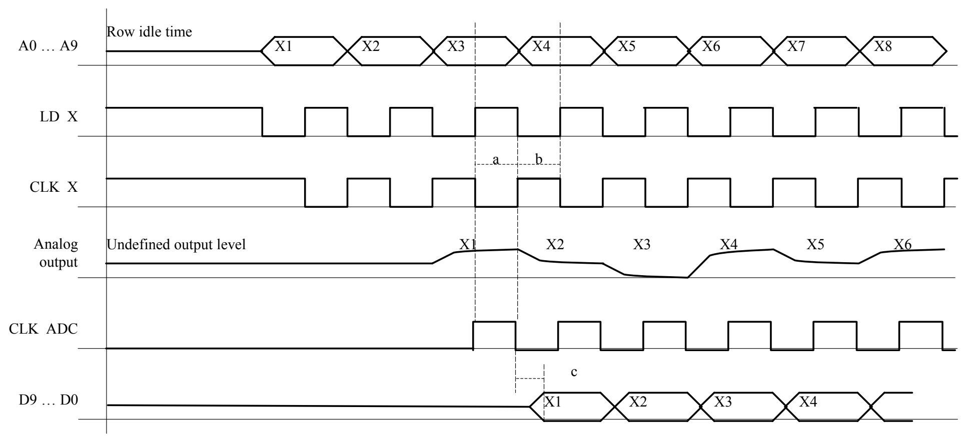


Figure 4: Column selection and read-out sequence

by CLK-X. The output amplifier uses the same pulse to subtract the pixel output level from the pixel-reset level and the signal level. This causes a pipeline effect such that the analog output of the first pixel is effectively present at the device output terminal at the third rising edge of the X-CLK signal.

The ADC conversion starts at the falling edge of the CLK-ADC signal and produces a valid digital output 20ns after this edge. The timing of these signals is given in table 3.

Table 6: Timing constraints of column read out

Symbol	Min	Typ	Description
a	40 ns		Address setup time
b	40 ns		Address valid time
c	0	20 ns	ADC output valid after falling edge of CLK_ADC

4. Pin list

Table 6 is a list of the pin connections; the following tables group the connections by their functionality.

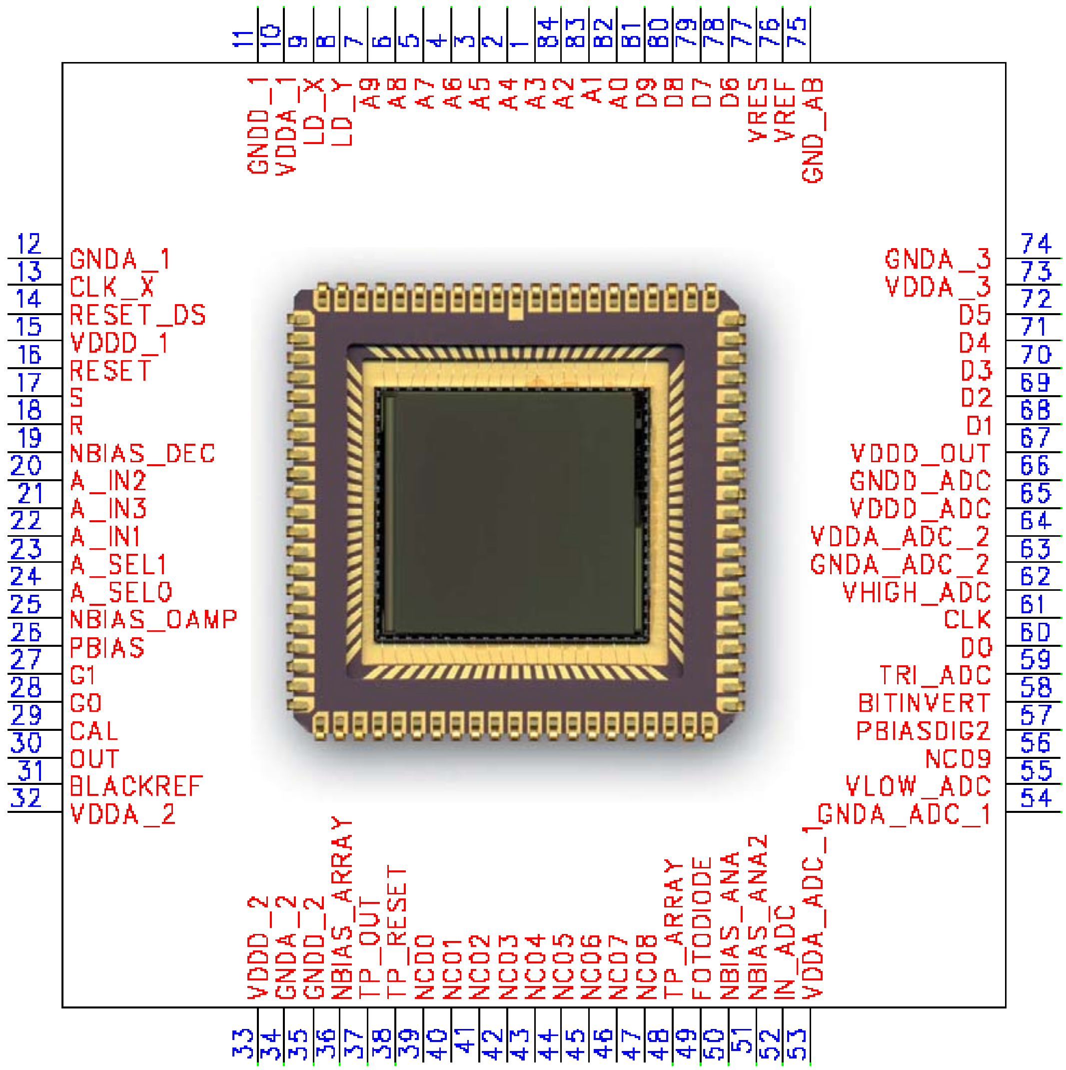


Figure 3: STAR-1000 pin connections

Table 7: Pin list of the STAR-1000 sensor

Pin	Pin name	Pin type	Pin description
1	A3	Input	Digital input. Address inputs for row and column addressing. A9=LSB, A0=MSB.
2	A4	Input	
3	A5	Input	
4	A6	Input	
5	A7	Input	
6	A8	Input	
7	A9	Input	
8	LD_Y	Input	Digital Input. Latch address (A0…A9) to Y-register (0 = track, 1 = hold).
9	LD_X	Input	Digital Input. Latch address (A0…A9) to X-register (0 = track, 1 = hold).
10	VDDA	Supply	Analog power supply of the imager (typical 5V).
11	GNDD	Ground	Digital ground of the imager.
12	GNDA	Ground	Analog ground of the imager.
13	CLK_X	Input	Digital input. Clock X-register (output valid & stable when CLK_X is high).
14	RESET_DS	Input	Digital input (high active). Resets row indicated by Y-address (see sensor timing diagram). RESET_DS can be used for dual-slope integration (see FAQ). Connect to GND for normal operation.
15	VDDD	Supply	Digital supply of the image sensor.
16	RESET	Input	Digital input (high active). Resets row indicated by Y-address (see sensor timing diagram).
17	S	Input	Digital input (high active). Control signal for column amplifier (see sensor timing diagram).
18	R	Input	Digital input (high active). Control signal for column amplifier (see sensor timing diagram).
19	NBIAS_DEC	Input	Analog input. Biasing of address decoder. Connect with 100kΩ to VDDA and decouple with 100 nF to GND.
20	A_IN2	Input	Additional analog inputs. For proper conversion with on-chip ADC the input signal must lie within the output signal range of the image sensor (approximately +2V to +4V).
21	A_IN3	Input	
22	A_IN1	Input	
23	A_SEL1	Input	Selection of analog channel: '00' selects image sensor ('01' selects A_IN1; '10' A_IN2 and '11' A_IN3).
24	A_SEL0	Input	
25	NBIAS_OAMP	Input	Analog input. Bias of output amplifier (speed/power control). Connect with 100kΩ to VDDA and decouple with 100 nF to GND for 12.5 MHz output rate (lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation).
26	PBIAS	Input	Analog input. Biasing of the multiplexer circuitry. Connect with 20kΩ to GND and decouple with 100nF to VDD.
27	G1	Input	Digital input. Select output amplifier gain value: G0 =

Pin	Pin name	Pin type	Pin description
28	G0	Input	LSB; G1 = MSB ('00' = unity gain; '01' = x2; '10'= x4; '11'=x8).
29	CAL	Input	Digital input (active high). Initialization of output amplifier. Output amplifier will output BLACKREF in unity gain mode when CAL is high (1). Apply pulse pattern (see sensor timing diagram).
30	OUT	Output	Analog output video signal. To be connected to the analog input of the internal (pin 52) 10-bit ADC or an external ADC.
31	BLACKREF	Input	Analog input. Control voltage for output signal offset level. Buffered on-chip, the reference level can be generated by a 100kΩ resistive divider. Connect to 2 V DC for use with on-chip ADC.
32	VDDA	Supply	Analog power supply of image core (typical 5 V).
33	VDDD	Supply	Digital power supply of image core (typical 5V).
34	GNDA	Ground	Analog ground of image core.
35	GNDD	Ground	Digital ground of image core.
36	NBIAS_ARRAY	Input	Analog input. Biasing of the pixel array. Connect with 1MΩ to VDDA and decouple with 100 nF capacitor to GND.
37	TESTPIX_OUT	Output	Output of single test pixel. Can be used for electro-optical evaluation.
38	TESTPIX_RESET	Input	Digital input (active high). Reset signal of single test pixel. Used to reset the single test pixel during electro-optical evaluation.
39	n.c.		
40	n.c.		
41	n.c.		
42	n.c.		
43	n.c.		
44	n.c.		
45	n.c.		
46	n.c.		
47	n.c.		
48	TESTPIXARRAY	Output	Analog output of an array of 20 x 35 test pixels where all photodiodes are connected in parallel. Can be used for electro-optical evaluation.
49	PHOTODIODE	Output	Plain photo diode (without circuitry). Area of the photodiode = 20 x 35 pixels. Can be used for electro-optical evaluation.
50	NBIAS_ANA	Input	Analog input. Analog biasing of the ADC circuitry. Connect with 100kΩ to VDDA and decouple with 100nF to GND.
51	NBIAS_ANA2	Input	
52	IN_ADC	Input	Analog input of the internal ADC. Connect to analog output of image sensor (pin 30). Input range (typically 2V and 4V) of the internal ADC is set between by VLOW_ADC (pin 55) and VHIGH_ADC (pin 62).
53	VDD_ADC_ANA	Supply	Analog power supply of the ADC (typical 5V).
54	GND_ADC_ANA	Ground	Analog ground of the ADC.

Pin	Pin name	Pin type	Pin description
55	VLOW_ADC	Input	Low reference voltage of internal ADC. Nominal input range of the ADC is between 2V and 4V. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 kΩ. Connect with 1k5Ω to GND and decouple with 100nF to GND.
56	n.c.		
57	PBIASDIG2	Input	Connect with 20K to GND and decouple with 100nF to VDDA.
58	BITINVERT	Input	Digital input. Inversion of the ADC output bits. 0 = invert output bits (0 => black: 1023; white: 0), 1 = no inversion of output bits (black: 0; white: 1023).
59	TRI_ADC	Input	Digital input. Tri-state control of digital ADC outputs (1 = tri-state; 0 = normal mode).
60	D0	Input	ADC output bits. D0 = LSB, D9=MSB.
61	CLK	Input	Digital input. ADC clock. ADC converts on falling edge.
62	VHIGH_ADC	Input	High reference voltage of internal ADC. Nominal input range of the ADC is between 2V and 4V. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 kΩ. Connect with 1k1Ω to VDDA and decouple with 100nF to GND.
63	GND_ADC_ANA	Ground	Analog ground of the ADC circuitry.
64	VDD_ADC_ANA	Supply	Analog supply of the ADC circuitry (typical 5V).
65	VDD_ADC_DIG	Supply	Digital supply of the ADC circuitry (typical 5V).
66	GND_ADC_DIG	Output	Digital ground of the ADC circuitry.
67	VDD_DIG_OUT	Supply	Power supply of ADC digital output. Connect to 5V for or normal operation. Can be brought to lower voltage when image sensor must be interfaced to low voltage periphery.
68	D1	Output	ADC output bits. D0 = LSB, D9=MSB.
69	D2	Output	
70	D3	Output	
71	D4	Output	
72	D5	Output	
73	VDDA	Supply	Analog supply of the image core (typical 5V).
74	GNDA	Ground	Analog ground of the image core (typical 5V).
75	GND_AB	Supply	Anti-blooming drain control voltage. Default: connect to ground, the anti-blooming is operational but not maximal. Apply 1 V DC for improved anti-blooming.
76	VREF	Supply	Analog supply. Reset level for RESET_DS. Can be used for extended optical dynamic range. See FAQ for more details.
77	VRES	Supply	Analog supply. Reset level for RESET (typical 5V).
78	D6	Output	ADC output bits. D0 = LSB, D9=MSB.
79	D7	Output	
80	D8	Output	
81	D9	Output	

Pin	Pin name	Pin type	Pin description
82	A0	Input	Digital input. Address inputs for row and column addressing. A9=LSB, A0=MSB.
83	A1	Input	
84	A2	Input	

Notes:

1. All pins with the same name can be connected together.
2. Unused inputs must always be tied to an appropriate level, e.g. VDD or GND.
3. Note on power up behaviour:
   At power-on, the image sensor is in an undefined state. It is advised that after start-up an address is latched ASAP into the Y-decoder and the X-decoder to prevent high current consumption.
4. There's no on-chip power supply rejection whatsoever. This means that every noise signal on the analog supply voltages is copied directly to the analog video signal (decoupling of the supply voltages as close as possible to the image sensor is recommended).

5. Packaging and Geometrical constraints

5.1. Package drawing

The detector is packaged in an 84-pin J-leaded package.

The detector is mounted into position with thermally and electrically conductive adhesive. The bottom plate of the cavity will be electrically connected to a ground pin.

The detector will be positioned into the cavity such that the optical centre of the detector coincides with the geometrical centre of the cavity within a tolerance of ± 50 µm in X- and Y direction. The tolerance on the parallelism of the detector is ± 50 µm in X- and Y-direction.

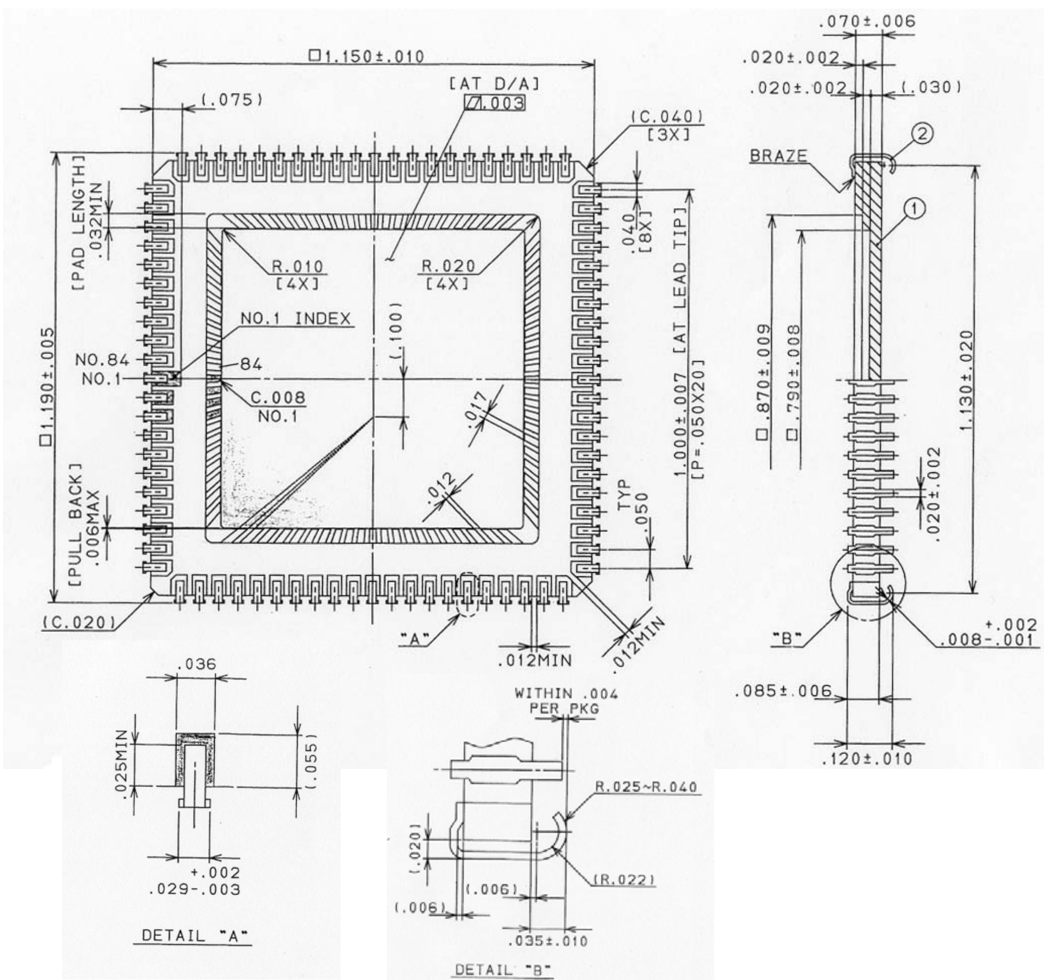


Figure 4: Package drawing

5.2. Die alignment

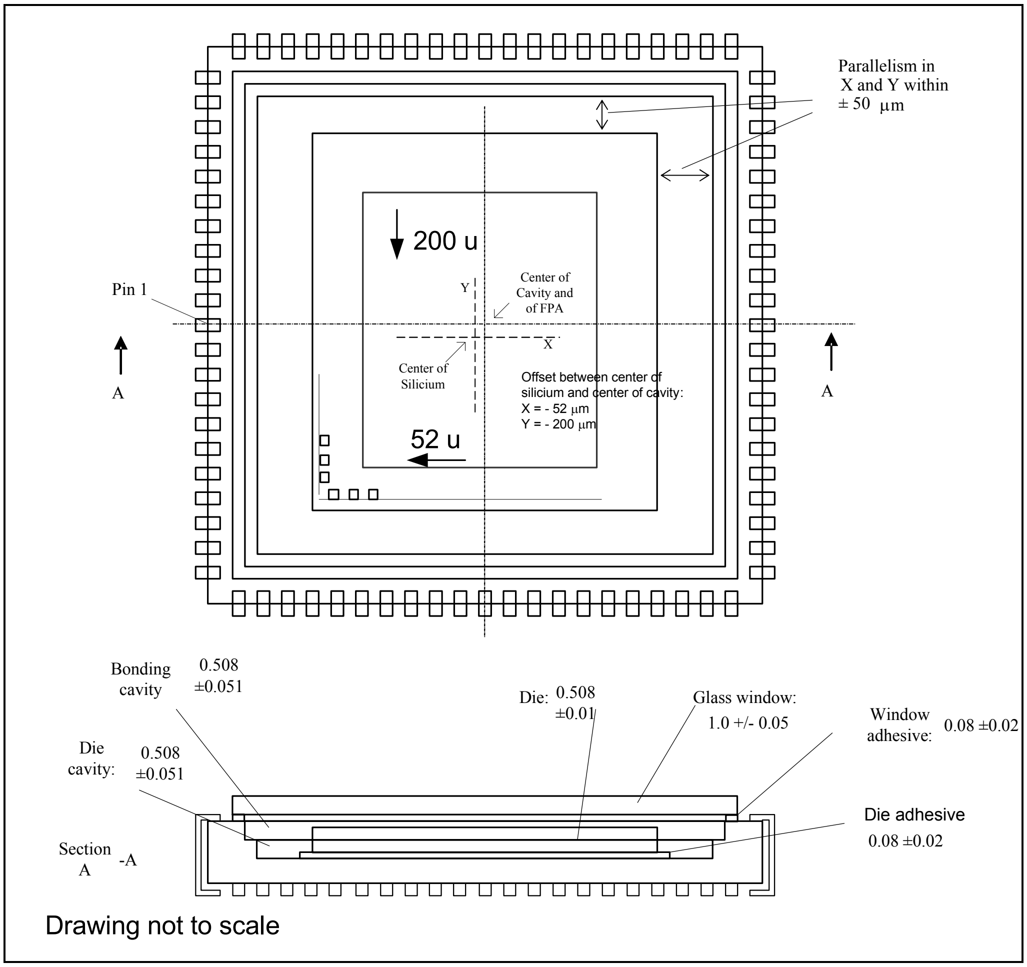


Figure 5: Die alignment

6. Ordering Information

FillFactory Part Number	Cypress Semiconductor Part Number
STAR-1000	CYIS1SM1000AA-HFC - (Preliminary)

Disclaimer

FillFactory image sensors are only warranted to meet the specifications as described in the production data sheet. FillFactory reserves the right to change any information contained herein without notice.

Please contact info@FillFactory.com for more information.

APPENDIX A: STAR-1000 evaluation system

For evaluating purposes an STAR-1000 evaluation kit is available.

The STAR-1000 evaluation kit consists of a multifunctional digital board (memory, sequencer and IEEE 1394 Fire Wire interface) and an analog image sensor board.

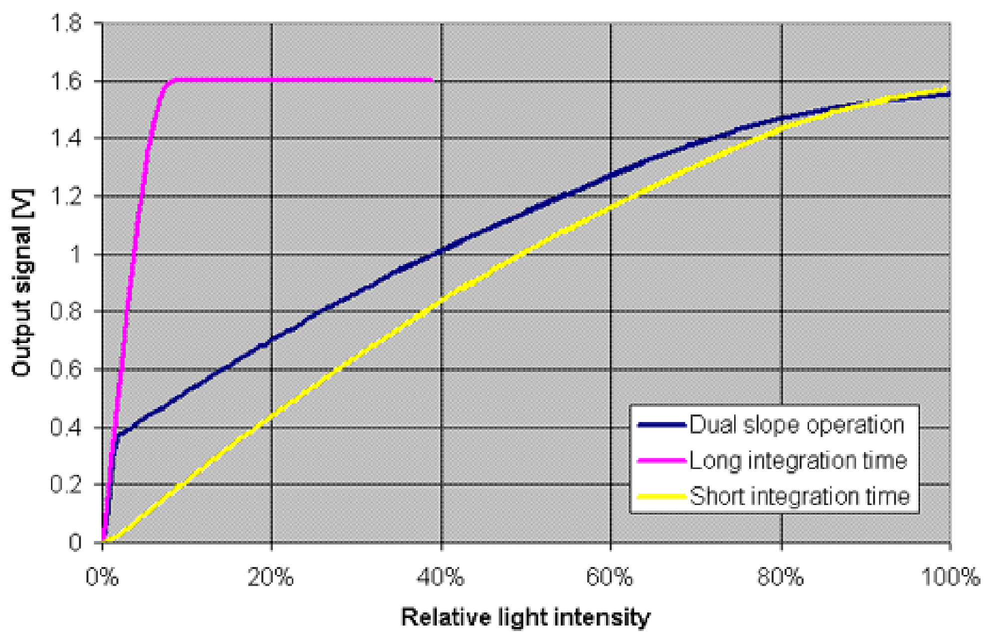
Visual Basic software (under Win 2000 or XP) allows the grabbing and display of images from the sensor. All acquired images can be stored in different file formats (8 or 16-bit). All setting can be adjusted on the fly to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state.

Please contact Fillfactory (info@Fillfactory.com) if you want any more information on the evaluation kit.

APPENDIX B: Frequently Asked Questions

Q: ***How does the dual slope extended dynamic range mode works?***

A: Dual slope is a method to extend the dynamic range of a normally linear-transfer imager, by combining the images taken with a long integration time (dark areas of a scene) and a short integration time (bright areas of a scene) into one image and this in one integration time cycle i.e. without combining two different images. The resulting electro-optical transfer curve is bi-linear.



Please look at our website to find some pictures with extended dynamic range: http://www.fillfactory.be/htm/technology/htm/dual-slope.htm.

Document History Page

Document Title: STAR-1000 1M Pixel Radiation Hard CMOS Image Sensor
Document Number: 38-05714

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	310213	See ECN	SIL	Initial Cypress release

EOD