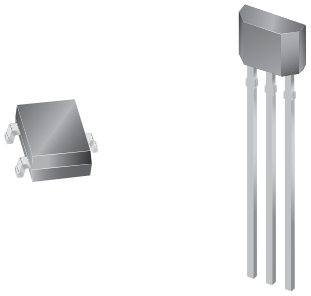
Sensitive Two-Wire Chopper-Stabilized Unipolar Hall Effect Switches

Features and Benefits

- Chopper stabilization
  - Low switchpoint drift over operating temperature range
  - Low sensitivity to stress
- Factory programmed at end-of-line for optimized switchpoints
- On-chip protection
  - Supply transient protection
  - Reverse-battery protection
  - On-board voltage regulator
  - 3.5 to 24 V operation

Packages: 3 pin SOT23W (suffix LH), and 3 pin SIP (suffix UA)



Not to scale

Description

The A1140, A1142, and A1143 devices are sensitive, two-wire, unipolar, Hall effect switches that are factory-programmed at end-of-line to optimize magnetic switchpoint accuracy. These devices use a patented high frequency chopper-stabilization technique, produced using the Allegro advanced BiCMOS wafer fabrication process, to achieve magnetic stability and to eliminate offset inherent in single-element devices exposed to harsh application environments.

Commonly found in a number of automotive applications, these switches are utilized in sensing seat track position, seat belt buckle presence, hood/trunk latching, and shift selector position. Two-wire unipolar switches, such as the A1140/A1142/A1143 family, are particularly advantageous in price-sensitive applications because they require one less wire for operation than do switches with the more traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges. Any current level not within these ranges indicates a fault condition. The A1140/A1142/A1143 family of switches also features on-chip

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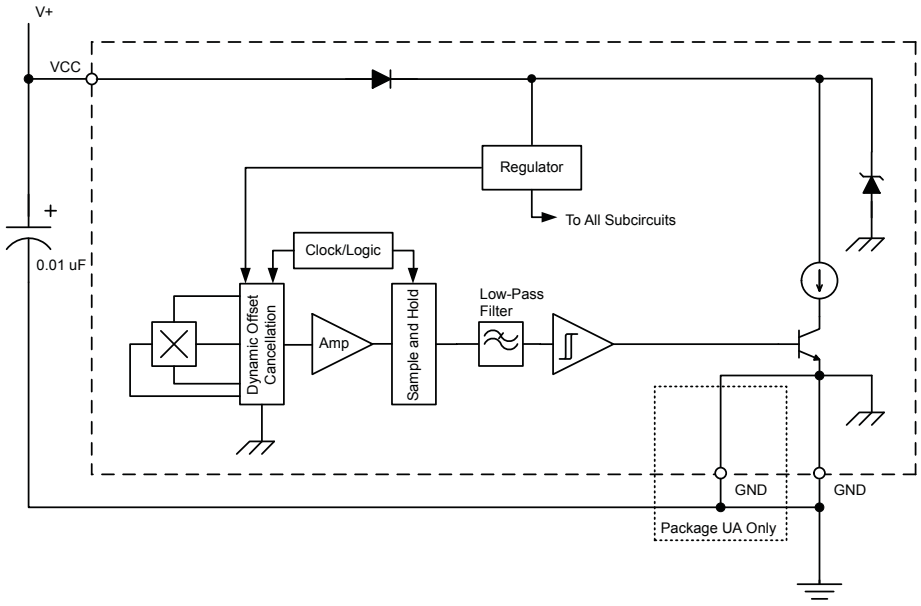
Functional Block Diagram



Description (continued)

transient protection and a Zener clamp to protect against overvoltage conditions on the supply line.

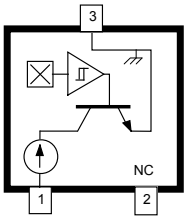
The output currents of the A1143 switch HIGH in the presence of a south (+) polarity magnetic field of sufficient strength, and switch LOW otherwise, as in the presence of a weak field or a north (–) polarity field. The other two devices in the family (A1140 and A1142) have an opposite output: the currents switch LOW in the presence of a south-polarity magnetic field of sufficient strength, and switch HIGH otherwise. The other differences in the switches are their defined low current levels and magnetic switchpoints.

All versions are offered in two package styles. The LH is a SOT-23W, miniature low-profile package for surface-mount applications. The UA is a three-lead ultramini SIP for through-hole mounting. Each package is available in a lead (Pb) free version (suffix, *–T*) with 100% matte tin plated leadframe. Field-programmable versions also available: A1180, A1182, and A1183.

Absolute Maximum Ratings

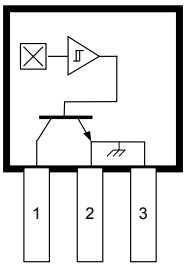
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Package LH, 3-pin SOT



1. VCC
2. No connection
3. GND

Package UA, 3-pin SIP



1. VCC
2. GND
3. GND

Product Selection Guide

Part Number	Packing[1]	Package	Operating Ambient Temperature, T_A (°C)	Output Level in South (+) Field[2]	Supply Current at Low Output, $I_{CC(L)}$ (mA)
A1140ELHLT-T[3]	Tape and Reel, 3000 pieces/reel	Surface Mount	–40 to 85	Low	2 to 5
~~A1140EUA-T~~[3,5]	Bulk Bag, 500 pieces/bag	Through Hole			
A1142ELHLT-T	Tape and Reel, 3000 pieces/reel	Surface Mount	–40 to 85	Low	5 to 6.9
~~A1142EUA-T~~[5]	Bulk Bag, 500 pieces/bag	Through Hole			
~~A1142LLHLT-T~~[5]	Tape and Reel, 3000 pieces/reel	Surface Mount	–40 to 150		
A1142LUA-T	Bulk Bag, 500 pieces/bag	Through Hole			
A1143ELHLT-T	Tape and Reel, 3000 pieces/reel	Surface Mount	–40 to 85	High	
A1143EUA-T	Bulk Bag, 500 pieces/bag	Through Hole			
A1143LLHLT-T	Tape and Reel, 3000 pieces/reel	Surface Mount	–40 to 150		
~~A1143LUA-T~~[4]	Bulk Bag, 500 pieces/bag	Through Hole			

[1]Contact Allegro for additional packing options.
[2]South (+) magnetic fields must be of sufficient strength.
[3]The devices listed in this footnote are available only in limited distribution. Interested customers should contact the appropriate sales person or field application engineer for more information on availability.
[4]Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.
[5]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 2, 2009. Deadline for receipt of LAST TIME BUY orders is April 30, 2010. Recommended substitutes: A1140EUA-T, contact Allegro sales; A1142LLHLT-T, use A1142ELHLT-T; and A1142EUA-T, use A1142LUA-T.

ELECTRICAL CHARACTERISTICS over the operating voltage and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage[1]	V_{CC}		3.5	–	24	V
Supply Current[2]	$I_{CC(L)}$	B>B_{OP} for A1140	2	–	5	mA
		B>B_{OP} for A1142; B<B_{RP} for A1143	5	––	6.9	mA
	$I_{CC(H)}$	B>B_{OP} for A1143 B<B_{RP} for A1140, A1142	12	––	17	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –18 V	–	–	–1.6	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	I_{CC} = $I_{CC(L)(max)}$ + 3 mA; T_A = 25°C	28	–	40	V
Supply Zener Clamp Current	$I_{ZSUPPLY}$	$V_{ZSUPPLY}$ = 28 V	–	–	$I_{CC(L)(max)}$ + 3 mA	mA
Output Slew Rate[3]	di/dt	Capacitance of the oscilloscope performing the measurement = 20 pF	–	36	–	mA/µs
Chopping Frequency	f_C		–	200	–	kHz
Power-On Time[3]	t_{on}	C_{BYPASS} = 0.01 µF	–	–	25	µs
Power-On State[5,6]	POS	t < t_{on}; V_{CC} slew rate > 25 mV/µs	–	HIGH	–	–

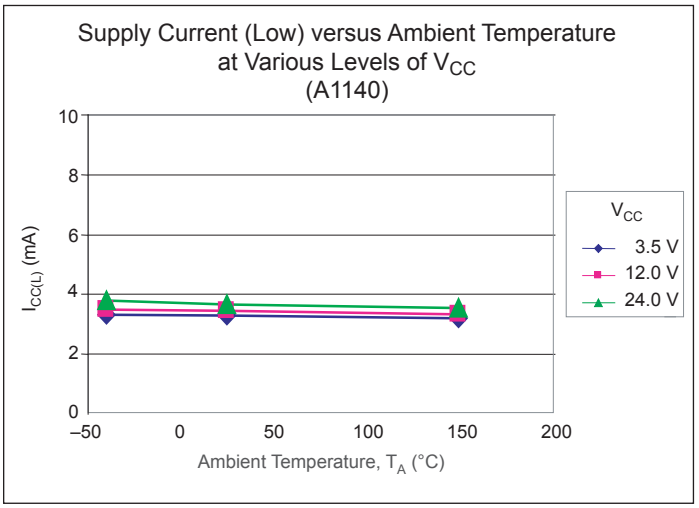
[1]V_{CC} represents the generated voltage between the VCC pin and the GND pin.
[2]Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[3]Measured without bypass capacitor between VCC and GND. Use of a bypass capacitor results in slower current change.
[3]Measured with and without bypass capacitor of 0.01 µF. Adding a larger bypass capacitor causes longer Power-On Time.
[5]POS is defined as true only with a V_{CC} slew rate of 25 mV/µs or greater. Operation with a V_{CC} slew rate less than 25 mV/µs can permanently harm device performance.
[6]POS is undefined for t > t_{on} or B_{RP} < B < B_{OP}.

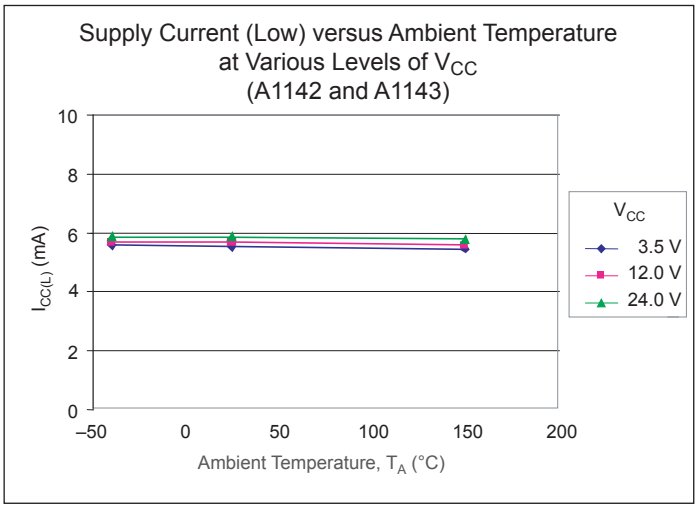
MAGNETIC CHARACTERISTICS over the operating voltage and temperature ranges, unless otherwise specified

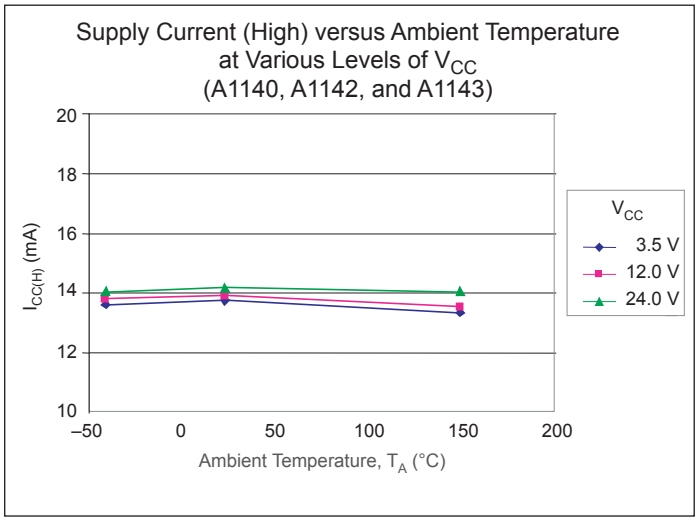
Characteristic	Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Operate Point	B_{OP}	A1140, A1142	I_{CC} = $I_{CC(L)}$	50	80	110	G
		A1143	I_{CC} = $I_{CC(H)}$				
Release Point	B_{RP}	A1140, A1142	I_{CC} = $I_{CC(H)}$	45	65	105	G
		A1143	I_{CC} = $I_{CC(L)}$				
Hysteresis	B_{HYS}	B_{HYS} = B_{OP} – B_{RP}		5	15	30	G

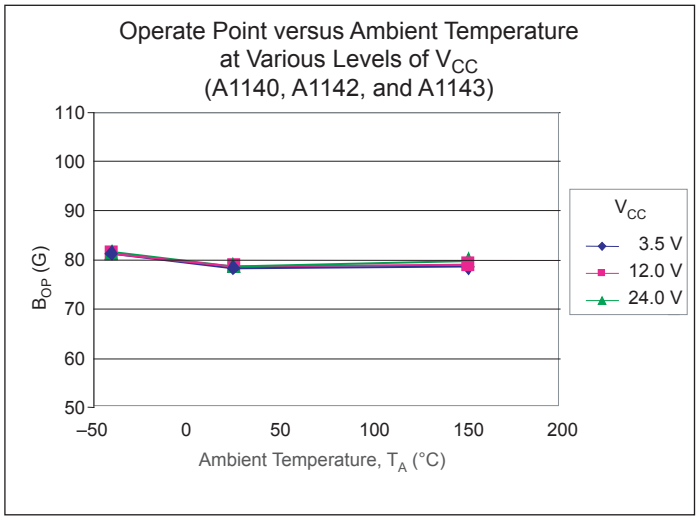
*Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.

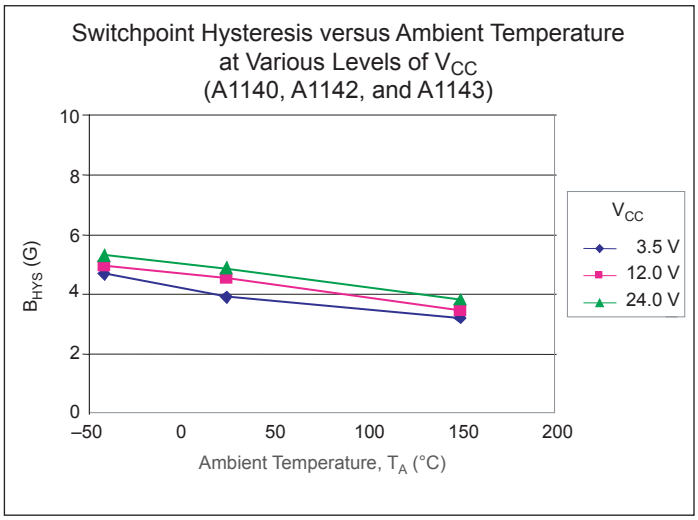
Characteristic Data









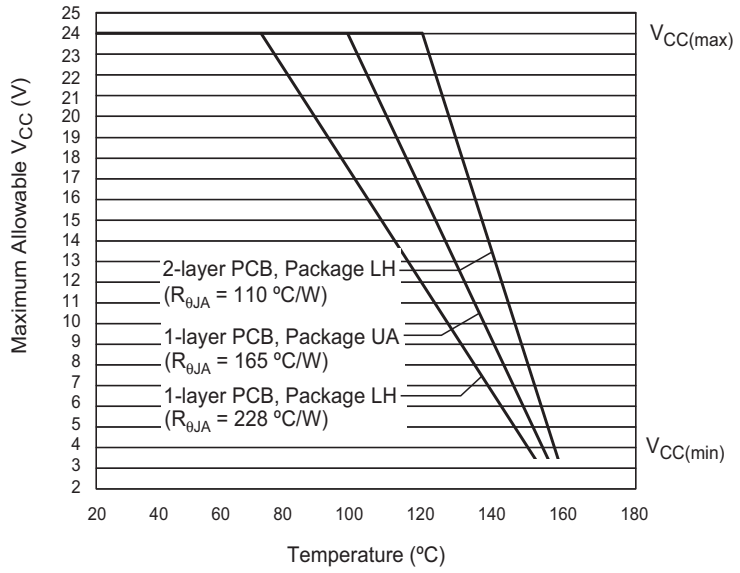


THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

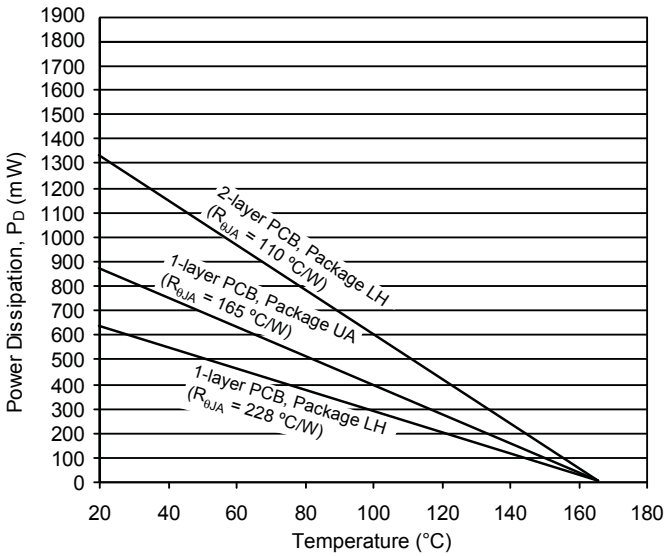
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro Web site.

Power Derating Curve



Power Dissipation versus Ambient Temperature



Functional Description

Operation

The output, I_{CC}, of the A1140 and A1142 devices switch low after the magnetic field at the Hall element exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes high. The differences between the magnetic operate and release point is called the hysteresis of the device, B_{HYS}. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The A1143 device switches with opposite polarity for similar B_{OP} and B_{RP} values, in comparison to the A1140 and A1142 (see figure 1).

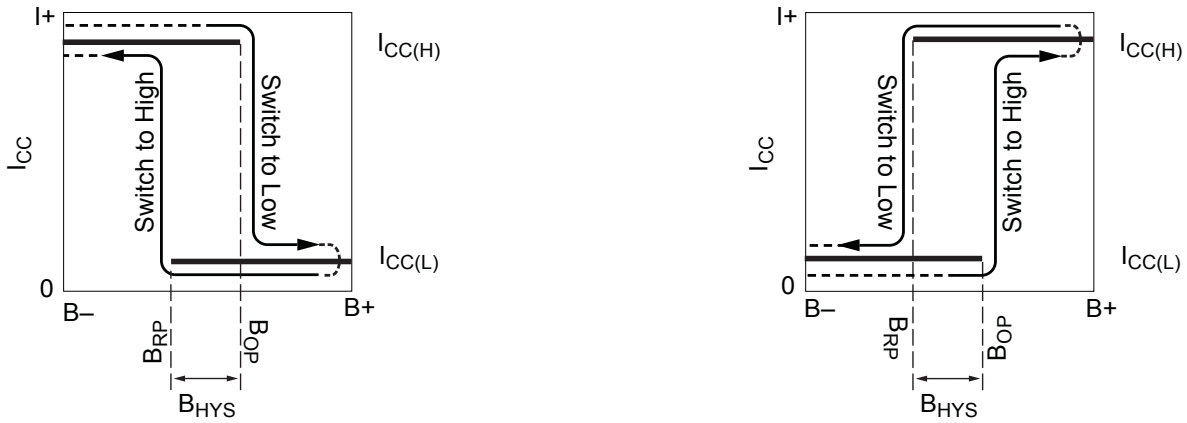


Figure 1. Alternative switching behaviors are available in the A114x device family. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This configuration is illustrated in figure 2.

The chopper stabilization technique uses a 200 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high-frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital device families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

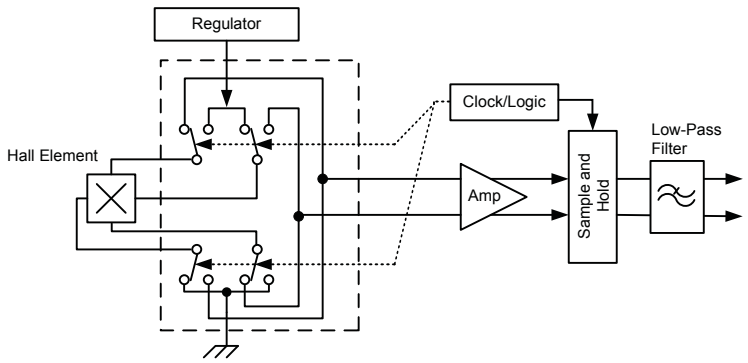


Figure 2. Chopper stabilization circuit (Dynamic Quadrature Offset Cancellation)

Application Information

Typical Application Circuit

The A114x family of devices must be protected by an external bypass capacitor, C_{BYP}, connected between the supply, VCC, and the ground, GND, of the device. C_{BYP} reduces both external noise and the noise generated by the chopper-stabilization function. As shown in figure 3, a 0.01 µF capacitor is typical.

Installation of C_{BYP} must ensure that the traces that connect it to the A114x pins are no greater than 5 mm in length.

All high-frequency interferences conducted along the supply lines are passed directly to the load through C_{BYP}, and it serves only to protect the A114x internal circuitry. As a result, the load ECU (electronic control unit) must have sufficient protection, other than C_{BYP}, installed in parallel with the A114x.

A series resistor on the supply side, RS (not shown), in combination with C_{BYP}, creates a filter for EMI pulses.

When determining the minimum V_{CC} requirement of the A114x device, the voltage drops across R_S and the ECU sense resistor, R_{SENSE}, must be taken into consideration. The typical value for R_{SENSE} is approximately 100 Ω.

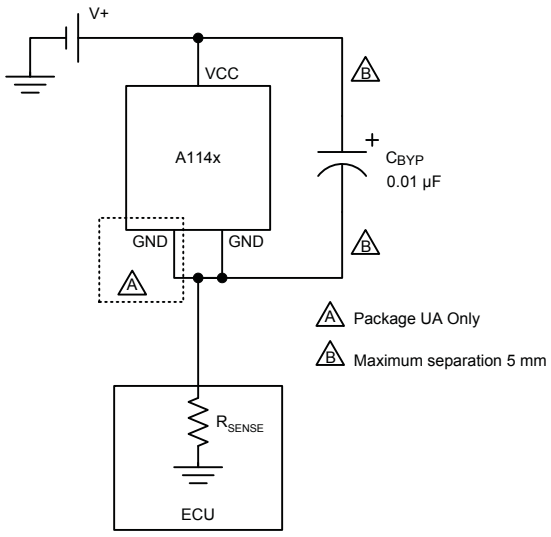


Figure 3. Typical application circuit

For additional general application information, visit the Allegro Web site at www. allegromicro.com.

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165°C/W, $T_{J(max)}$=165°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 17 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 91\ mW \div 17\ mA = 5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Device Qualification Program

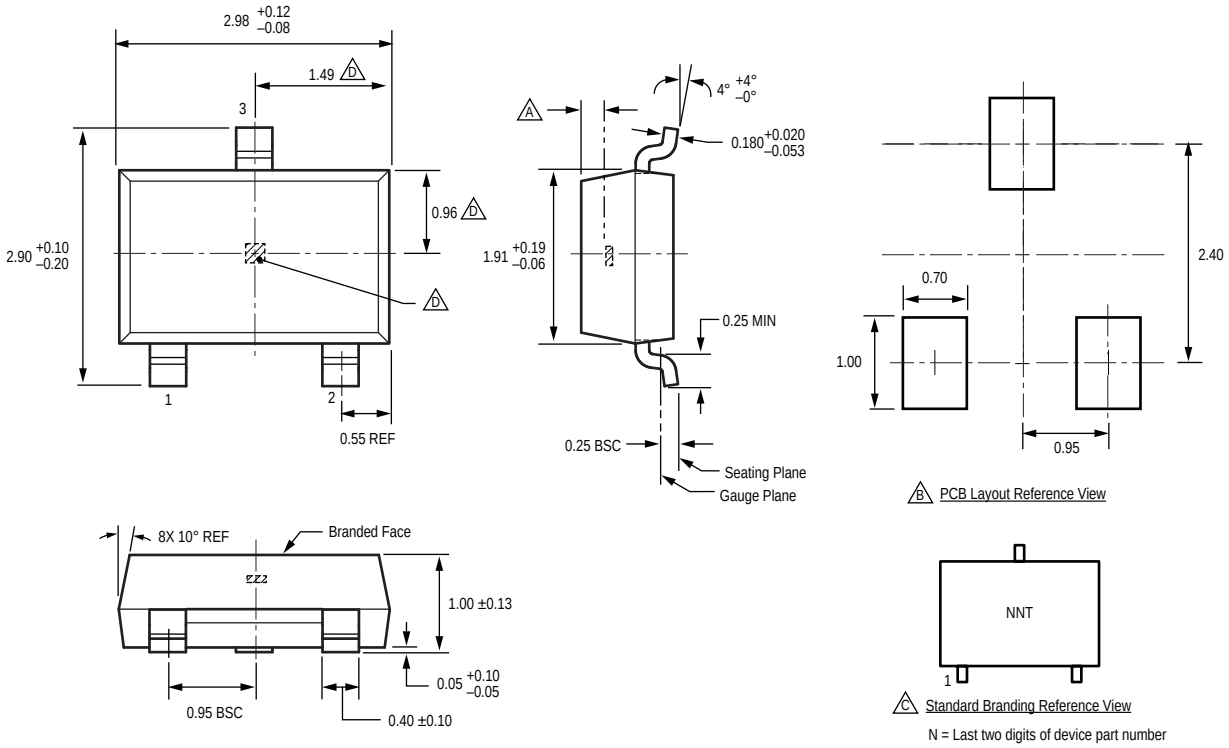
Contact Allegro for information.

EMC (Electromagnetic Compatibility) Requirements

Contact your local representative for EMC results.

Test Name	Reference Specification
ESD – Human Body Model	AEC-Q100-002
ESD – Machine Model	AEC-Q100-003
Conducted Transients	ISO 7637-2
Direct RF Injection	ISO 11452-7
Bulk Current Injection	ISO 11452-4
TEM Cell	ISO 11452-3

Package LH, 3-Pin; (SOT-23W)



N = Last two digits of device part number
T = Temperature code

For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

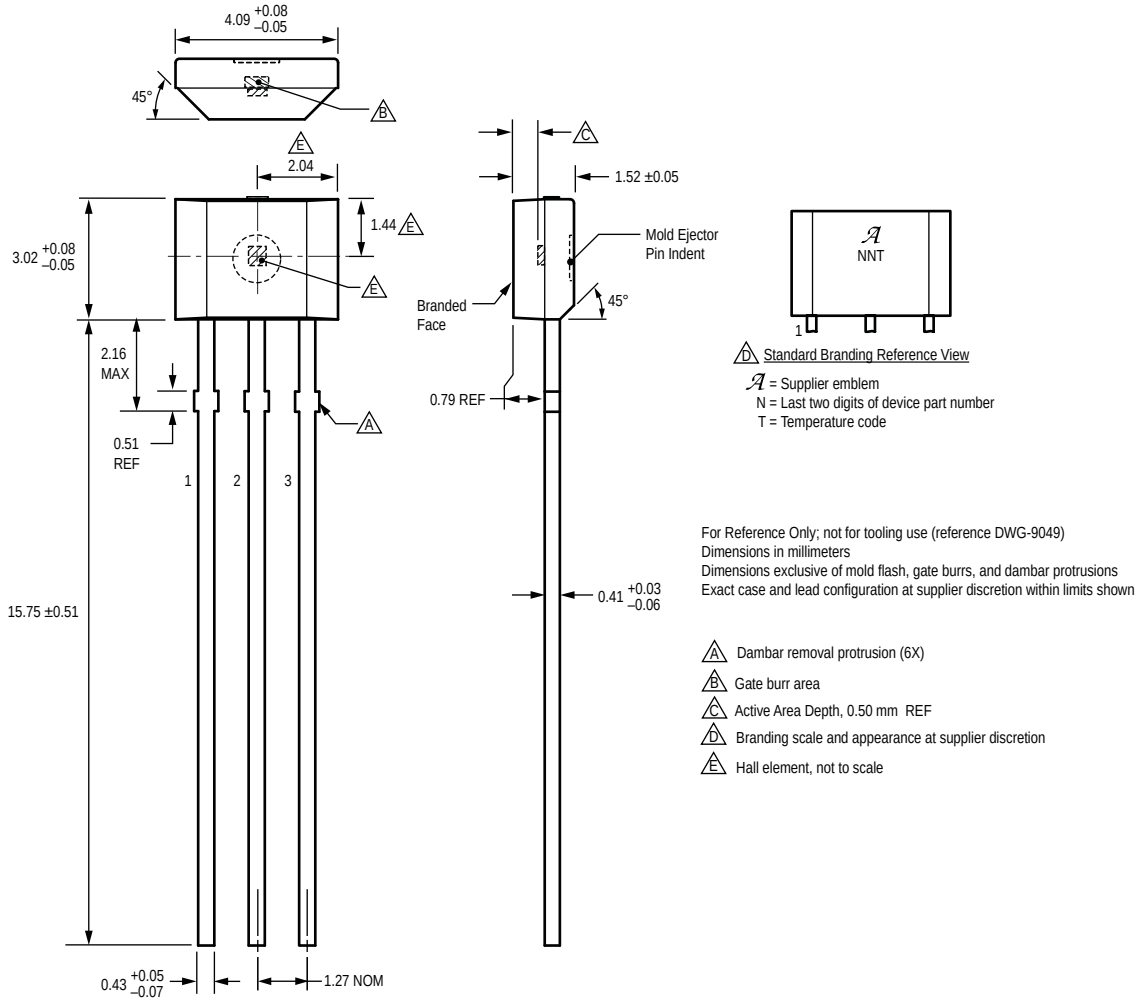
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package UA, 3-Pin SIP



The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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