National Semiconductor

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DS90C241/DS90C124

5-35MHz DC-Balanced 24-Bit FPD-Link II Serializer and Deserializer

General Description

The DS90C241/DS90C124 Chipset translates a 24-bit parallel bus into a fully transparent data/control LVDS serial stream with embedded clock information. This single serial stream simplifies transferring a 24-bit bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

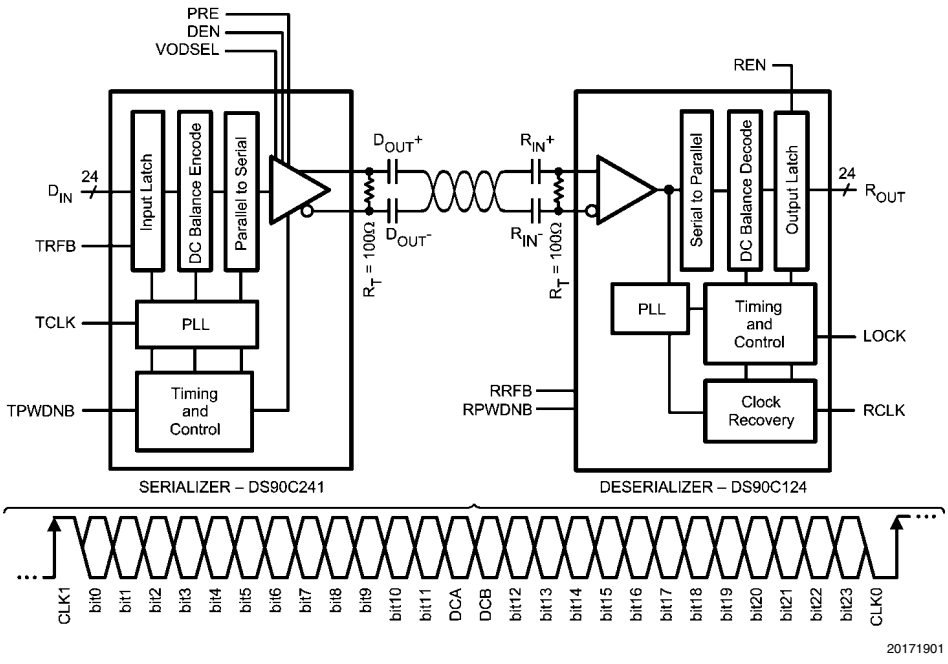
The DS90C241/DS90C124 incorporates LVDS signaling on the high-speed I/O. LVDS provides a low power and low noise environment for reliably transferring data over a serial transmission path. By optimizing the serializer output edge rate for the operating frequency range EMI is further reduced.

In addition the device features pre-emphasis to boost signals over longer distances using lossy cables. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects.

Features

- 5 MHz–35 MHz clock embedded and DC-Balancing 24:1 and 1:24 data transmissions
- User defined Pre-Emphasis driving ability through external resistor on LVDS outputs and capable to drive up to 10 meters shielded twisted-pair cable
- User selectable clock edge for parallel data on both Transmitter and Receiver
- Internal DC Balancing encode/decode – Supports AC-coupling interface with no external coding required
- Individual power-down controls for both Transmitter and Receiver
- Embedded clock CDR (clock and data recovery) on Receiver and no external source of reference clock needed
- All codes RDL (random data lock) to support live-pluggable applications
- LOCK output flag to ensure data integrity at Receiver side
- Balanced T_{SETUP}/T_{HOLD} between RCLK and RDATA on Receiver side
- PTO (progressive turn-on) LVCMOS outputs to reduce EMI and minimize SSO effects
- All LVCMOS inputs and control pins have internal pulldown
- On-chip filters for PLLs on Transmitter and Receiver
- Temperature range –40°C to +105°C
- Greater than 8 kV HBM ESD tolerant
- Meets AEC-Q100 compliance
- Power supply range 3.3V ± 10%
- 48-pin TQFP package

Block Diagram



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Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage	−0.3V to (V_{CC} +0.3V)
LVCMOS/LVTTL Output Voltage	−0.3V to (V_{CC} +0.3V)
LVDS Receiver Input Voltage	−0.3V to 3.9V
LVDS Driver Output Voltage	−0.3V to 3.9V
LVDS Output Short Circuit Duration	10 ms
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity Package De-rating:	
48L TQFP	1/θ_{JA} °C/W above +25°C
DS90C241	
θ_{JA}	45.8 (4L*); 75.4 (2L*) °C/W
θ_{JC}	21.0°C/W
DS90C124	
θ_{JA}	45.4 (4L*); 75.0 (2L*)°C/W
θ_{JC}	21.1°C/W
	**JEDEC*
ESD Rating (HBM)	≥±8 kV
ESD Rating (ISO10605)	DS90C241 meets ISO 10605
R_D = 2 kΩ, C_S = 330 pF	
Contact Discharge (D_{OUT+}, D_{OUT-})	±8 kV
Air Discharge (D_{OUT+}, D_{OUT-})	±25 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
Clock Rate	5		35	MHz
Supply Noise			±100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS							
V_{IH}	High Level Voltage		**Tx:** DIN[23:0], TCLK, TPWDNB, DEN, TRFB, DCAOFF, DCBOFF, VODSEL **Rx:** RPWDNB, RRFB, REN	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA (*Note 9*)			−0.8	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V	**Tx:** DIN[23:0], TCLK, TPWDNB, DEN, TRFB, DCAOFF, DCBOFF, VODSEL	−10	±5	+10	µA
			Rx: RPWDNB, RRFB, REN	−20	±5	+20	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	**Rx:** ROUT[23:0], RCLK, LOCK	2.3	3.0	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA		GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (*Note 9*)		−40	−70	−110	mA
I_{OZ}	TRI-STATE® Output Current	RPWDNB, REN = 0V V_{OUT} = 0V or 2.4V	**Rx:** ROUT[23:0], RCLK, LOCK	−30	±0.4	+30	µA
LVDS DC SPECIFICATIONS							
V_{TH}	Differential Threshold High Voltage	V_{CM} = +1.2V	**Rx:** R_{IN+}, R_{IN-}			+50	mV
V_{TL}	Differential Threshold Low Voltage			−50			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V or 0V				±200	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±200	µA

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage (D_{OUT+})–(D_{OUT-})	R_L = 100Ω, w/o Pre-emphasis VODSEL = L *(Figure 10)*	**Tx:** D_{OUT+}, D_{OUT-}	250	400	600	mV
		R_L = 100Ω, w/o Pre-emphasis VODSEL = H *(Figure 10)*		450	750	1200	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω, w/o Pre-emphasis			10	50	mV
V_{OS}	Offset Voltage	R_L = 100Ω, w/o Pre-emphasis		1.00	1.25	1.50	V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω, w/o Pre-emphasis			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT = 0V, DIN = H, TPWDNB, DEN = 2.4V, VODSEL = L		–2		–8	mA
		DOUT = 0V, DIN = H, TPWDNB, DEN = 2.4V, VODSEL = H		–7		–13	mA
I_{OZ}	TRI-STATE Output Current	TPWDNB, DEN = 0V, DOUT = 0V or 2.4V		–15	±1	+15	µA
SER/DES SUPPLY CURRENT (DVDD*, PVDD* and AVDD* pins) **Digital, PLL, and Analog VDDs*							
I_{CCT}	Serializer (Tx) Total Supply Current (includes load current)	R_L = 100Ω R_{PRE} = OFF VODSEL = H/L Checker-board pattern *(Figure 1)*	f = 35 MHz		40	65	mA
		R_L = 100Ω R_{PRE} = 6 kΩ VODSEL = H/L Checker-board pattern *(Figure 1)*	f = 35 MHz		45	70	mA
	Serializer (Tx) Total Supply Current (includes load current)	R_L = 100Ω R_{PRE} = OFF VODSEL = H/L	f = 35 MHz		40	65	mA
		R_L = 100Ω R_{PRE} = 6 kΩ VODSEL = H/L Random pattern	f = 35 MHz		45	70	mA
I_{CCTZ}	Serializer (Tx) Supply Current Power-down	TPWDNB = 0V (All other LVCMOS Inputs = 0V)				800	µA
I_{CCR}	Deserializer (Rx) Total Supply Current (includes load current)	C_L = 8 pF LVCMOS Output Checker-board pattern *(Figure 2)*	f = 35 MHz			85	mA
	Deserializer (Rx) Total Supply Current (includes load current)	C_L = 8 pF LVCMOS Output Random pattern	f = 35 MHz			80	mA
I_{CCRZ}	Deserializer (Rx) Supply Current Power-down	RPWDNB = 0V (All other LVCMOS Inputs = 0V, R_{IN+}/ R_{IN-} = 0V)				50	µA

Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	*(Figure 5)*	28.6	T	200	ns
t_{TCIH}	Transmit Clock High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	TCLK Input Transition Time	*(Figure 4)*		3	6	ns
t_{JIT}	TCLK Input Jitter	(*Note 10*)			33	ps (RMS)

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	LVDS Low-to-High Transition Time	R_L = 100Ω, *(Figure 3)* C_L = 10 pF to GND VODSEL = L			0.6	ns
t_{LHLT}	LVDS High-to-Low Transition Time				0.6	ns
t_{DIS}	DIN (23:0) Setup to TCLK	R_L = 100Ω, C_L = 10 pF to GND (*Note 9*)	5			ns
t_{DIH}	DIN (23:0) Hold from TCLK		5			ns
t_{HZD}	DOUT ± HIGH to TRI-STATE Delay	R_L = 100Ω, C_L = 10 pF to GND *(Figure 6)* (*Note 5*)			15	ns
t_{LZD}	DOUT ± LOW to TRI-STATE Delay				15	ns
t_{ZHD}	DOUT ± TRI-STATE to HIGH Delay				200	ns
t_{ZLD}	DOUT ± TRI-STATE to LOW Delay				200	ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω, *(Figure 7)*			10	ms
t_{SD}	Serializer Delay	R_L = 100Ω, *(Figure 8)* VODSEL = L, TRFB = H		3.5T + 2.85	3.5T + 10	ns
		R_L = 100Ω, *(Figure 8)* VODSEL = L, TRFB = L		3.5T + 2.85	3.5T + 10	ns
TxOUT_E_O	TxOUT_Eye_Opening (respect to ideal)	5–35 MHz *(Figure 9)* (*Note 9*, *Note 10*, *Note 14*)	0.75			UI (*Note 11*)

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	**R**eceiver out **C**lock **P**eriod	$t_{RCP} = t_{TCP}$ (*Note 9*)	RCLK	28.6		200	ns
t_{RDC}	**R**CLK **D**uty **C**ycle		RCLK	45	50	55	%
t_{CLH}	LV**C**MOS **L**ow-to-**H**igh Transition Time	C_L = 8 pF (lumped load) *(Figure 11)* (*Note 9*)	ROUT [23:0], LOCK, RCLK		2.5	3.5	ns
t_{CHL}	LV**C**MOS **H**igh-to-**L**ow Transition Time				2.5	3.5	ns
t_{ROS}	**RO**UT (7:0) **S**etup Data to RCLK (Group 1)	*(Figure 15)*	ROUT [7:0]	(0.40)* t_{RCP}	(29/56)*t_{RCP}		ns
t_{ROH}	**RO**UT (7:0) **H**old Data to RCLK (Group 1)			(0.40)* t_{RCP}	(27/56)*t_{RCP}		ns
t_{ROS}	**RO**UT (15:8) **S**etup Data to RCLK (Group 2)	*(Figure 15)*	ROUT [15:8], LOCK	(0.40)* t_{RCP}	0.5*t_{RCP}		ns
t_{ROH}	**RO**UT (15:8) **H**old Data to RCLK (Group 2)			(0.40)* t_{RCP}	0.5*t_{RCP}		ns

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{ROS}	**RO**UT (23:16) **S**etup Data to RCLK (Group 3)	*(Figure 15)*	ROUT [23:16]	(0.40)* t_{RCP}	(27/56)*t_{RCP}		ns
t_{ROH}	**RO**UT (23:16) **H**old Data to RCLK (Group 3)			(0.40)* t_{RCP}	(29/56)*t_{RCP}		ns
t_{HZR}	**H**IGH to TRI-STATE Delay	*(Figure 13)*	ROUT [23:0], RCLK, LOCK		3	10	ns
t_{LZR}	**L**OW to TRI-STATE Delay				3	10	ns
t_{ZHR}	TRI-STATE to **H**IGH Delay				3	10	ns
t_{ZLR}	TRI-STATE to **L**OW Delay				3	10	ns
t_{DD}	**D**eserializer **D**elay	*(Figure 12)*	RCLK		[4+(3/56)]T +5.9	[4+(3/56)]T +14	ns
t_{DRDL}	Deserializer PLL Lock Time from Powerdown	*(Figure 14)* (*Note 8*, *Note 9*)	5 MHz		5	50	ms
			35 MHz		5	50	ms
RxIN_TOL_L	**R**eceiver **IN**put **TOL**erance **L**eft,	*(Figure 16)* (*Note 7*, *Note 9*, *Note 11*)	5 MHz–35 MHz			0.25	UI
RxIN_TOL_R	**R**eceiver **IN**put **TOL**erance **R**ight,	*(Figure 16)* (*Note 7*, *Note 9*, *Note 11*)	5 MHz–35 MHz			0.25	UI

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{CC} = 3.3V, Ta = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 4: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 5: When the Serializer output is tri-stated, the Deserializer will lose PLL lock. Resynchronization MUST occur before data transfer.

Note 6: t_{DRDL} is the time required by the deserializer to obtain lock when exiting powerdown mode. t_{DRDL} is specified with an external synchronization pattern.

Note 7: RxIN_TOL is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. It is a measurement in reference with the ideal bit position, please see National's AN-1217 for detail.

Note 8: The Deserializer PLL lock time (t_{DRDL}) may vary depending on input data patterns and the number of transitions within the pattern.

Note 9: Specification is guaranteed by characterization and is not tested in production.

Note 10: t_{JIT} (@BER of 10e-9) specifies the allowable jitter on TCLK. t_{JIT} not included in TxOUT_E_O parameter.

Note 11: UI – Unit Interval, equivalent to one ideal serialized data bit width. The UI scales with frequency.

Note 12: Figures 1, 2, 8, 12, 14 show a falling edge data strobe (TCLK IN/RCLK OUT).

Note 13: Figures 5, 15 show a rising edge data strobe (TCLK IN/RCLK OUT).

Note 14: TxOUT_E_O is affected by pre-emphasis value.

AC Timing Diagrams and Test Circuits

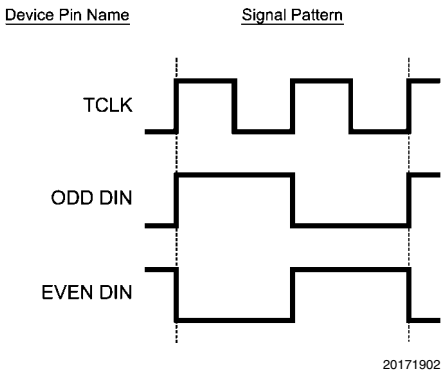


FIGURE 1. Serializer Input Checker-board Pattern

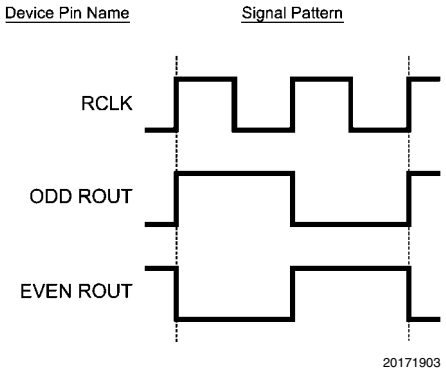


FIGURE 2. Deserializer Output Checker-board Pattern

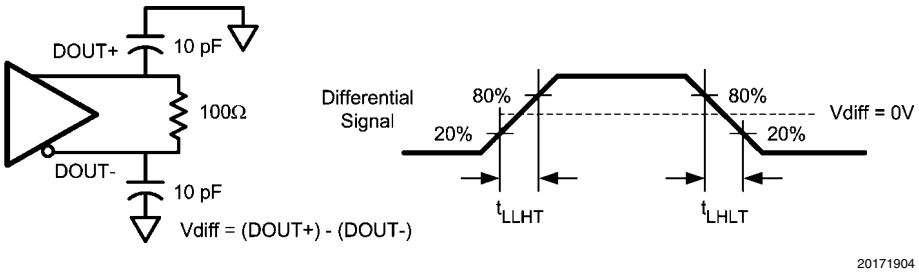


FIGURE 3. Serializer LVDS Output Load and Transition Times

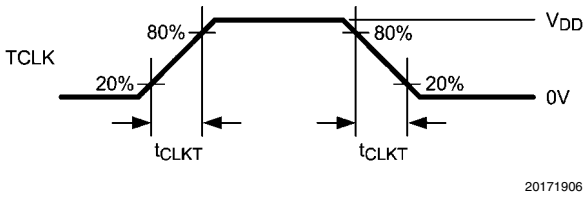


FIGURE 4. Serializer Input Clock Transition Times

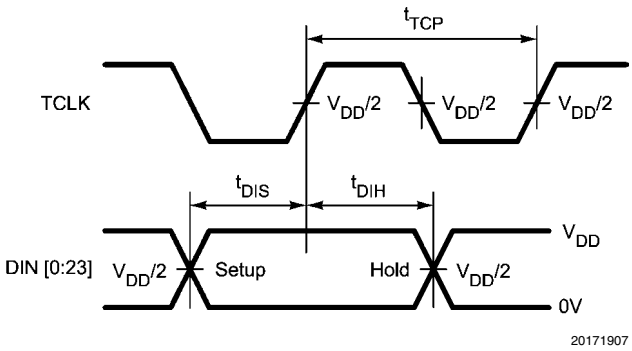


FIGURE 5. Serializer Setup/Hold Times

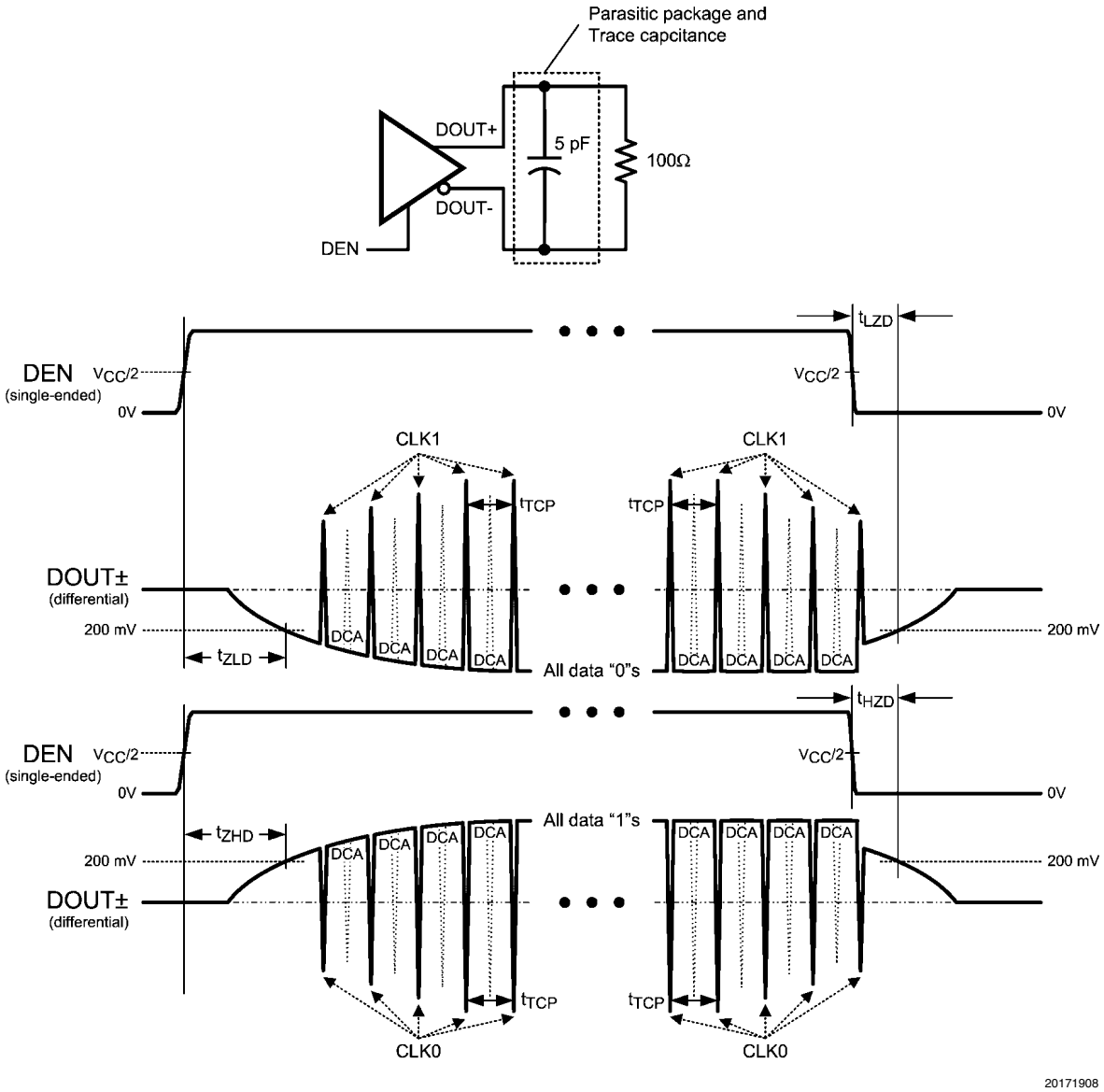


FIGURE 6. Serializer TRI-STATE Test Circuit and Delay

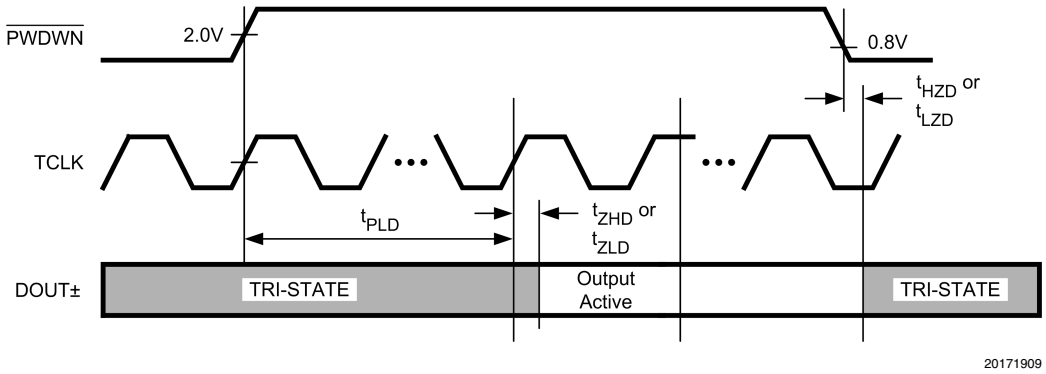


FIGURE 7. Serializer PLL Lock Time, and TPWDNB TRI-STATE Delays

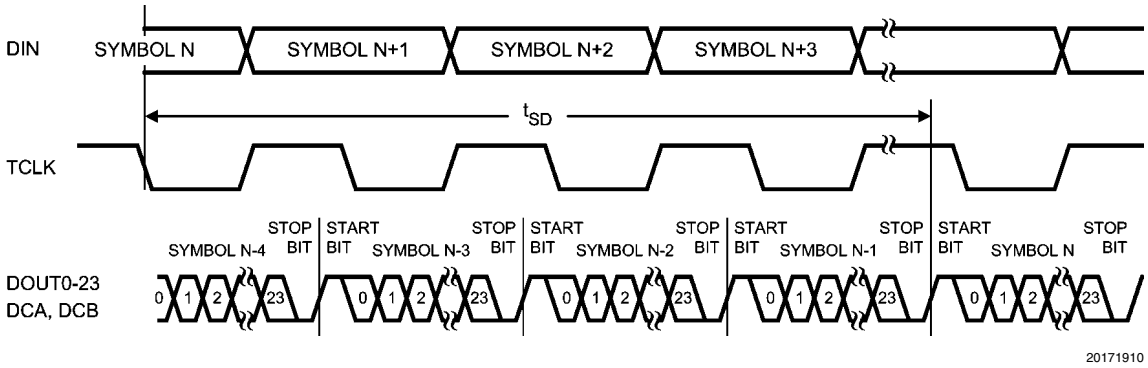


FIGURE 8. Serializer Delay

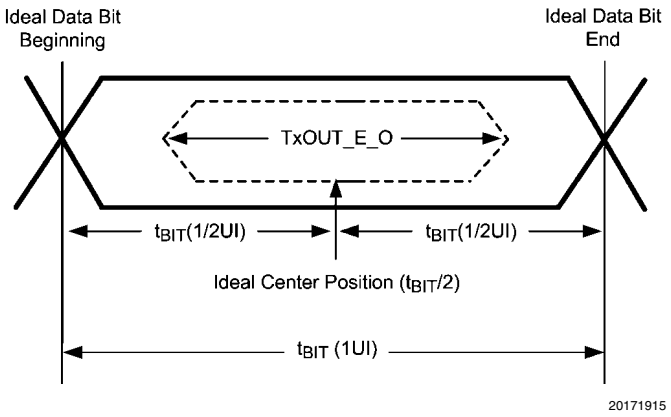
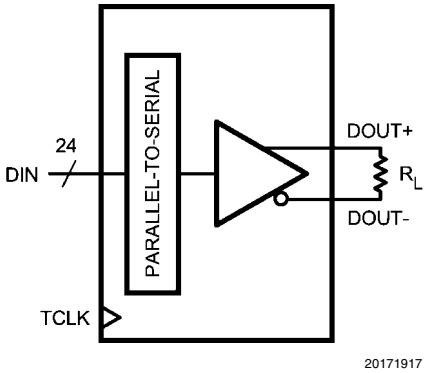


FIGURE 9. Transmitter Output Eye Opening (TxOUT_E_O)



$VOD = (D_{OUT+}) - (D_{OUT-})$

Differential output signal is shown as $(D_{OUT+}) - (D_{OUT-})$, device in Data Transfer mode.

FIGURE 10. Serializer VOD Diagram

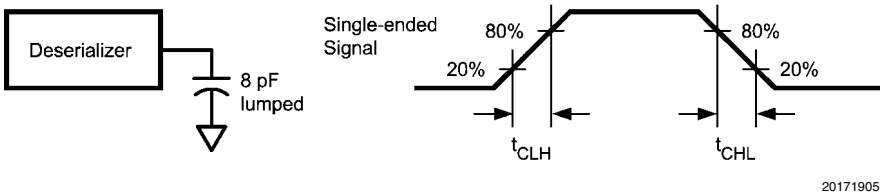


FIGURE 11. Deserializer LVCMOS/LVTTL Output Load and Transition Times

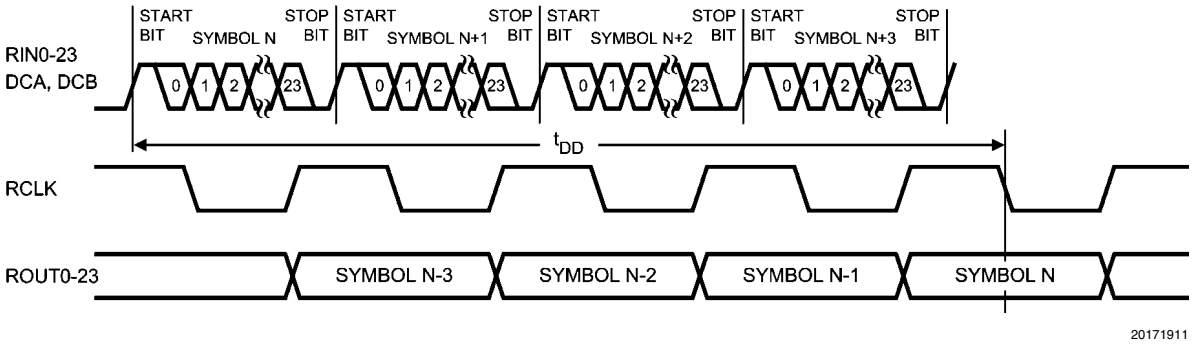
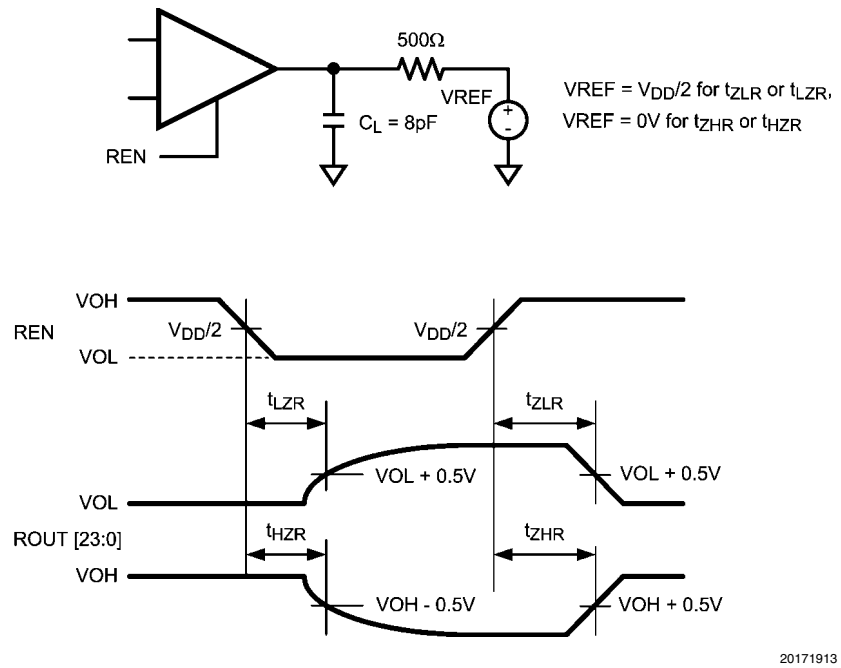


FIGURE 12. Deserializer Delay



Note: C_L includes instrumentation and fixture capacitance within 6 cm of ROUT[23:0]

FIGURE 13. Deserializer TRI-STATE Test Circuit and Timing

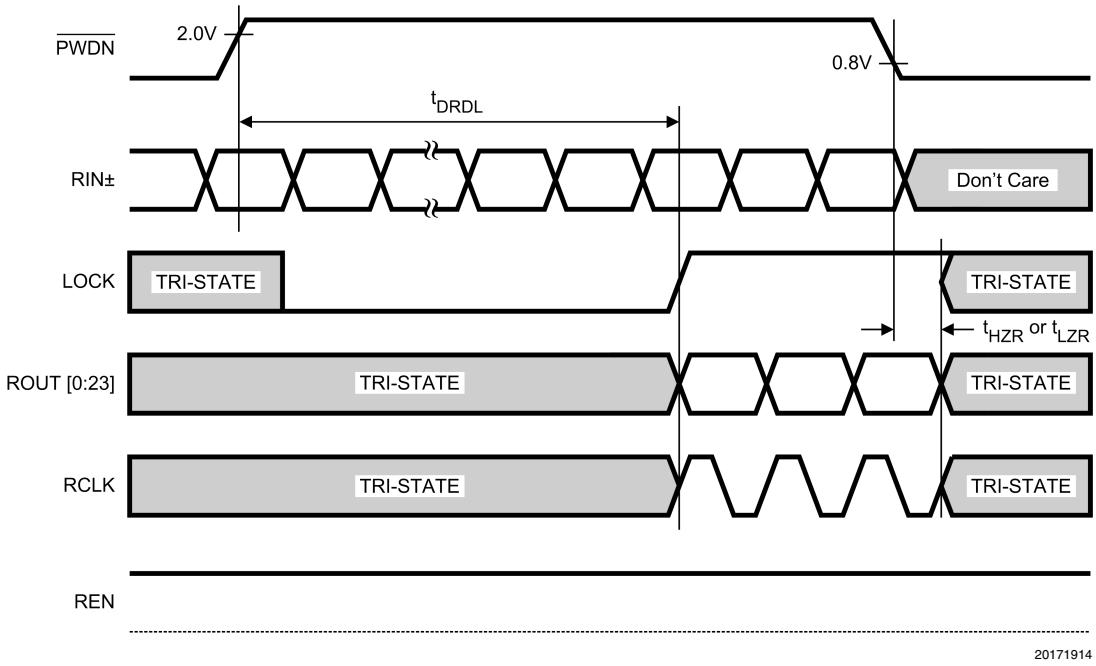


FIGURE 14. Deserializer PLL Lock Times and RPWDNB TRI-STATE Delay

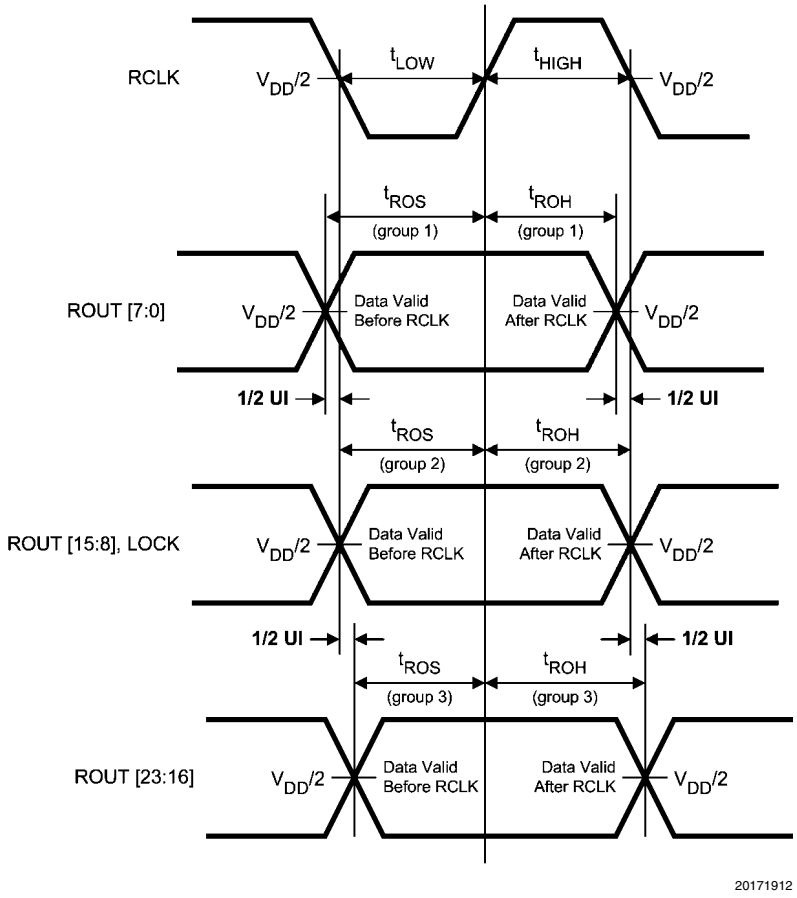
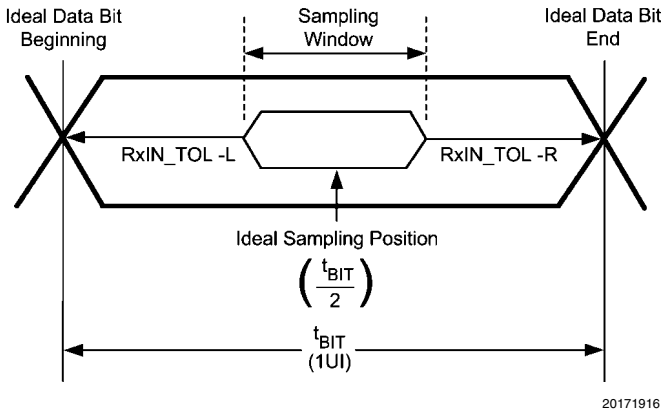


FIGURE 15. Deserializer Setup and Hold Times



RxIN_TOL_L is the ideal noise margin on the left of the figure, with respect to ideal.
RxIN_TOL_R is the ideal noise margin on the right of the figure, with respect to ideal.

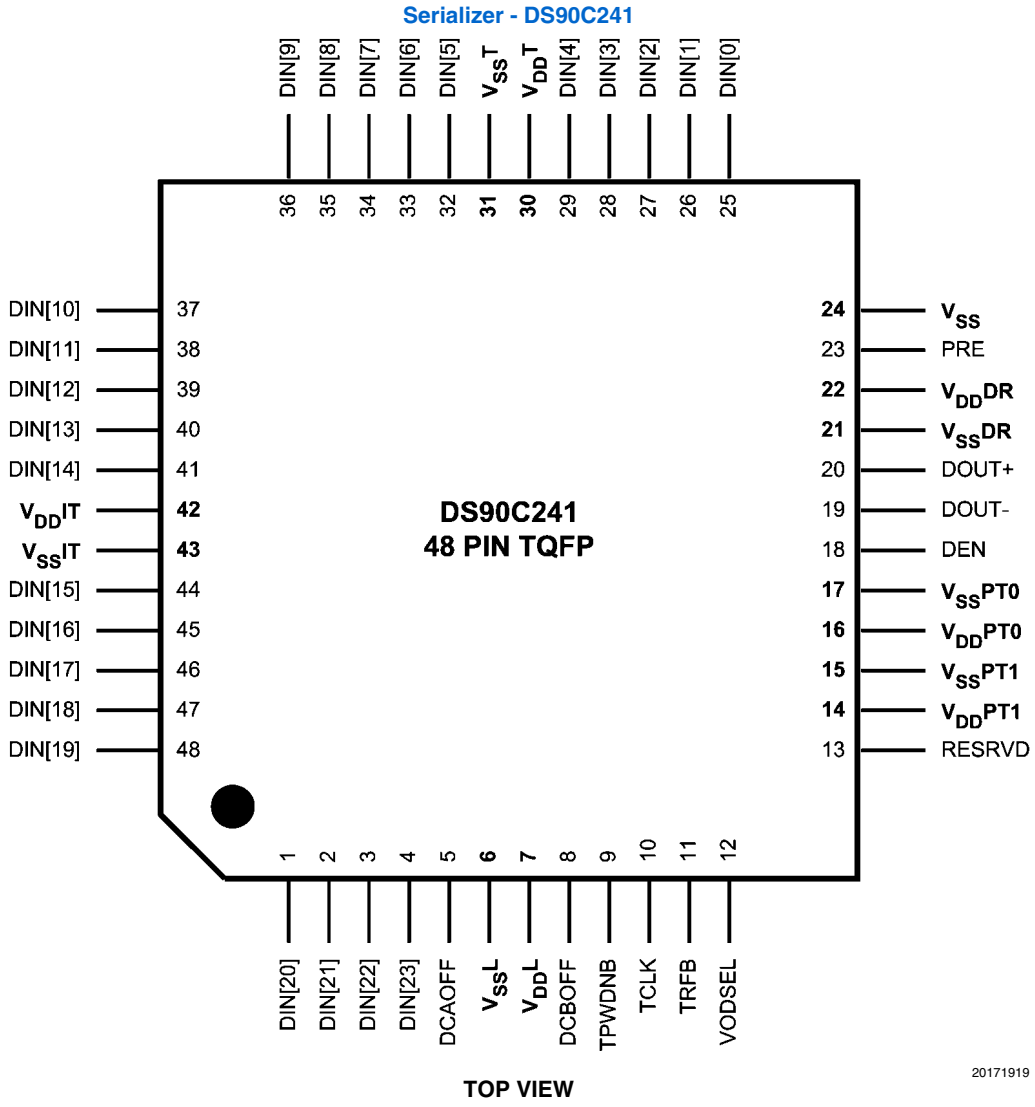
FIGURE 16. Receiver Input Tolerance (RxIN_TOL) and Sampling Window

DS90C241 Serializer Pin Descriptions

Pin #	Pin Name	I/O	Description
LVCMOS PARALLEL INTERFACE PINS			
4-1, 48-44, 41-32, 29-25	DIN[23:0]	LVCMOS_I	Transmitter Parallel Interface Data Input Pins. Tie LOW if unused, do not float.
10	TCLK	LVCMOS_I	Transmitter Parallel Interface Clock Input Pin. Strobe edge set by TRFB configuration pin.
CONTROL AND CONFIGURATION PINS			
9	TPWDNB	LVCMOS_I	Transmitter Power Down Bar TPWDNB = H; Transmitter is Enabled and ON TPWDNB = L; Transmitter is in power down mode (Sleep), LVDS Driver D_{OUT} (+/-) Outputs are in TRI-STATE stand-by mode, PLL is shutdown to minimize power consumption.
18	DEN	LVCMOS_I	Transmitter Data Enable DEN = H; LVDS Driver Outputs are Enabled (ON). DEN = L; LVDS Driver Outputs are Disabled (OFF), Transmitter LVDS Driver D_{OUT} (+/-) Outputs are in TRI-STATE, PLL still operational and locked to TCLK.
23	PRE	LVCMOS_I	Pre-emphasis Level Select PRE = NC (No Connect); Pre-emphasis is Disabled (OFF). Pre-emphasis is active when input is tied to VSS through external resistor R_{PRE}. Resistor value determines pre-emphasis level. Recommended value $R_{PRE} \geq 3\ k\Omega$; $I_{max} = [(1.2/R)*20]$, $R_{min} = 3\ k\Omega$
11	TRFB	LVCMOS_I	Transmitter Clock Edge Select Pin TRFB = H; Parallel Interface Data is strobed on the Rising Clock Edge. TRFB = L; Parallel Interface Data is strobed on the Falling Clock Edge
12	VODSEL	LVCMOS_I	VOD Level Select VODSEL = L; LVDS Driver Output is ≈±400 mV (R_L = 100Ω) VODSEL = H; LVDS Driver Output is ≈±750 mV (R_L = 100Ω) For normal applications, set this pin LOW. For long cable applications where a larger VOD is required, set this pin HIGH.
5	DCAOFF	LVCMOS_I	Reserved. This pin **MUST** be tied LOW.
8	DCBOFF	LVCMOS_I	Reserved. This pin **MUST** be tied LOW.
13	RESRVD	LVCMOS_I	Reserved. This pin **MUST** be tied LOW.
LVDS SERIAL INTERFACE PINS			
20	DOUT+	LVDS_O	Transmitter LVDS True **(+)** Output. This output is intended to be loaded with a 100Ω load to the D_{OUT+} pin. The interconnect should be AC Coupled to this pin with a 100 nF capacitor.
19	DOUT–	LVDS_O	Transmitter LVDS Inverted **(-)** Output This output is intended to be loaded with a 100Ω load to the D_{OUT-} pin. The interconnect should be AC Coupled to this pin with a 100 nF capacitor.
POWER / GROUND PINS			
22	VDDDR	VDD	Analog Voltage Supply, LVDS Output Power
21	VSSDR	GND	Analog Ground, LVDS Output Ground
16	VDDPT0	VDD	Analog Voltage supply, VCO Power
17	VSSPT0	GND	Analog Ground, VCO Ground
14	VDDPT1	VDD	Analog Voltage supply, PLL Power
15	VSSPT1	GND	Analog Ground, PLL Ground
30	VDDT	VDD	Digital Voltage supply, Tx Serializer Power
31	VSST	GND	Digital Ground, Tx Serializer Ground
7	VDDL	VDD	Digital Voltage supply, Tx Logic Power
6	VSSL	GND	Digital Ground, Tx Logic Ground
42	VDDIT	VDD	Digital Voltage supply, Tx Input Power

Pin #	Pin Name	I/O	Description
43	VSSIT	GND	Digital Ground, Tx Input Ground
24	VSS	GND	ESD Ground

DS90C241 Pin Diagram

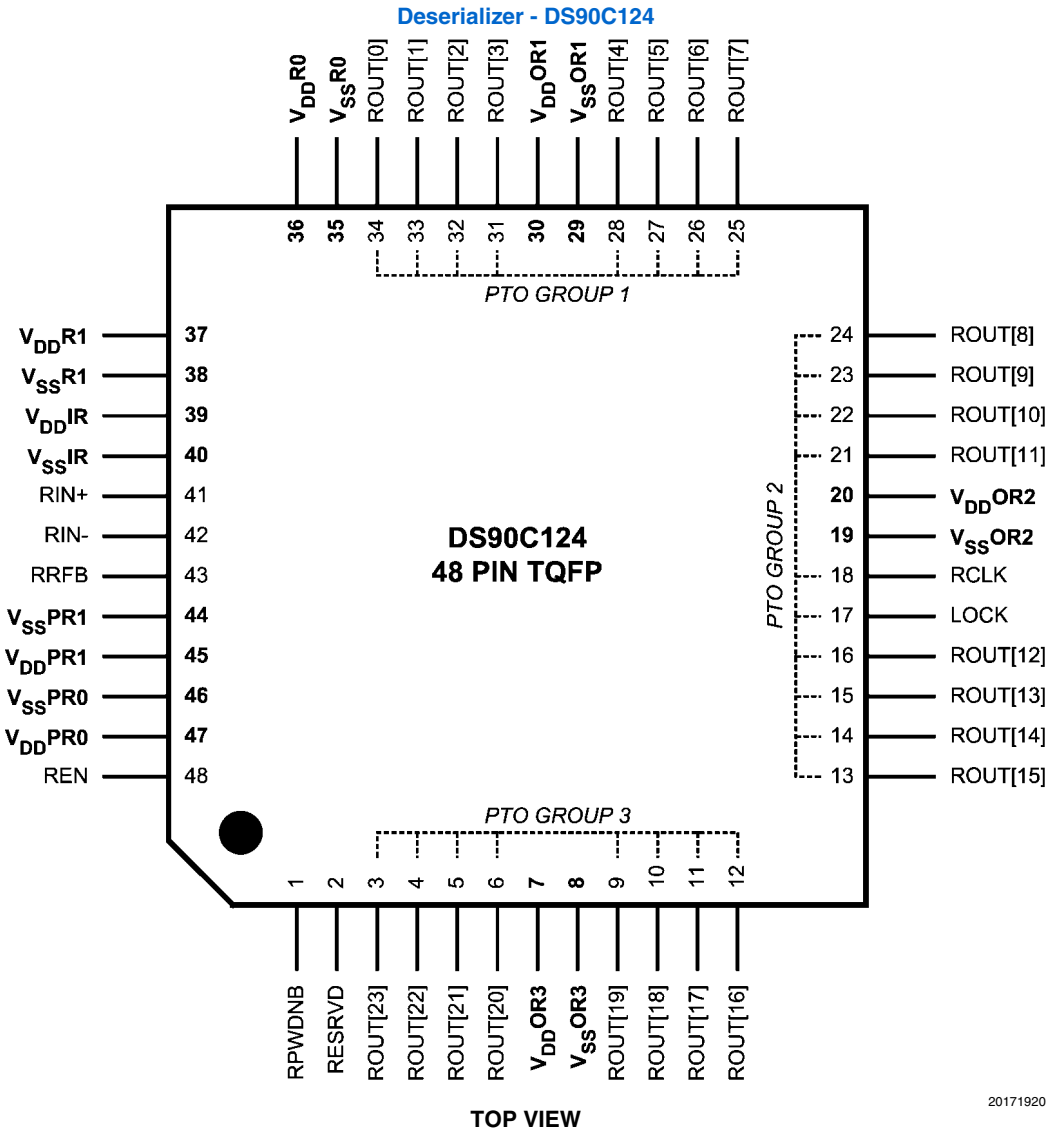


TOP VIEW

DS90C124 Deserializer Pin Descriptions

Pin #	Pin Name	I/O	Description
LVCMOS PARALLEL INTERFACE PINS			
25-28, 31-34	ROUT[7:0]	LVCMOS_O	Receiver LVCMOS level Outputs – Group 1
13-16, 21-24	ROUT[15:8]	LVCMOS_O	Receiver LVCMOS level Outputs – Group 2
3-6, 9-12	ROUT[23:16]	LVCMOS_O	Receiver LVCMOS level Outputs – Group 3
18	RCLK	LVCMOS_O	Parallel Interface Clock Output Pin. Strobe edge set by RRFB configuration pin.
CONTROL AND CONFIGURATION PINS			
43	RRFB	LVCMOS_I	Receiver Clock Edge Select Pin RRFB = H; R_{OUT} LVCMOS Outputs strobed on the Rising Clock Edge. RRFB = L; R_{OUT} LVCMOS Outputs strobed on the Falling Clock Edge.
48	REN	LVCMOS_I	Receiver Data Enable REN = H; R_{OUT}[23-0] and RCLK are Enabled (ON). REN = L; R_{OUT}[23-0] and RCLK are Disabled (OFF), Receiver R_{OUT}[23-0] and RCLK Outputs are in TRI-STATE, PLL still operational and locked to TCLK.
1	RPWDNB	LVCMOS_I	Receiver Power Down Bar RPWDNB = H; Receiver is Enabled and ON RPWDNB = L; Receiver is in power down mode (Sleep), R_{OUT}[23-0], RCLK, and LOCK are in TRI-STATE stand-by mode, PLL is shutdown to minimize power consumption.
17	LOCK	LVCMOS_O	LOCK indicates the status of the receiver PLL LOCK = H; receiver PLL is locked LOCK = L; receiver PLL is unlocked, R_{OUT}[23-0] and RCLK are TRI-STATED
2	RESRVD	LVCMOS_I	Reserved. This pin **MUST** be tied LOW.
LVDS SERIAL INTERFACE PINS			
41	RIN+	LVDS_I	Receiver LVDS True **(+)** Input This input is intended to be terminated with a 100Ω load to the R_{IN+} pin. The interconnect should be AC Coupled to this pin with a 100 nF capacitor.
42	RIN–	LVDS_I	Receiver LVDS Inverted **(–)** Input This input is intended to be terminated with a 100Ω load to the R_{IN-} pin. The interconnect should be AC Coupled to this pin with a 100 nF capacitor.
POWER / GROUND PINS			
39	VDDIR	VDD	Analog LVDS Voltage supply, Power
40	VSSIR	GND	Analog LVDS Ground
47	VDDPR0	VDD	Analog Voltage supply, PLL Power
46	VSSPR0	GND	Analog Ground, PLL Ground
45	VDDPR1	VDD	Analog Voltage supply, PLL VCO Power
44	VSSPR1	GND	Analog Ground, PLL VCO Ground
37	VDDR1	VDD	Digital Voltage supply, Logic Power
38	VSSR1	GND	Digital Ground, Logic Ground
36	VDDR0	VDD	Digital Voltage supply, Logic Power
35	VSSR0	GND	Digital Ground, Logic Ground
30	VDDOR1	VDD	Digital Voltage supply, LVCMOS Output Power
29	VSSOR1	GND	Digital Ground, LVCMOS Output Ground
20	VDDOR2	VDD	Digital Voltage supply, LVCMOS Output Power
19	VSSOR2	GND	Digital Ground, LVCMOS Output Ground
7	VDDOR3	VDD	Digital Voltage supply, LVCMOS Output Power
8	VSSOR3	GND	Digital Ground, LVCMOS Output Ground

DS90C124 Pin Diagram



TOP VIEW

Functional Description

The DS90C241 Serializer and DS90C124 Deserializer chipset is an easy-to-use transmitter and receiver pair that sends 24-bits of parallel LVCMOS data over a single serial LVDS link from 120 Mbps to 840 Mbps throughput. The DS90C241 transforms a 24-bit wide parallel LVCMOS data into a single high speed LVDS serial data stream with embedded clock and scrambles / DC Balances the data to enhance signal quality to support AC coupling. The DS90C124 receives the LVDS serial data stream and converts it back into a 24-bit wide parallel data and recovered clock. The 24-bit Serializer/Deserializer chipset is designed to transmit data up to 10 meters over shielded twisted pair (STP) at clock speeds from 5 MHz to 35 MHz.

The Deserializer can attain lock to a data stream without the use of a separate reference clock source; greatly simplifying system complexity and overall cost. The Deserializer synchronizes to the Serializer regardless of data pattern, delivering true automatic “plug and lock” performance. It will lock to the incoming serial stream without the need of special training patterns or sync characters. The Deserializer recovers the clock and data by extracting the embedded clock information and validating data integrity from the incoming data stream and then deserializes the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the LOCK output high when lock occurs. Each has a power down control to enable efficient operation in various applications.

INITIALIZATION AND LOCKING MECHANISM

Initialization of the DS90C241 and DS90C124 must be established before each device sends or receives data. Initialization refers to synchronizing the Serializer’s and Deserializer’s PLL’s together. After the Serializers locks to the input clock source, the Deserializer synchronizes to the Serializers as the second and final initialization step.

Step 1: When V_{CC} is applied to both Serializer and/or Deserializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.2V) the PLL in Serializer begins locking to a clock input. For the Serializer, the local clock is the transmit clock, TCLK. The Serializer outputs are held in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer block is now ready to send data patterns. The Deserializer output will remain in TRI-STATE while its PLL locks to the embedded clock information in serial data stream. Also, the Deserializer LOCK output will remain low until its PLL locks to incoming data and sync-pattern on the RIN± pins.

Step 2: The Deserializer PLL acquires lock to a data stream without requiring the Serializer to send special patterns. The Serializer that is generating the stream to the Deserializer will automatically send random (non-repetitive) data patterns during this step of the Initialization State. The Deserializer will lock onto embedded clock within the specified amount of time. An embedded clock and data recovery (CDR) circuit locks to the incoming bit stream to recover the high-speed receive bit clock and re-time incoming data. The CDR circuit expects a coded input bit stream. In order for the Deserializer to lock to a random data stream from the Serializer, it performs a series of operations to identify the rising clock edge and validates data integrity, then locks to it. Because this locking procedure is independent on the data pattern, total random locking duration may vary. At the point when the Deserializer’s CDR locks to the embedded clock, the LOCK pin goes high and valid RCLK/data appears on the outputs. Note that the LOCK signal is synchronous to valid data appearing on the outputs. The Deserializer’s LOCK pin is a convenient way to ensure data integrity is achieved on receiver side.

DATA TRANSFER

After Serializer lock is established, the inputs DIN0–DIN23 may be used to input data to the Serializer. Data is clocked into the Serializer by the TCLK input. The edge of TCLK used to strobe the data is selectable via the TRFB pin. TRFB high selects the rising edge for clocking data and low selects the falling edge. The Serializer outputs (DOUT±) are intended to drive point-to-point connections as shown in *Figure 17*.

CLK1, CLK0, DCA, DCB are four overhead bits transmitted along the single LVDS serial data stream. The CLK1 bit is always high and the CLK0 bit is always low. The CLK1 and CLK0 bits function as the embedded clock bits in the serial stream. DCB functions as the DC Balance control bit. It does not require any pre-coding of data on transmit side. The DC Balance bit is used to minimize the short and long-term DC bias on the signal lines. This bit operates by selectively sending the data either unmodified or inverted. The DCA bit is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are integrated and automatically performed within Serializer and Deserializer.

Serialized data and clock/control bits (24+4 bits) are transmitted from the serial data output (DOUT±) at 28 times the TCLK frequency. For example, if TCLK is 35 MHz, the serial rate is 35 x 28 = 980 Mega bits per second. Since only 24 bits are from input data, the serial “payload” rate is 24 times the TCLK frequency. For instance, if TCLK = 35 MHz, the payload data rate is 35 x 24 = 840 Mbps. TCLK is provided by the data source and must be in the range of 5 MHz to 35 MHz nominal. The Serializer outputs (DOUT±) can drive a point-to-point connection. The outputs transmit data when the enable pin (DEN) is high, TPWDNB is high. The DEN pin may be used to TRI-STATE the outputs when driven low.

When the Deserializer channel attains lock to the input from a Serializer, it drives its LOCK pin high and synchronously delivers valid data and recovered clock on the output. The Deserializer locks onto the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock to the RCLK pin. The recovered clock (RCLK output pin) is synchronous to the data on the ROUT[23:0] pins. While LOCK is high, data on ROUT[23:0] is valid. Otherwise, ROUT[23:0] is invalid. The polarity of the RCLK edge is controlled by the RRFB input. ROUT(0-23), LOCK and RCLK outputs will each drive a maximum of 8 pF load with a 35 MHz clock. REN controls TRI-STATE for ROUTn and the RCLK pin on the Deserializer.

RESYNCHRONIZATION

If the Deserializer loses lock, it will automatically try to re-establish lock. For example, if the embedded clock edge is not detected one time in succession, the PLL loses lock and the LOCK pin is driven low. The Deserializer then enters the operating mode where it tries to lock to a random data stream. It looks for the embedded clock edge, identifies it and then proceeds through the locking process. The logic state of the LOCK signal indicates whether the data on ROUT is valid; when it is high, the data is valid. The system must monitor the LOCK pin to determine whether data on the ROUT is valid.

POWERDOWN

The Powerdown state is a low power sleep mode that the Serializer and Deserializer may use to reduce power when no data is being transferred. The TPWDNB and RPWDNB are

used to set each device into power down mode, which reduces supply current to the µA range. The Serializer enters powerdown when the TPWDNB pin is driven low. In powerdown, the PLL stops and the outputs go into TRI-STATE, disabling load current and reducing supply. To exit Powerdown, TPWDNB must be driven high. When the Serializer exits Powerdown, its PLL must lock to TCLK before it is ready for the Initialization state. The system must then allow time for Initialization before data transfer can begin. The Deserializer enters powerdown mode when RPWDNB is driven low. In powerdown mode, the PLL stops and the outputs enter TRI-STATE. To bring the Deserializer block out of the powerdown state, the system drives RPWDNB high.

Both the Serializer and Deserializer must reinitialize and relock before data can be transferred. The Deserializer will initialize and assert LOCK high when it is locked to the input clock.

TRI-STATE

For the Serializer, TRI-STATE is entered when the DEN or TPWDNB pin is driven low. This will TRI-STATE both driver output pins (DOUT+ and DOUT–). When DEN is driven high, the serializer will return to the previous state as long as all other control pins remain static (TPWDNB, TRFB).

When you drive the REN or RPWDNB pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT23) and RCLK will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL. The Deserializer input pins are high impedance during receiver powerdown (RPWDNB low) and power-off (V_{CC} = 0V).

PRE-EMPHASIS

The DS90C241 features a Pre-Emphasis function used to compensate for long or lossy transmission media. Cable drive is enhanced with a user selectable Pre-Emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance will be limited by the loss characteristics and quality of the media. Pre-Emphasis adds extra current during LVDS logic transition to reduce the cable loading effects and increase driving distance. In addition, Pre-Emphasis helps provide faster transitions, increased eye openings, and improved signal integrity. To enable the Pre-Emphasis function, the “PRE” pin requires one external resistor (Rpre) to Vss in order to set the additional current level. Pre-Emphasis strength is set via an external resistor (Rpre) applied from min to max (floating to 3kΩ) at the “PRE” pin. A lower input resistor value on the ”PRE” pin increases the magnitude of dynamic current during data transition. There is an internal current source based on the following formula: PRE = (Rpre ≥ 3kΩ); I_{MAX} = [(1.2/Rpre) X 20]. The ability of the DS90C241 to use the Pre-Emphasis feature will extend the transmission distance up to 10 meters in most cases.

The amount of Pre-Emphasis for a given media will depend on the transmission distance of the application. In general, too much Pre-Emphasis can cause over or undershoot at the receiver input pins. This can result in excessive noise, crosstalk and increased power dissipation. For short cables or distances, Pre-Emphasis may not be required. Signal quality measurements are recommended to determine the proper amount of Pre-Emphasis for each application.

AC-COUPLING AND TERMINATION

The DS90C241 and DS90C124 supports AC-coupled interconnects through integrated DC balanced encoding/decoding scheme. To use AC coupled connection between the Serializer and Deserializer, insert external AC coupling capacitors in series in the LVDS signal path as illustrated in *Figure 17*. The Deserializer input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal V_{CM} to +1.2V. With AC signal coupling, capacitors provide the ac-coupling path to the signal input.

For the high-speed LVDS transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The most common used capacitor value for the interface is 100 nF (0.1 uF) capacitor. NPO class 1 or X7R class 2 type capacitors are recommended. 50 WVDC should be the minimum used for the best system-level ESD performance.

The DS90C124 input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal VCM to +1.2V. Therefore multiple termination options are possible.

Receiver Termination Option 1

A single 100 Ohm termination resistor is placed across the RIN± pins (see *Figure 17*). This provides the signal termination at the Receiver inputs. Other options may be used to increase noise tolerance.

Receiver Termination Option 2

For additional EMI tolerance, two 50 Ohm resistors may be used in place of the single 100 Ohm resistor. A small capacitor is tied from the center point of the 50 Ohm resistors to ground (see *Figure 20*). This provides a high-frequency low impedance path for noise suppression. Value is not critical, 4.7nF maybe used with general applications.

Receiver Termination Option 3

For high noise environments an additional voltage divider network may be connected to the center point. This has the advantage of a providing a DC low-impedance path for noise suppression. Use resistor values in the range of 75Ω-2KΩ for the pullup and pulldown. Ratio the resistor values to bias the center point at 1.2V. For example (see *Figure 21*): VDD=3.3V, Rpullup=1.3KΩ, Rpulldown=750Ω; or Rpullup=130Ω, Rpulldown=75Ω (strongest). The smaller values will consume more bias current, but will provide enhanced noise suppression.

PROGRESSIVE TURN–ON (PTO)

Deserializer ROUT[23:0] outputs are grouped into three groups of eight, with each group switching about 0.5UI apart in phase to reduce EMI, simultaneous switching noise, and system ground bounce.

Applications Information

USING THE DS90C241 AND DS90C124

The DS90C241/DS90C124 Serializer/Deserializer (SERDES) pair sends 24 bits of parallel LVCMOS data over a serial LVDS link up to 840 Mbps. Serialization of the input data is accomplished using an on-board PLL at the Serializer which embeds clock with the data. The Deserializer extracts the clock/control information from the incoming data stream and deserializes the data. The Deserializer monitors the incoming clockl information to determine lock status and will indicate lock by asserting the LOCK output high.

DISPLAY APPLICATION

The DS90C241/DS90C124 chipset is intended for interface between a host (graphics processor) and a Display. It supports an 18-bit color depth (RGB666) and up to 800 X 480 display formats. In a RGB666 configuration 18 color bits (R [5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) along with three spare bits are supported across the serial link with PCLK rates from 5 to 35 MHz.

TYPICAL APPLICATION CONNECTION

Figure 18 shows a typical application of the DS90C241 Serializer (SER). The LVDS outputs utilize a 100 ohm termination and 100nF coupling capacitors to the line. Bypass capacitors are placed near the power supply pins. A system GPO (General Purpose Output) controls the TPWDNB pin. In this application the TRFB pin is tied High to latch data on the rising edge of the TCLK. The DEN signal is not used and is tied High also. In this application the link is short, therefore the VODSEL pin is tied Low for the standard LVDS swing. The pre-emphasis input utilizes a resistor to ground to set the amount of pre-emphasis desired by the application.

Figure 19 shows a typical application of the DS90C124 Deserializer (DES). The LVDS inputs utilize a 100 ohm termination and 100nF coupling capacitors to the line. Bypass capacitors are placed near the power supply pins. A system GPO (General Purpose Output) controls the RPWDNB pin. In this application the RRFB pin is tied High to strobe the data on the rising edge of the RCLK. The REN signal is not used and is tied High also.

POWER CONSIDERATIONS

An all CMOS design of the Serializer and Deserializer makes them inherently low power devices. Additionally, the constant current source nature of the LVDS outputs minimize the slope of the speed vs. I_{CC} curve of CMOS designs.

NOISE MARGIN

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably recover data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)

Media: ISI, V_{CM} noise

Deserializer: V_{CC} noise

For a graphical representation of noise margin, please see *Figure 16*.

TRANSMISSION MEDIA

The Serializer and Deserializer can be used in point-to-point configuration, through a PCB trace, or through twisted pair cable. In a point-to-point configuration, the transmission media needs be terminated at both ends of the transmitter and receiver pair. Interconnect for LVDS typically has a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. In most applications that involve cables, the transmission distance will be determined on data rates involved, acceptable bit error rate and transmission medium.

LIVE LINK INSERTION

The Serializer and Deserializer devices support live pluggable applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS90C124 to attain lock to the active data stream during a live insertion event.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS SERDES devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz range. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS (LVTTL) signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled

lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications, termination should be located at both ends of the devices. Nominal value is 100 Ohms to match the line's differential impedance. Place the resistor as close to the transmitter DOUT± outputs and receiver RIN± inputs as possible to minimize the resulting stub between the termination resistor and device.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - —S = space between the pair
  - —2S = space between pairs
  - —3S = space to LVCMOS/LVTTL signal
- Minimize the number of VIA
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the National web site at: **www.national.com/lvds**

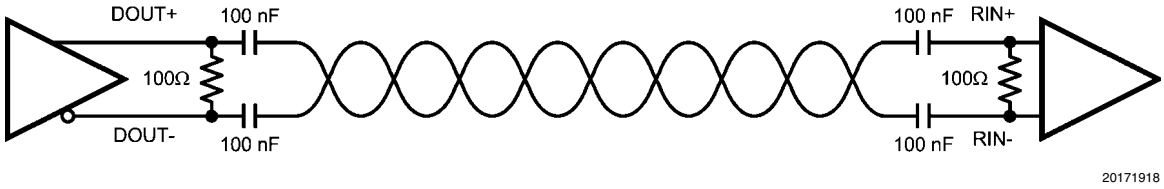


FIGURE 17. AC Coupled Application

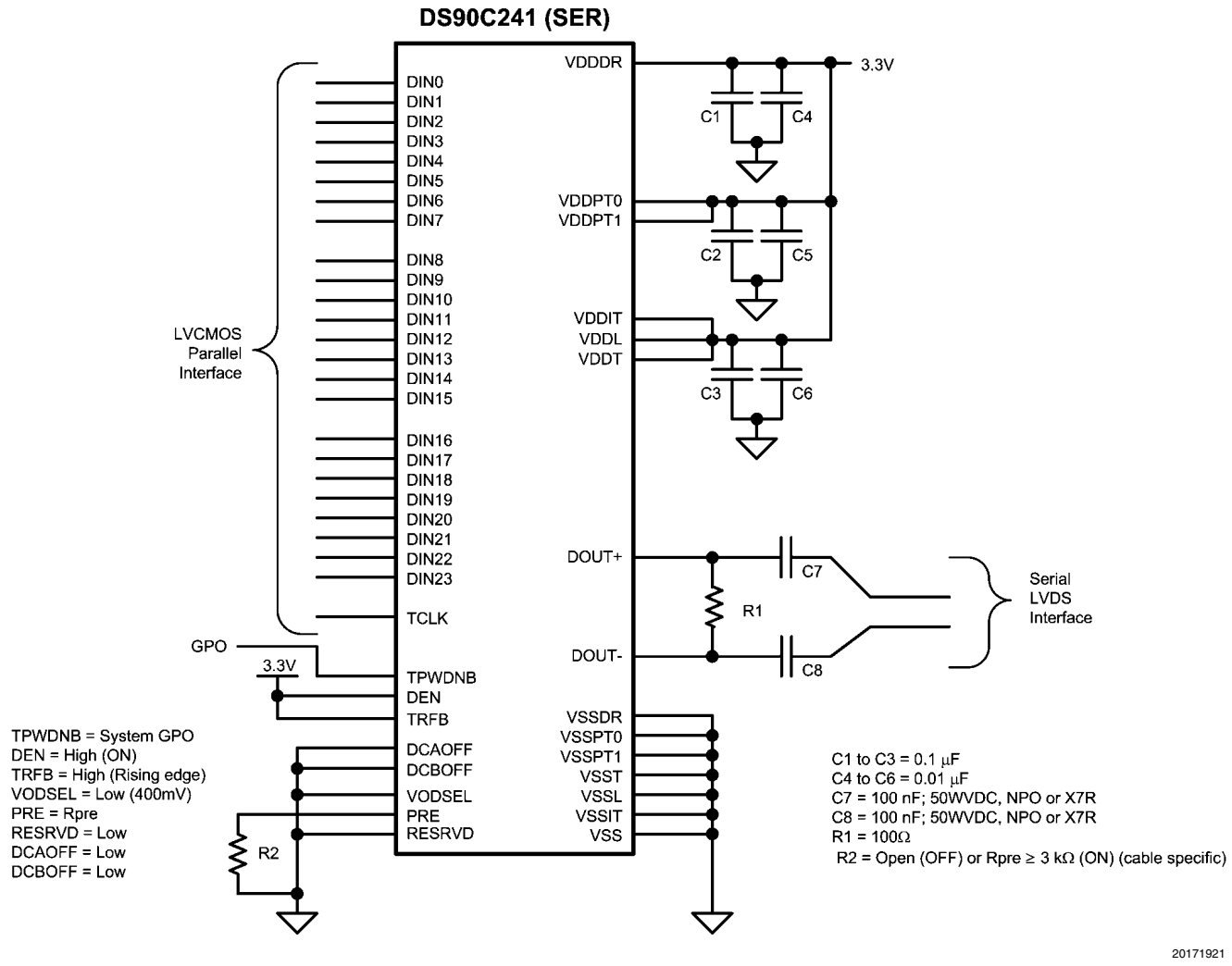


FIGURE 18. DS90C241 Tyical Application Connection

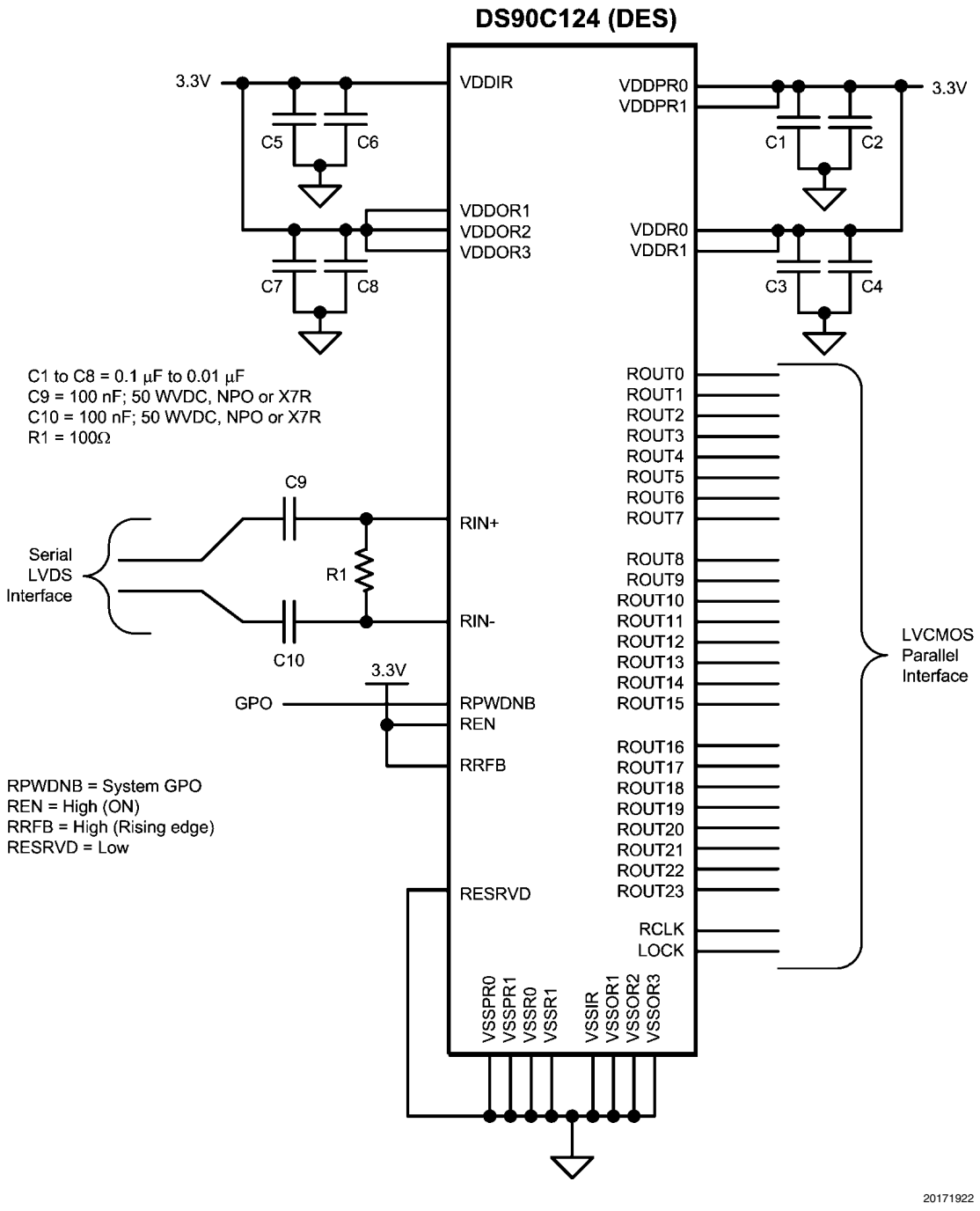


FIGURE 19. DS90C124 Tyical Application Connection

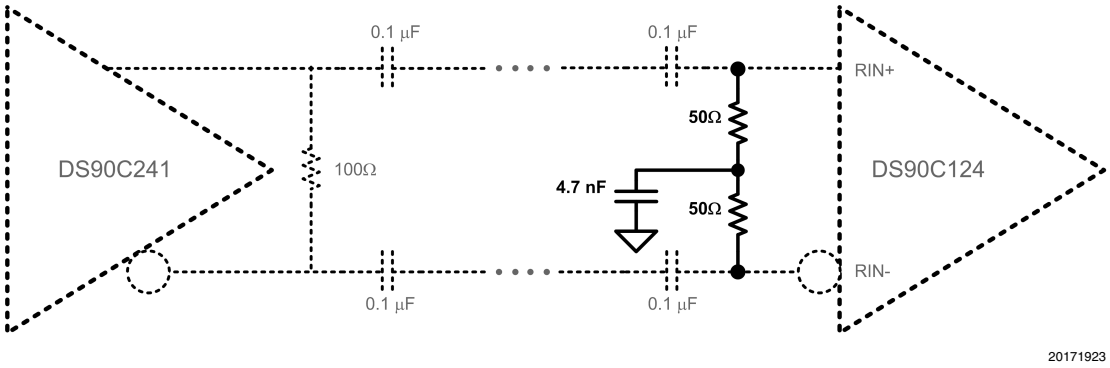


FIGURE 20. Receiver Termination Option 2

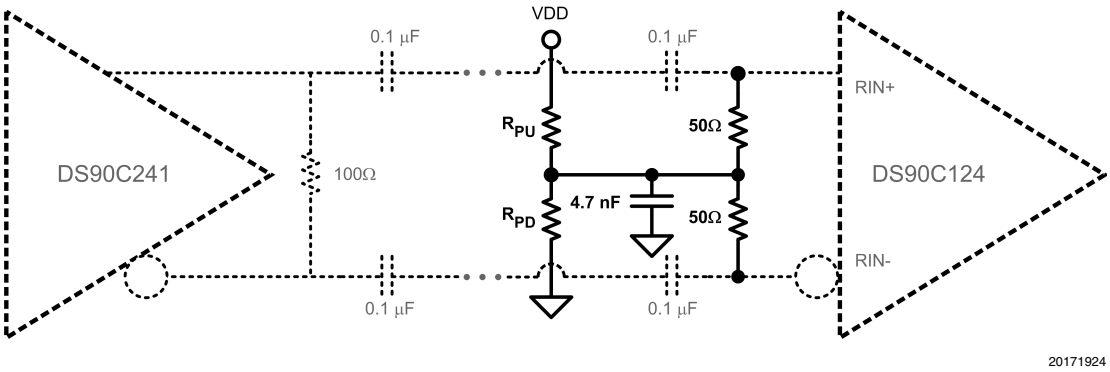


FIGURE 21. Receiver Termination Option 3

Truth Tables

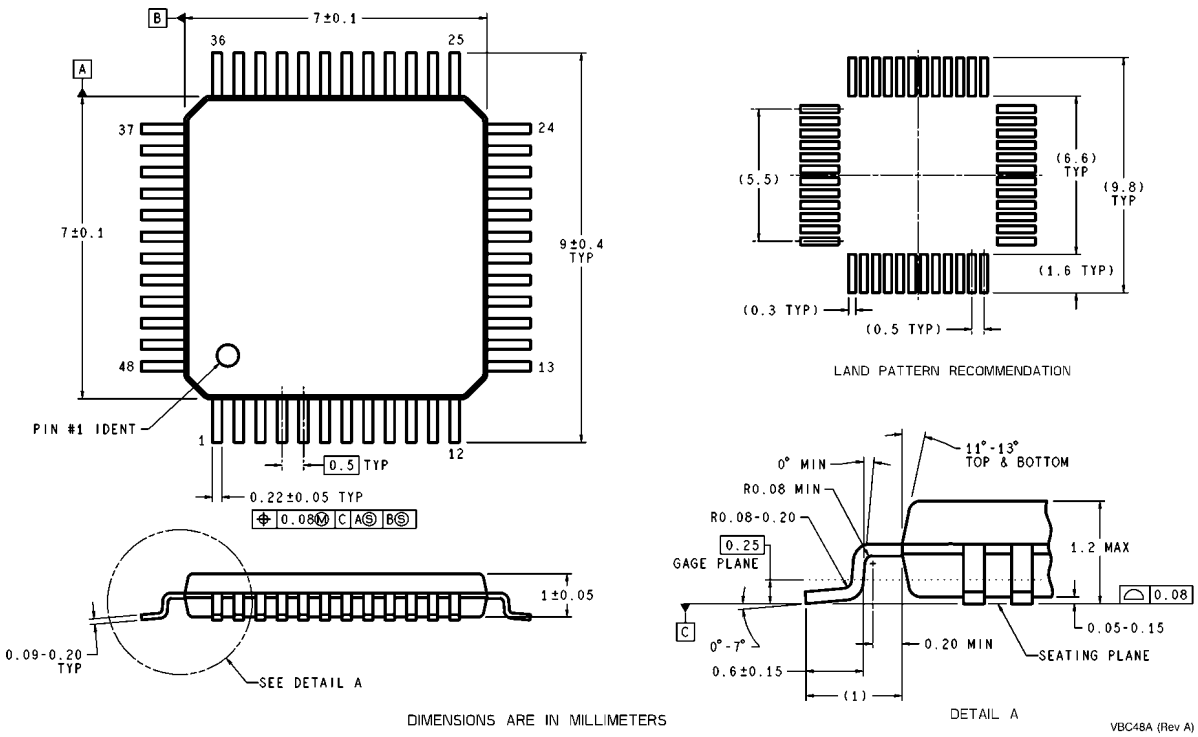
TABLE 1. DS90C241 Serializer Truth Table

TPWDNB (Pin 9)	DEN (Pin 18)	Tx PLL Status (Internal)	LVDS Outputs (Pins 19 and 20)
L	X	X	Hi Z
H	L	X	Hi Z
H	H	Not Locked	Hi Z
H	H	Locked	Serialized Data with Embedded Clock

TABLE 2. DS90C124 Deserializer Truth Table

RPWDNB (Pin 1)	REN (Pin 48)	Rx PLL Status (Internal)	ROUTn and RCLK (See Pin Diagram)	LOCK (Pin 17)
L	X	X	Hi Z	Hi Z
H	L	X	Hi Z	L = PLL Unocked; H = PLL Locked
H	H	Not Locked	Hi Z	L
H	H	Locked	Data and RCLK Active	H

Physical Dimensions inches (millimeters) unless otherwise noted



Dimensions show in millimeters only
NS Package Number VBC48A

Ordering Information

NSID	Package Type	Package ID
DS90C241QVS	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch	VBC48A
DS90C241QVSX	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel	VBC48A
DS90C241IVS	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch	VBC48A
DS90C241IVSX	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel	VBC48A
DS90C124QVS	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch	VBC48A
DS90C124QVSX	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel	VBC48A
DS90C124IVS	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch	VBC48A
DS90C124IVSX	48 Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel	VBC48A

Notes

Notes

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Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
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