STw5094

18 BIT 8kHz TO 48kHz LOW POWER STEREO AUDIO DAC WITH INTEGRATED POWER AMPLIFIERS AND VOICE CODEC

FEATURES:

Complete STEREO AUDIO DAC and FILTERS including:

- 18 BIT DIGITAL TO ANALOG CONVERTERS.
- LINEAR PHASE DIGITAL FILTERS.
- ACTIVE LINEAR PHASE SMOOTHING FILTER.
- 30Ω LOAD STEREO HEADPHONES DRIVERS, 8Ω LOAD MONO LOUDSPEAKER DRIVER FOR GROUP LISTENING.

Stereo Audio DAC Features:

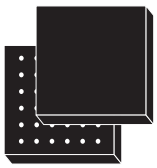
- MULTIBIT ΣΔ MODULATOR WITH DATA WEIGHTED AVERAGING DAC.
- 92 dB DYNAMIC RANGE, 0.01% THD OVER 30Ω LOAD PERFORMANCE.
- SUPPORTS ALL THE MPEG 1 & 2 SAMPLING FREQUENCIES AND THE EXTENSION TO MPEG 2.5: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz.
- TONES FROM TONE GENERATOR CAN BE INJECTED IN THE AUDIO PATHS.

Stereo Headphones and Loudspeaker/Earpiece Power Amplifiers features and Stereo Input for FM Radio Features:

- 20kHz BANDWIDTH STEREO HEADPHONES OUTPUTS. DRIVING CAPABILITY: 20mW (TYP. 0.1% T.H.D) OVER 30Ω WITH 40 dB RANGE PROGRAMMABLE GAIN.
- BALANCED EARPIECE/LOUDSPEAKER OUTPUT. DRIVING CAPABILITY: 190mW (TYP. 0.1% T.H.D) OVER 8Ω WITH 30dB RANGE PROGRAMMABLE GAIN.
- ANALOG STEREO INPUT FOR FM RADIO WITH 38 dB RANGE PROGRAMMABLE GAIN.

Complete CODEC and FILTER system including:

- 14 BIT LINEAR ADC AND DAC.
- 8 BIT COMPANDED ADC AND DAC A-LAW OR μ-LAW.
- TRANSMIT AND RECEIVE DIGITAL BAND-PASS FILTERS.
- ACTIVE ANTIALIAS AND SMOOTHING FILTERS.
- 8Ω LOAD EARPIECE/LOUDSPEAKER DRIVER, 30Ω LOAD AUXILIARY DRIVER.



TFBGA 6x6 (36 pins)
ORDERING NUMBER: STw5094

Voice CODEC Features:

- SUPPORT BOTH 8kHz AND 16kHz SAMPLING RATE.
- ONE MICROPHONE BIASING OUTPUT.
- REMOTE CONTROL FUNCTION.
- ONE LINE INPUT AND TWO SWITCHABLE MICROPHONE AMPLIFIER INPUTS. 42.5dB RANGE PROGRAMMABLE GAIN.
- TRANSIENT SUPRESSION DURING POWER UP AND POWER DOWN.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT.
- INTERNAL RING, TONE AND DTMF GENERATOR.
- PROGRAMMABLE PWM BUZZER DRIVER.

General Features:

- SINGLE 2.7V to 3.3V SUPPLY.
- EXTENDED TEMPERATURE RANGE OPERATION (*) -40°C to 85°C.
- 1 μW STANDBY POWER (TYP. AT 2.7V).
- 13 mW OPERATING POWER IN AUDIO LISTENING MODE (TYP. AT 2.7V).
- 11 mW OPERATING POWER IN VOICE CODEC MODE (TYP. AT 2.7V).
- 1.8V TO 3.3V CMOS COMPATIBLE DIGITAL INTERFACES.
- PROGRAMMABLE PCM INTERFACE.
- I^2C COMPATIBLE CONTROL INTERFACE.
- PROGRAMMABLE SERIAL AUDIO DATA INPUT INTERFACE (I^2S AND OTHER FORMATS).

(*) Functionality guaranteed in the range - 40°C to +85°C; Timing and Electrical Specifications are guaranteed in the range - 30°C to +85°C.

APPLICATIONS:

- CDMA,GSM,DCS1800,PCS1900,JDC DIGITAL CELLULAR TELEPHONES WITH MP3 AND FM RADIO STEREO LISTENING FUNCTIONS.
- PORTABLE DEVICES WITH A STEREO DIGITAL AUDIO SOURCE AND FM RADIO LISTENING FUNCTION.

GENERAL DESCRIPTION

STw5094 is a low power Stereo Audio DAC device with Headphones Amplifiers for high quality MP3 and FM radio listening. The STw5094 includes also an high performance low power combined PCM CODEC/FILTER tailored to implement the audio front-end functions required by low voltage low power consumption digital cellular terminals with added MP3 and FM radio listening.

STw5094 offers a number of programmable functions accessed through an I^2C-bus compatible interface.

The STw5094 Stereo Audio DAC section is suited for MP3, or any other audio stereo source, listening. It supports all the MP3 rates from 8kHz to 48kHz. The audio data serial interface is I^2S compatible and can be programmed to handle 16 to 24 bit word length input data. The internal D to A converters work with 18 bit input resolution.

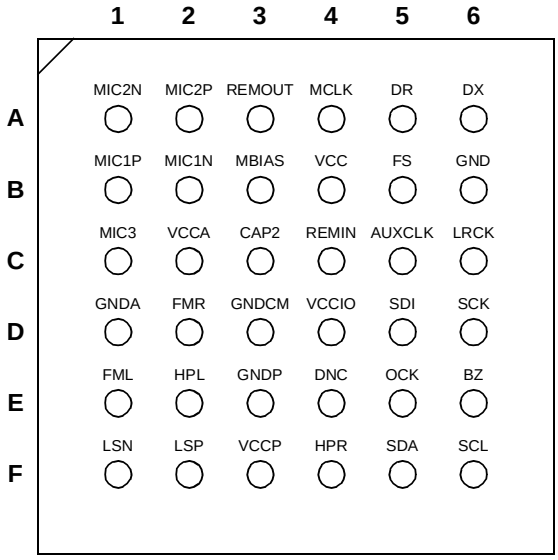
The Stereo Headphones drivers can also be used for FM Radio listening via an auxiliary stereo analog input. A Loudspeaker driver can also be used for monophonic group listening.

The STw5094 Voice Codec section can be configured either as a 14-bit linear or as an 8-bit companded PCM coder. The Frame Synchronism frequency of the Voice Codec can be either the standard 8kHz value or the extended 16kHz one.

In addition to the Stereo Audio DAC and CODEC/FILTER functions, STw5094 includes a Tone/Ring/DTMF generator that can be used both in Audio Listening mode and in Voice Codec mode, a sidetone generation, a buzzer driver output and a remote control function tailored to handle an external on-hook off-hook button.

STw5094 Voice Codec fulfills and exceeds D3/D4 and CCITT recommendations and ETSI requirements for digital handset terminals. The Stereo Audio DAC part fulfills and exceeds the requirements for MP3 quality and FM radio quality listening. Main applications include digital mobile phones, as cellular and cordless phones, with added low-power high-quality MP3 and/or FM radio listening features, or any battery powered equipment that requires Stereo Audio DAC with Headphones drivers operating at low single supply voltage.

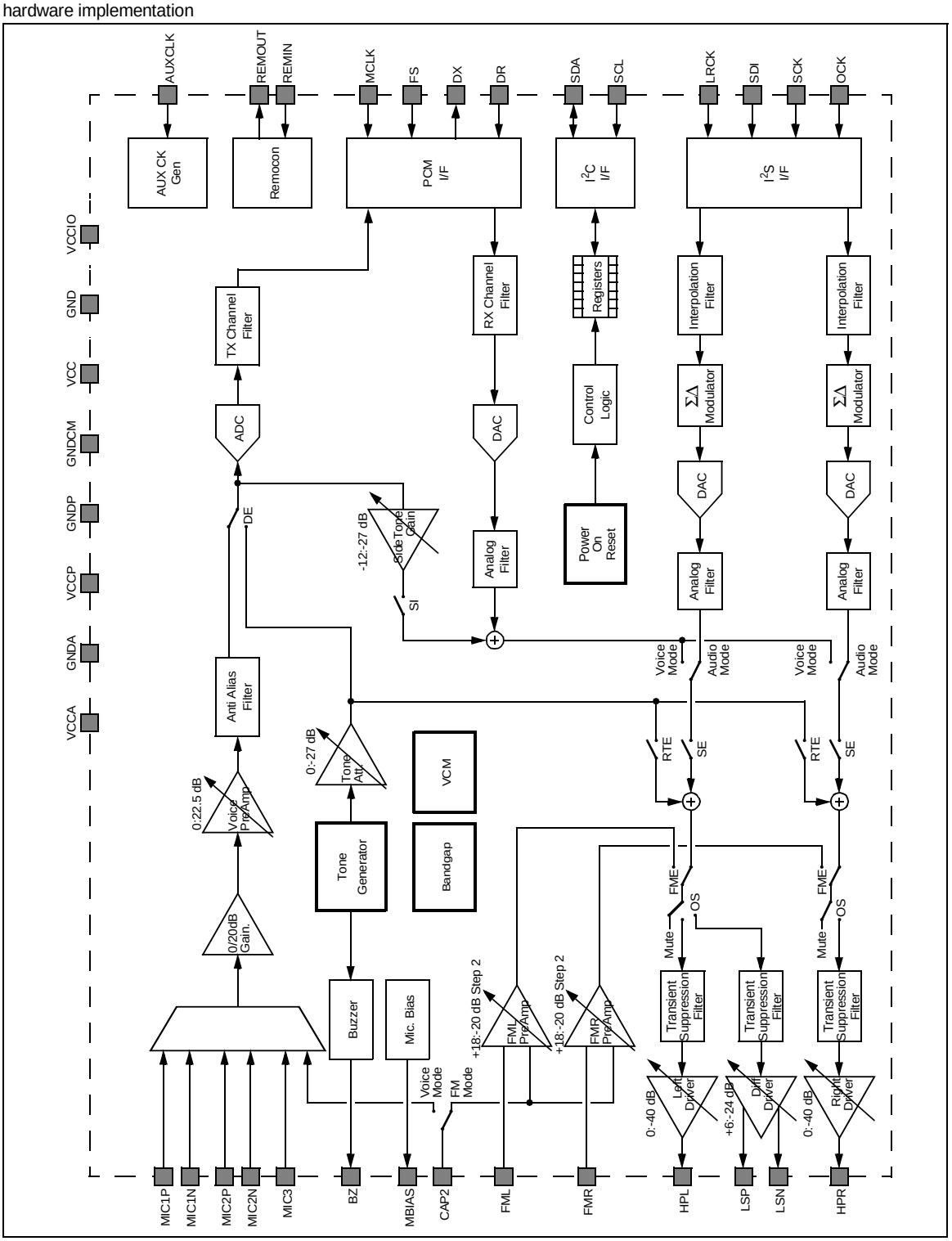
PIN CONNECTIONS (Top view)



TFBGA 6x6x1.2 (36 Pin)

FUNCTIONAL BLOCK DIAGRAM

NOTE: This diagram shows the functionality of the device and of some register bits but it does not necessarily reflect the exact hardware implementation



PIN FUNCTION

Pin N°	Name	Type	Description
B1	MIC1P	AI	Positive high impedance input to transmit preamplifier for microphone 1 connection.
B2	MIC1N	AI	Negative high impedance input to transmit preamplifier for microphone 1 connection.
A2	MIC2P	AI	Positive high impedance input to transmit preamplifier for microphone 2 connection.
A1	MIC2N	AI	Negative high impedance input to transmit preamplifier for microphone 2 connection.
C1	MIC3	AI	High impedance single ended input to transmit preamplifier for line input connection. Only 0dB gain is allowed.
B3	MBIAS	AO	Microphone Biasing Switch.
E1	FML	AI	Auxiliary analog audio Left channel input.
D2	FMR	AI	Auxiliary analog audio Right channel input.
F2,F1	LSP, LSN	AO	Receive analog amplifier complementary outputs. This differential output can drive 50nF (with series resistor) or directly an earpiece transductor of 8Ω. The signal at this output can be: the sum of the Receive Speech signal from DR, the Internal Tone Generator, and the Sidetone signal, or the sum of the Audio Left channel and the Internal Tone Generator, or can come from FML input.
E2	HPL	AO	Audio headphone amplifier Left channel output. This output can drive 50nF (with series resistor) or directly an earpiece transductor of 30Ω. The signal at this output can be the sum of Audio Left channel and Internal Tone Generator, or the sum of Receive Speech signal from DR, Internal Tone Generator, Sidetone signal, or can come from FML input.
F4	HPR	AO	Audio headphone amplifier Right channel output. This output can drive 50nF (with series resistor) or directly an earpiece transductor of 30Ω. The signal at this output can be the sum of Audio Right channel and Internal Tone Generator, or the sum of Receive Speech signal from DR, Internal Tone Generator, Sidetone signal, or can come from FMR input.
A3	REMOUT	DO	Remocon function digital output.
C4	REMIN	DI	Remocon function input. A high level at this pin is detected as a non pressed key, while a low level is detected as a pressed key.
E6	BZ	AO	Pulse width modulated buzzer driver output.
F6	SCL	DI	I2C-bus interface serial clock input. SCL is asynchronous with the other system clocks.
F5	SDA	DIO	I2C-bus interface serial data input-output.
C6	LRCK	DI	Left/Right clock for Audio interface input.
D6	SCK	DI	Audio interface Clock input.
D5	SDI	DI	Audio interface Data input.
E5	OCK	DI	Master Clock Input for Audio Mode. Can also be used as Master Clock in Tone Only and FM Modes.
A6	DX	DOT	Transmit Data output: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere DX output is in the high impedance state. In delayed and non-delayed normal frame sync modes, voice data byte is shifted out from tristate output DX at the MCLK frequency on the rising edge of MCLK, while in non-delayed reverse frame sync mode voice data is shifted out on the falling edge of MCLK.
A5	DR	DI	Receive data input: Data is shifted in during the assigned Received time slots In delayed and non-delayed normal frame sync modes voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK, while in non-delayed reverse frame sync mode voice data byte is shifted in on the rising edge of MCLK.

PIN FUNCTION (continued)

Pin N°	Name	Type	Description
B5	FS	DI	Frame Sync input: This signal is a 8/16kHz clock which defines the start of the transmit and receive frames. Any of three formats may be used for this signal: non delayed normal mode, delayed mode, and non delayed reverse mode.
A4	MCLK	DI	Master Clock Input for Voice Mode. Can also be used as Master Clock in Tone Only and FM Modes. The allowed clock frequencies are 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz. MCLK is the Voice Data Clock.
C5	AUXCLK	DI	Auxiliary Clock Input. Can be used as Master Clock in Tone Only and FM Modes. Allowed clock frequencies are 512kHz, 1.536MHz, 2.048MHz or 2.56MHz.
E4	DNC	AI	Do Not Connect. This pin must be left unconnected.
C3	CAP2	AI	A capacitor must be connected between this node and Ground.
C2	VCCA	P	Power supply input for the analog section. VCC and VCCA can be directly connected together for low cost applications.
D1	GNDA	P	Analog Ground: All analog signals are referenced to this pin. GND and GNDA can be connected together for low cost applications.
F3	VCCP	P	Power supply input for the output drivers. VCCP and VCCA must be connected together.
E3	GNDP	P	Power ground. Output drivers are referenced to this pin. GNDP and GNDA must be connected together.
D3	GNDCM	P	Analog Ground connection. GNDCM can be connected to GNDA.
B4	VCC	P	Power supply input for the digital section.
B6	GND	P	Ground for the digital section
D4	VCCIO	P	Power supply Input for the Digital I/O pins.

Type definitions:

AI - Analog input, AO - Analog Output, DI - Digital Input, DO - Digital output, DOT - Digital Output Tristate, DIO - Digital Input Output Open Drain, P - Power Supply or Ground.

FUNCTIONAL DESCRIPTION

I DEVICE MODES

STw5094 can work in 4 different modes, selected by bits **MD** in Control Register 18 (**CR18**). Depending on the mode different data interfaces, clock inputs, and internal blocks are selected. A built-in power consumption management function keeps in power down the blocks that are not needed by the selected operating mode. In all the modes the Output Drivers can be activated in all the combinations allowed by bits **OS** in **CR6** (in case of stereo input and **LSP**/**N** driver selected the Left channel is sent to this driver, while in case of voice input and **HPL** + **HPR** drivers selected the same signal is sent to both drivers).

I.1 **Audio Mode:**

In Audio mode the path from the I^2S I/F to the output drivers is active to allow the Stereo Audio DAC function. The I^2S I/F is active while the PCM I/F is inactive.
The master clock of the device is **OCK**. The **OCK** frequency must be 256 times the sampling frequency for the MPEG1 and MPEG2 sampling frequencies and 512 times for the MPEG2.5 sampling frequencies.
The sampling frequency (**LRCK** frequency) can be selected with bits **LAY** and **AFS** in **REG6**.
Since the **OCK** clock is used directly in all the Audio blocks, its jitter and spectral properties must be adequate to the desired Audio quality.
The Tone/Ring/DTMF generator can be activated if needed. The FM preamplifiers are in power down.

I.2 **Voice Mode:**

In Voice mode the TX path from microphone or line input to **DX** and the RX path from **DR** to the output drivers are active to allow the PCM CODEC function. The PCM I/F is active while the I^2S I/F is inactive.
The master clock of the device is **MCLK**, the frequency of the clock can be selected with bits **F** in **CR0**.
The FM preamplifiers are in power down.

I.3 **Tone Only Mode:**

In Tone Only mode the path from the Tone generator to the output Drivers and to the Buzzer is active to allow Tones or Ringer listening only. Both I^2S I/F and PCM I/F are inactive, as all the Audio and Voice converters functions.
The master clock of the device can be selected to be **AUXCLK**, **MCLK** or **OCK** (bits **CFM** in **CR18**).
The Tone/Ring/DTMF generator can be activated if needed. The FM preamplifiers are in power down.

I.4 **FM Mode:**

In FM mode the path from **FML** and **FMR** analog inputs to the output Drivers is active to allow FM Stereo Radio listening. Both I^2S I/F and PCM I/F are inactive, as all the Audio and Voice converters functions.
The master clock of the device can be selected to be **AUXCLK**, **MCLK** or **OCK** (bits **CFM** in **CR18)**.
The Tone/Ring/DTMF generator is in power down.

II DEVICE OPERATION

II.1 **Power on initialization and Software Reset:**

When power is first applied, power on reset circuitry initializes STw5094 and puts it into the power down state. All the Registers are initialized as indicated in the Control Register description section. All the functions are disabled.
The registers can be initialized also writing bit **SRS** (software reset) in **CR18.**

II.2 **Power up/down control:**

It is recommended that all programmable functions (excluding the gain controls) are set while the device is powered down. Power state control can then be included in the last programming instruction (the power up bit **PU** is located in the last address register (**CR18**) so that the multi-byte mode of the control interface can be easily used to program all the required functions before power up).
When a power up command is given, all the circuits needed for the selected mode are activated (in Voice mode the **DX** output will remain in the high impedance state until the second **FS** pulse after power up arrives). A built-in power consumption management function keeps in power down the blocks that are not needed by the selected operating mode.

II.3 **Power down state:**

Following a period of activity, power down state may be reentered by writing 0 in bit **PU** in **CR18**. All the Control Registers remain in their current state and can be changed by I^2C control interface.
In addition to the power down instruction, the detection of absence of the current Master Clock (no transition detected) automatically puts the device in power down state without setting bit **PU**. If transitions on the master clock are detected the device is put again in power up.

II.4 **Voice Transmit section:**

This section is active in Voice Mode. Voice Transmit analog preamplifier gain is designed in two stages to enable gains up to 42.5 dB. Stage 1 provides a selectable 0 or 20 dB gain via bit **PG** in **CR4**. Stage 2 is a programmable gain amplifier which provides from 0 to 22.5 dB of additional gain in 1.5dB step. It can be programmed with bits **TXA** in **CR4**. Two differential microphone inputs (**MIC1P/N, MIC2P/N**) and one single ended line input (**MIC3**) are provided. The line input **MIC3** can only be used with preamplifier gain set to 0dB in both stages. The microphone input or Transmit Mute is selected with bits **MS** in **CR4**. In the Mute case, the analog transmit signal is grounded. A separate **MBIAS** output can be used to bias a microphone (bit **MB** in **CR4**). An active anti-alias filter then precedes the single bit $\Sigma\Delta$ analog to digital converter that is followed by an 8th order IIR digital TX channel filter. The TX channel filter is band-pass if the **FS** frequency is 8kHz and low-pass if the **FS** frequency is 16kHz (bit **VFS** in **CR0**). A precision on chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the analog blocks is cancelled by an internal autozero circuit. Voice data is sent to the PCM I/F to be serially sent to **DX** output.

II.5 **Voice Receive section:**

This section is active in Voice Mode. Voice Data coming from PCM I/F **DR** pin is sent to the 8th order digital IIR RX channel filter. The filter can be selected to be band-pass or low-pass, with bit **HPB** in **CR5**, when **FS** frequency is 8kHz, while it is always low-pass when **FS** frequency is 16kHz. The filter is followed by a $\Sigma\Delta$ digital to analog converter and a 3rd order switched-capacitor reconstruction filter. The Sidetone can be summed to the received signal (bit **SI** in **CR5**) and its amplitude can be programmed with bits **SA** in **CR5**.

II.6 **Stereo Audio DAC section:**

This section is active in Audio Mode. The Left and Right Audio samples coming from the I^2S Interface are interpolated with an FIR filter in order to feed the oversampled multi-bit $\Sigma\Delta$ modulator, the digital to analog converter is followed by a 3rd order switched-capacitor reconstruction filter.

II.7 **Output Drivers section:**

There are 3 Analog Output Drivers. The **LSP/N** differential driver delivers 190mW typical power with 0.1% T.H.D. (140mW minimum undistorted) on a 8Ω earpiece/loudspeaker (piezoceramic loads up to 50nF can also be driven, with a series resistor), it has a 30dB range gain control (bits **LSA** in **CR7**). The 2 single ended drivers (**HPL** and **HPR**) deliver 20mW typical power with 0.1% T.H.D. (16.5mW minimum undistorted) on 30Ω stereo headphones, they have a 40dB range gain control (**CR8** for **HPL** and **CR9** for **HPR**). It is possible to put all the drivers in power-down, enable the **LSP/N** one, enable the **HPL** one or enable **HPL** and **HPR** together

programming bits **OS** in **CR6**. These settings are not dependent from the selected operative Mode. If **HPL** and **HPR** are enabled together in Voice Mode or Tone Only Mode the same signal is sent to both Drivers. The active Drivers can be muted (keeping them in power-up state) using bit **MUT** in **CR7**. At power-up or after a change in **OS** bits the outputs are muted for 10 ms to avoid unwanted noise. The transient suppression filter is used to avoid clicks when the gain value is changed.

II.8 **Tone Generator:**

The Tone Generator can be activated (writing **CR12**) in all the Stw5094 operating modes except FM mode. In Voice and Audio modes the tones are summed to the signal. It is possible to generate 1 or 2 summed waveforms (either sinusoidal or square wave), their frequencies can be set in **CR13** for the first one (f1) and in **CR14** for the second one (f2) accordingly to the values listed in Table 1. The amplitude of the generated waveform can be regulated in **CR12** over a 33dB range. When both f1 and f2 are selected the amplitude of f1 and f2 are lowered by 5dB and 7dB respectively with respect to the amplitude of a single waveform. In this way the amplitude of the summed waveforms does not overload and there is a 2dB difference between f1 and f2 amplitude as required for DTMF generation. The Tone Generator output can be sent to the Voice Transmit section (in Voice Mode), to the Power amplifiers, possibly mixed with audio or voice, (in all the modes except FM mode) and to the buzzer output **BZ** (in all the modes except FM mode).

II.9 **Buzzer Output:**

The output **BZ** is intended to drive a Buzzer, via an external BJT, with a squarewave pulse width modulated (PWM) signal. The frequency of the signal is stored in **CR13** (see Table1 for frequency values). For some applications it is also possible to multiply this PWM signal with a squarewave signal having a frequency stored in **CR14**. The duty cycle of the buzzer output can be varied in **CR15** in order to change the buzzer volume. Maximum load for **BZ** is 5kΩ and 50pF.

II.10 **Voice Data Interface (PCM I/F):**

The PCM I/F is used to exchange the Voice data in both TX and RX direction, it can be programmed for linear format data or companded A-law or μ-law format (see Fig.1, 2 and 3).
Frame Sync input **FS** determines the beginning of frame. It may have any duration from a single cycle of **MCLK** to a squarewave. Three different relationships may be established between the Frame Sync input and the first time slot of the frame by setting bits **DM** in **CR1**. In non delayed normal and reverse data mode (long frame timing) the first time slot starts at the rising edge of FS. In delayed data mode (short frame sync timing) **FS** input must be high for at least a half cycle of **MCLK** before the frame start.
When linear code is selected (bit **CM** = 0 in **CR0**) the MSB is transmitted and received first, the word length is 16 bit. When companded code is selected (bit **CM** = 1 in **CR0**) a time slot assignment may be used in all timing modes (bit **TS** in **CR1**), that allows connection to one of the two B1 and B2 voice data channels. Two data formats are available: in Format 1, time slot B1 corresponds to the 8 **MCLK** cycles that immediately follow the rising edge of **FS**, while time slot B2 corresponds to the 8 **MCLK** cycles that immediately follow time slot B1. In Format 2, time slot B1 is identical to Format 1 while time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data. Data format is selected by bit **FF** in **CR0**.
Bit **EN** in **CR1** enables or disables data transfer on **DX** and **DR**.
Outside the selected time slot **DX** is in the high impedance condition. During the selected time slot the **DX** output and the **DR** input are synchronized as follow:
-If delayed or non-delayed modes are selected the transmit voice data is sent to **DX** output on the rising edges of **MCLK** and receive voice data is read at **DR** input on the falling edges of **MCLK**.
-If non-delayed reverse mode is selected the transmit voice data register is sent to **DX** output on the falling edges of **MCLK** and receive voice data is read at **DR** input on the rising edges of **MCLK.**
When 16kHz Frame Sync frequency is selected (bit **VFS** in **CR0**) the RX and TX filters are both low-pass and their cutoff frequencies are doubled.
It is possible to access the B channel data when companded A-law or μ-law formats are used (bits **MX** and **MR** in **CR1**). A byte written into **CR3** will be sent to **DX** output in place of the transmit channel PCM data. A byte written in **CR2** will be sent to the receive path. The current byte received on **DR** input can be read in **CR2**.

II.11 Audio Data Interface (I^2S I/F):

The I^2S I/F is used to receive the Left and Right channel Audio data (see Fig. 4 and 5). The interface is I^2S compatible and can be configured in other different modes writing **CR16**.
When the I^2S I/F is active (Audio mode) the Master Clock of the device is **OCK**. The frequency of **OCK** is 256 times the sampling frequency (**LRCK** frequency) when the sampling frequency is between 16kHz and 48kHz (**LAY(1)** = 0 in **CR6**), and 512 times when the sampling frequency is between 8kHz and 12kHz (**LAY** = 10 in **CR6**). The polarity of **OCK** can be selected**.**
SCK frequency is 32 times the **LRCK** one in case of 16bit Data word and 64 times in case of 18bit to 24bit Data word. Left channel data are always received first, the polarity of **LRCK** can be selected.
The first 35 Data frames after power up are discarded while the interpolation filters data memory is cleared.

II.12 Control Interface (I^2C I/F):

The I^2C I/F is used to program the device by writing and reading the control registers (see Fig 6 and 7). The interface is I^2C bus compatible, being the STw5094 a Slave device. **SDA** is the bidirectional open-drain data pin and **SCL** is the input clock pin. The Device Address is E2 hex. for writing and E3 hex. for reading.
The interface has an internal address register that keeps the current address of the control register to be read or written. At each write access of the interface the address register is loaded with the data of the register address field. The value in the address register is increased after each data byte read or write. It is possible to access the interface in 2 modes: single-byte mode in which the address and data of a single register are specified, and multi-byte mode in which the address of the first register to be written or read is specified and all the following bytes exchanged are the data of successive address registers starting from the one specified (in multi-byte mode the internal address counter restart from register 0 after the last register 18). Using the multi-byte mode it is possible to write or read all the registers with a single access to the device on the I^2C bus.
The Control interface can be used both in power-up and power-down state.

II.13 Master Clock in FM mode and Tone Only modes:

In FM mode and in Tone Only mode the Master Clock of the device can be selected to be **AUXCLK**, **MCLK** or **OCK** writing bits **CFM** in **CR18**. The Auxiliary clock **AUXCLK** can be used when the Audio mode clock **OCK** and the Voice mode clock **MCLK** are not available. **AUXCLK** and **MCLK** frequency selection is done with bits **F** in **CR0**.

II.14 REMOCON function:

The REMOCON (Remote Control) function can be used to detect the status of an headset button. The REMOCON function is enabled by setting bit **REN** in **CR17**. If enabled, this function is active also when the STw5094 is in power-down state.
A High level at **REMIN** input is detected as a non pressed button, while a low level is detected as a pressed button. The "Pressed Button" information can be treated in 2 ways depending on bit **RLM** in **CR17**:
- if **RLM** = 0 (Transparent mode) the information at **REMIN** is seen at **REMOUT** after a debounce time of 50ms maximum;
- if **RLM** = 1 (Latched Mode) the information stored in bit **RDL** in **CR17** is seen at **REMOUT**. **RDL** is set after a debounce time of 50ms maximum when a low level at **REMIN** is detected. **RDL** is reset with power on initialization and can also be reset writing 0 in bit **RDL**.

The **REMOUT** output polarity can be inverted setting bit **ROI** in **CR17**: the pressed button information is presented at **REMOUT** output as a logic 1 if bit **ROI** = 0. If **ROI** = 1 the polarity is inverted.

III PROGRAMMABLE REGISTERS

Control Register CR0 Functions (Address: 0x00)

7	6	5	4	3	2	1	0	Function	
F(1:0)		VFS	CM	MA	IA	FF	B7		
0 0 1 1	0 1 0 1							MCLK or AUXCLK = 512 kHz MCLK or AUXCLK = 1.536 MHz MCLK or AUXCLK = 2.048 MHz MCLK or AUXCLK = 2.560 MHz	*
		0 1						Voice Data Fs is 8 kHz Voice Data Fs is 16 kHz	*
			0 1					Linear code Companded code	*
								Linear Code	Companded Code
				0 0 1 1	0 1 0 1			2-complement * sign and magnitude 2-complement 1-complement	µ-law: CCITT D3-D4 * µ-law: Bare Coding A-law including even bit inversion A-law: Bare Coding
						0 1		B1 and B2 consecutive (1) * B1 and B2 separated (1)	
							0 1	8 bits time-slot (1) * 7 bits time-slot (1)	

(1): significant in companded mode only
*: state at power on initialization

Control Register CR1 Functions (Address: 0x01)

7	6	5	4	3	2	1	0	Function	
DM(1:0)			MR	MX	EN	TS	DL		
0 1 1	X 0 1							delayed data timing non-delayed normal data timing non-delayed reverse data timing	*
		X							
			0 1					D_R connected to RX path CR2 connected to RX path (1)	*
				0 1				TX path connected to D_X CR3 connected to D_X (1)	*
					0 1			PCM I/F disabled PCM I/F enabled	*
						0 1		B1 channel selected B2 channel selected (1)	*
							0 1	Normal operation Digital Loopback	*

(1) significant in companded mode only
*: state at power on initialization
X: reserved: write 0

Control Register CR2 Functions (Address: 0x02)

7	6	5	4	3	2	1	0	Function
DRD(7:0)								
msb							lsb	Data sent to Receive path or Data received from DR input (1)

(1) Significant in companded mode only.

Control Register CR3 Functions (Address: 0x03)

7	6	5	4	3	2	1	0	Function
DXD(7:0)								
msb							lsb	DX data transmitted (1)

(1) Significant in companded mode only.

Control Register CR4 Functions (Address: 0x04)

7	6	5	4	3	2	1	0	Function
MS(1:0)		MB	PG	TXA(3:0)				
0 0 1 1	0 1 0 1							Transmit input muted * MIC1 Selected MIC2 Selected MIC3 Selected (1)
		0 1						MBIAS output disabled * MBIAS output enabled
			0 1					20dB preamplifier gain * 0dB preamplifier gain (1)
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	0 dB Transmit Amplifier gain (1)* 1.5 dB Transmit Amplifier gain Transmit Amplifier in 1.5 dB step 22.5 dB Transmit Amplifier gain

*: state at power on initialization
(1) When the single ended line input MIC3 is selected, microphone gain must be set to 0dB (PG=1, TXA=0000).

Control Register CR5 Functions (Address: 0x05)

7	6	5	4	3	2	1	0	Function
		HPB	SI	SA(3:0)				
X	X							
		0 1						Voice Codec Receive High Pass filter enabled (1) * Voice Codec Receive High Pass filter disabled
			0 1					Voice Codec internal sidetone disabled * Voice Codec internal sidetone enabled
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	-12.5 dB Sidetone gain * -13.5 dB Sidetone gain Sidetone gain in 1 dB step -27.5 dB Sidetone gain

*: state at power on initialization
X: reserved: write 0
(1): Valid only when Voice Data Fs=8kHz (VFS=0). When Voice data Fs=16kHz (VFS=1) The High Pass Filter is always disabled.

Control Register CR6 Functions (Address: 0x06)

7	6	5	4	3	2	1	0	Function
LAY(1:0)		AFS(1:0)		OS(1:0)		SE	RTE	
0 0 1	0 1 X							Audio Data Fs is 32 or 44.1 or 48 kHz (1) * Audio Data Fs is 16 or 22.025 or 24 kHz. (1) Audio Data Fs is 8 or 11.025 or 12 kHz. (2)
		0 0 1	0 1 X					Audio Data Fs is 44.1 or 22.05 or 11.025 kHz * Audio Data Fs is 48 or 24 or 12 kHz. Audio Data Fs is 32 or 16 or 8 kHz.
				0 0 1 1	0 1 0 1			Output Drivers off * LSP/N output Driver selected. HPL output Driver selected. HPL and HPR output Drivers selected.
						0 1		Audio or Voice Codec Signal to LS or HP disabled * Audio or Voice Codec Signal to LS or HP enabled.
							0 1	Ring/Tone to LS or HP disabled * Ring/Tone to LS or HP enabled.

(1): OCK frequency must be 256 times Audio Data Fs frequency.
(2): OCK frequency must be 512 times Audio Data Fs frequency.
*: state at power on initialization
X: reserved: write 0

Control Register CR7 Functions (Address: 0x07)

7	6	5	4	3	2	1	0	Function
			MUT	LSA(3:0)				
X	X	X						
			0 1					The selected output Drivers are operative * The selected output Drivers are muted
				0 0 - 1	0 0 - 1	0 0 - 1	0 1 - 1	Earpiece/Loudspeaker Amplifier 6 dB gain * Earpiece/Loudspeaker Amplifier 4 dB gain Earpiece/Loudspeaker Amplifier gain in 2 dB step Earpiece/Loudspeaker Amplifier -24 dB gain

*: state at power on initialization
X: reserved: write 0

Control Register CR8 Functions (Address: 0x08)

7	6	5	4	3	2	1	0	Function
			HPLA(4:0)					
X	X	X						
			0 0 - 1	0 0 - 0	0 0 - 1	0 0 - 0	0 1 - 0	Headphones amplifier (Left channel) 0 dB gain * Headphones amplifier (Left channel) -2 dB gain Headphones amplifier (Left channel) gain in 2 dB step Headphones amplifier (Left channel) -40 dB gain

*: state at power on initialization
X: reserved: write 0

Control Register CR9 Functions (Address: 0x09)

7	6	5	4	3	2	1	0	Function	
			HPRA(4:0)						
X	X	X							
			0	0	0	0	0	Headphones amplifier (Right channel) 0 dB gain	*
			0	0	0	0	1	Headphones amplifier (Right channel) -2 dB gain	
			-	-	-	-	-	Headphones amplifier (Right channel) gain in 2 dB step	
			1	0	1	0	0	Headphones amplifier (Right channel) -40 dB gain	

*: state at power on initialization
X: write 0

Control Register CR10 Functions (Address: 0x0A)

7	6	5	4	3	2	1	0	Function	
			FMLA(4:0)						
X	X	X							
			0	0	0	0	0	FM Preamplifier (Left channel) +18 dB gain	*
			0	0	0	0	1	FM Preamplifier (Left channel) +16 dB gain	
			-	-	-	-	-	FM Preamplifier (Left channel) gain in 2 dB step	
			1	0	0	1	1	FM Preamplifier (Left channel) -20 dB gain	

*: state at power on initialization
X: reserved: write 0

Control Register CR11 Functions (Address: 0x0B)

7	6	5	4	3	2	1	0	Function	
			FMRA(4:0)						
X	X	X							
			0	0	0	0	0	FM Preamplifier (Right channel) +18 dB gain	*
			0	0	0	0	1	FM Preamplifier (Right channel) +16 dB gain	
			-	-	-	-	-	FM Preamplifier (Right channel) gain in 2 dB step	
			1	0	0	1	1	FM Preamplifier (Right channel) -20 dB gain	

*: state at power on initialization
X: reserved: write 0

Control Register CR12 Functions (Address: 0x0C)

7	6	5	4	3	2	1	0	Function
TONEG(3:0)				FSEL(1:0)		SN	DE	
0 0 - 1	0 0 - 0	0 0 - 1	0 1 - 1					Tone gain is 0 dB * Tone gain is -3 dB Tone gain in 3 dB step Tone gain is -33 dB
				0 0 1 1	0 1 0 1			f1 and f2 muted * f1 selected f2 selected f1 and f2 in summed mode
						0 1		Squarewave signal selected * Sinewave signal selected
							0 1	Tone/Ring Generator not connected to Transmit path * Tone/Ring Generator connected to Transmit path

*: state at power on initialization
X: reserved write 0

Control Register CR13 Functions (Address: 0x0D)

7	6	5	4	3	2	1	0	Function
F1(7:0)								
msb							lsb	Binary equivalent of the decimal number used to calculate f1 See Table 1

Control Register CR14 Functions (Address: 0x0E)

7	6	5	4	3	2	1	0	Function
F2(7:0)								
msb							lsb	Binary equivalent of the decimal number used to calculate f2 See Table 1

Control Register CR15 Functions (Address: 0x0F)

7	6	5	4	3	2	1	0	Function
BE	BI	BZ(5:0)						
0 1								Buzzer output disabled (set to 0) * Buzzer output enabled
	0 1							Duty Cycle is intended as the relative width of logic 1 * Duty cycle is intended as the relative width of logic 0
		msb					lsb	Binary equivalent of the decimal number used to calculate the duty cycle, using the formula: DutyCycle = BZ(5:0) x 0.78125 %

* state at power on initialization

Control Register CR16 Functions (Address: 0x10)

7	6	5	4	3	2	1	0	Function
POL	ORD	DIF	INV	FOR	SCL	PREC(1:0)		
0								OCK polarity, SCK changes on the rising edge of OCK *
1								OCK polarity, SCK changes on the falling edge of OCK
	0							Audio I/F data order, the MSB is received first (I^2S) *
	1							Audio I/F data order, the LSB is received first
		0						Audio I/F data alignment, the word is left justified (I^2S)(1) *
		1						Audio I/F data alignment, the word is right justified (1)
			0					LRCK polarity, when LRCK=0 Left data is received (I^2S) (2) *
			1					LRCK polarity, when LRCK=1 Left data is received (2)
				0				Audio I/F format, I^2S format (first bit is delayed) (3) *
				1				Audio I/F format, non delayed formats
					0			SCK polarity, SDI and LRCK sampled on the rising edge (I^2S) *
					1			SCK polarity, SDI and LRCK sampled on the falling edge
						0	0	Audio I/F data width 16 bit (32 SCK clocks per frame) *
						0	1	Audio I/F data width 18 bit (64 SCK clocks per frame)
						1	0	Audio I/F data width 20 bit (64 SCK clocks per frame)
						1	1	Audio I/F data width 24 bit (64 SCK clocks per frame)

(1) significant in 18/20/24 bit per word mode only
(2) Left Channel data is always received first.
(3) First bit delay, in 18/20/24 bit per word mode, is applied only if word is left justified.
*: state at power on initialization

Control Register CR17 Functions (Address: 0x11)

7	6	5	4	3	2	1	0	Function
REN	RLM	ROI	RDL					
0								Remocon Function disabled *
1								Remocon Function enabled
	0							Remocon output in transparent mode *
	1							Remocon output in latched mode
		0						Remocon output not inverted *
		1						Remocon output inverted
			0					Remocon detection latch reset by µP *
			1					Remocon detection latch set by internal logic
				X	X	X	X	

*: state at power on initialization
X: reserved write 0

Control Register CR18 Functions (Address: 0x12)

7	6	5	4	3	2	1	0	Function
MD(1:0)		CFM(1:0)				SRS	PU	
0 0 1 1	0 1 0 1							Voice Mode * Audio Mode. Tone Only Mode. FM Mode.
		0 0 1	0 1 X					The Master Clock Input for Tone Only and FM Mode is AUXCLK* The Master Clock Input for Tone Only and FM Mode is MCLK The Master Clock Input for Tone Only and FM Mode is OCK
				X				
					X			
						0 1		Normal Operation * Software Reset, all registers are set to their default.
							0 1	Device is in Power Down * Device is in Power Up

*: state at power on initialization
X: reserved write 0

Table 1. Tone Generator frequency versus CR13 CR14 register value correspondence table

CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)	CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)	CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)	CR13/14 Value (dec.)	F1/F2 Tone Frequency (Hz)
0	0.0	64	250.0	128	750.0	192	1750.0
1	3.9	65	257.8	129	765.6	193	1781.2
2	7.8	66	265.6	130	781.2	194	1812.5
3	11.7	67	273.4	131	796.9	195	1843.8
4	15.6	68	281.2	132	812.5	196	1875.0
5	19.5	69	289.1	133	828.1	197	1906.2
6	23.4	70	296.9	134	843.8	198	1937.5
7	27.3	71	304.7	135	859.4	199	1968.8
8	31.2	72	312.5	136	875.0	200	2000.0
9	35.2	73	320.3	137	890.6	201	2031.2
10	39.1	74	328.1	138	906.2	202	2062.5
11	43.0	75	335.9	139	921.9	203	2093.8
12	46.9	76	343.8	140	937.5	204	2125.0
13	50.8	77	351.6	141	953.1	205	2156.2
14	54.7	78	359.4	142	968.8	206	2187.5
15	58.6	79	367.2	143	984.4	207	2218.8
16	62.5	80	375.0	144	1000.0	208	2250.0
17	66.4	81	382.8	145	1015.6	209	2281.2
18	70.3	82	390.6	146	1031.2	210	2312.5
19	74.2	83	398.4	147	1046.9	211	2343.8
20	78.1	84	406.2	148	1062.5	212	2375.0
21	82.0	85	414.1	149	1078.1	213	2406.2
22	85.9	86	421.9	150	1093.8	214	2437.5
23	89.8	87	429.7	151	1109.4	215	2468.8
24	93.8	88	437.5	152	1125.0	216	2500.0
25	97.7	89	445.3	153	1140.6	217	2531.2
26	101.6	90	453.1	154	1156.2	218	2562.5
27	105.5	91	460.9	155	1171.9	219	2593.8
28	109.4	92	468.8	156	1187.5	220	2625.0
29	113.3	93	476.6	157	1203.1	221	2656.2
30	117.2	94	484.4	158	1218.8	222	2687.5
31	121.1	95	492.2	159	1234.4	223	2718.8
32	125.0	96	500.0	160	1250.0	224	2750.0
33	128.9	97	507.8	161	1265.6	225	2781.2
34	132.8	98	515.6	162	1281.2	226	2812.5
35	136.7	99	523.4	163	1296.9	227	2843.8
36	140.6	100	531.2	164	1312.5	228	2875.0
37	144.5	101	539.1	165	1328.1	229	2906.2
38	148.4	102	546.9	166	1343.8	230	2937.5
39	152.3	103	554.7	167	1359.4	231	2968.8
40	156.2	104	562.5	168	1375.0	232	3000.0
41	160.2	105	570.3	169	1390.6	233	3031.2
42	164.1	106	578.1	170	1406.2	234	3062.5
43	168.0	107	585.9	171	1421.9	235	3093.8
44	171.9	108	593.8	172	1437.5	236	3125.0
45	175.8	109	601.6	173	1453.1	237	3156.2
46	179.7	110	609.4	174	1468.8	238	3187.5
47	183.6	111	617.2	175	1484.4	239	3218.8
48	187.5	112	625.0	176	1500.0	240	3250.0
49	191.4	113	632.8	177	1515.6	241	3281.2
50	195.3	114	640.6	178	1531.2	242	3312.5
51	199.2	115	648.4	179	1546.9	243	3343.8
52	203.1	116	656.2	180	1562.5	244	3375.0
53	207.0	117	664.1	181	1578.1	245	3406.2
54	210.9	118	671.9	182	1593.8	246	3437.5
55	214.8	119	679.7	183	1609.4	247	3468.8
56	218.8	120	687.5	184	1625.0	248	3500.0
57	222.7	121	695.3	185	1640.6	249	3531.2
58	226.6	122	703.1	186	1656.2	250	3562.5
59	230.5	123	710.9	187	1671.9	251	3593.8
60	234.4	124	718.8	188	1687.5	252	3625.0
61	238.3	125	726.6	189	1703.1	253	3656.2
62	242.2	126	734.4	190	1718.8	254	3687.5
63	246.1	127	742.2	191	1734.4	255	3718.8

TIMING DIAGRAM

Figure 1. Voice Interface (PCM I/F) Non Delayed Data Timing Mode (*)

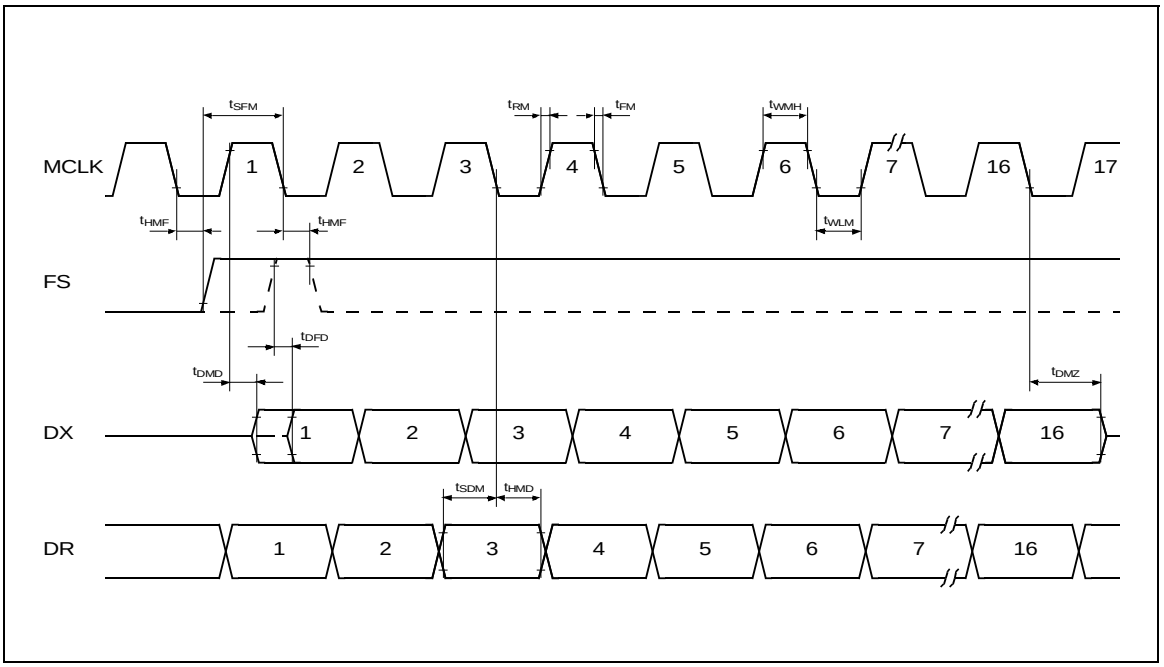
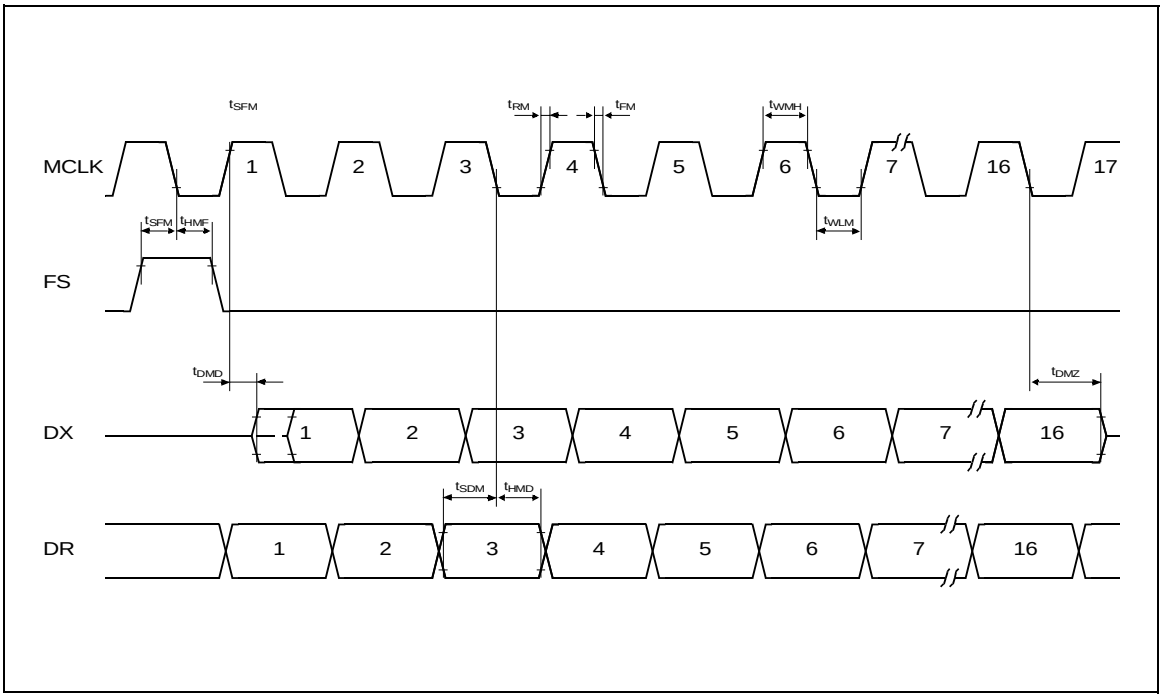


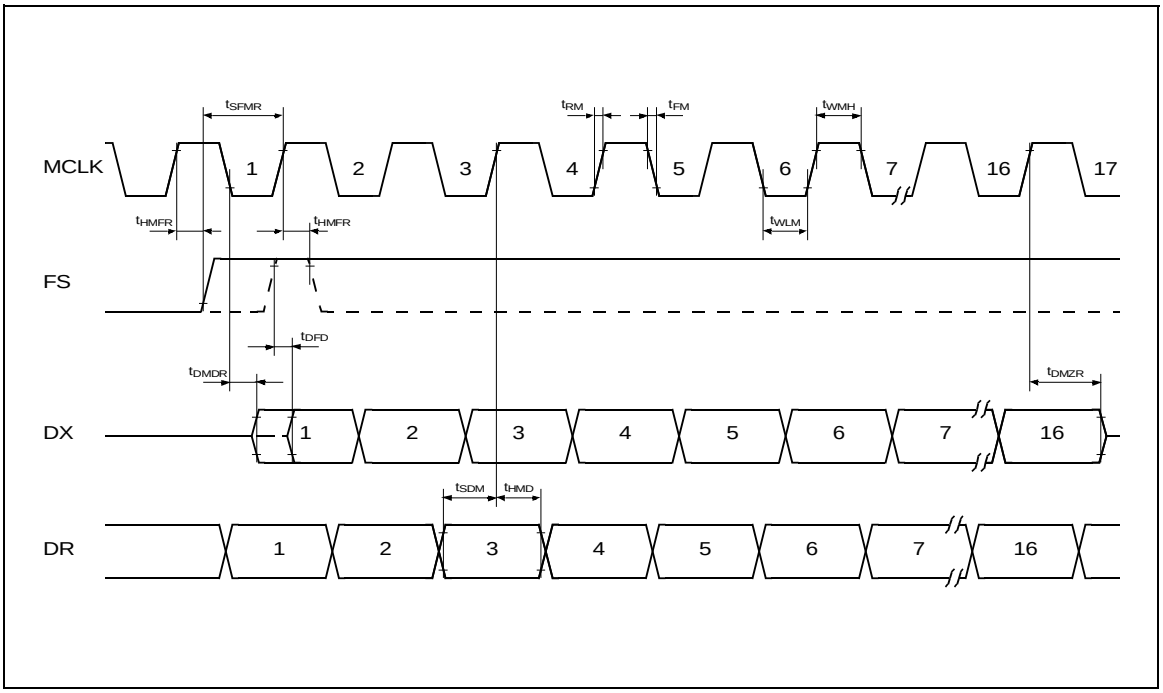
Figure 2. Voice Interface (PCM I/F) Delayed Data Timing Mode (*)



(*) In the case of companded code the timing is applied to 8 bits instead of 16 bits.

TIMING DIAGRAM

Figure 3. Voice Interface (PCM I/F) Non Delayed Reverse Data Timing Mode (*)



(*) In the case of companded code the timing is applied to 8 bits instead of 16 bits.

Figure 4. Audio Interface (I^2S I/F) Timing

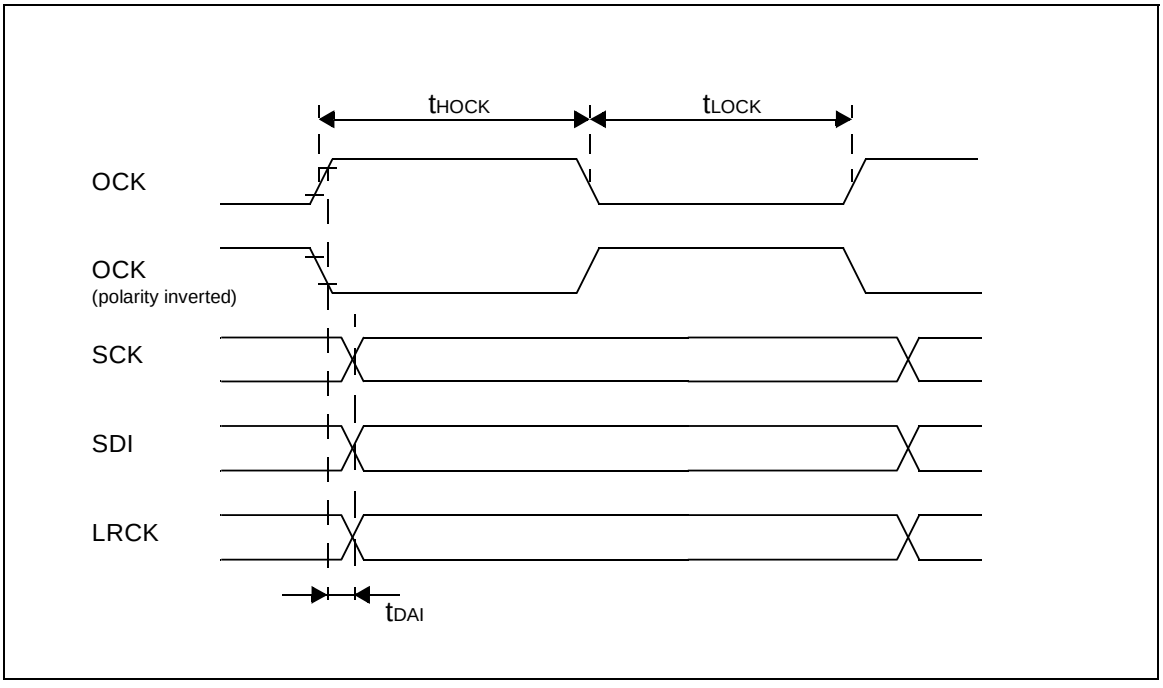
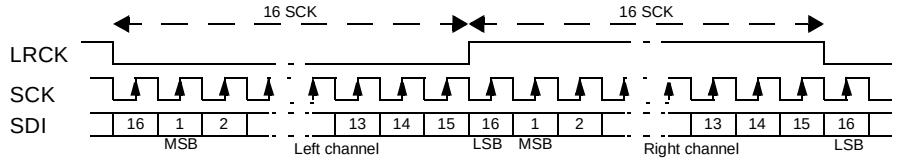
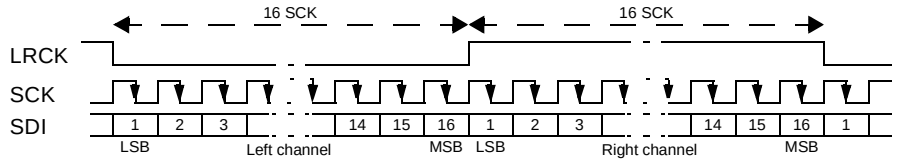


Figure 5. Audio Interface (I^2S I/F) Formats

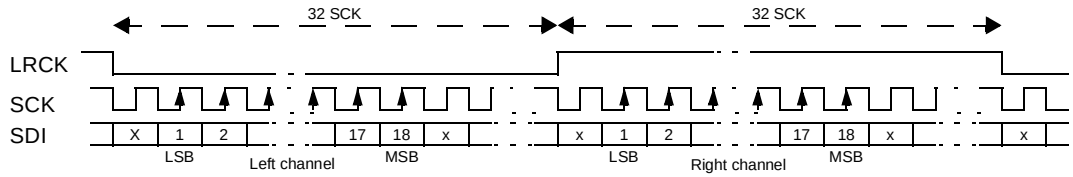
I^2S Format (delayed), Data word 16 bit, MSB first (default)



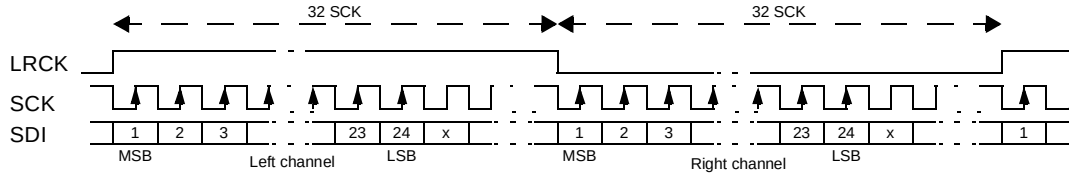
Non-delayed Format, SCK polarity inverted, Data word 16 bit, LSB first



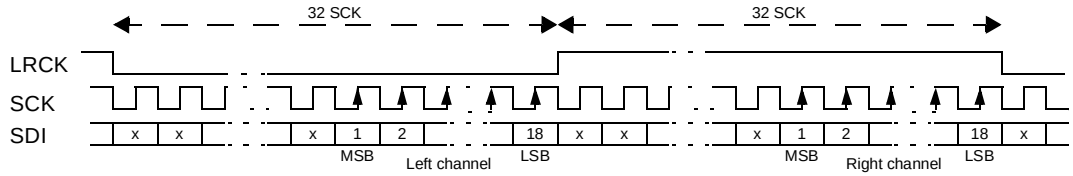
I^2S Format (delayed), Data word 18 bit, Left justified, LSB first



Non-delayed Format, Data word 24 bit, Left justified, MSB first, LRCK polarity inverted



Data word 18 bit, Right justified, MSB first



For the other possible formats see Control Register **CR16** description

Figure 6. Control Interface (I^2C I/F) formats

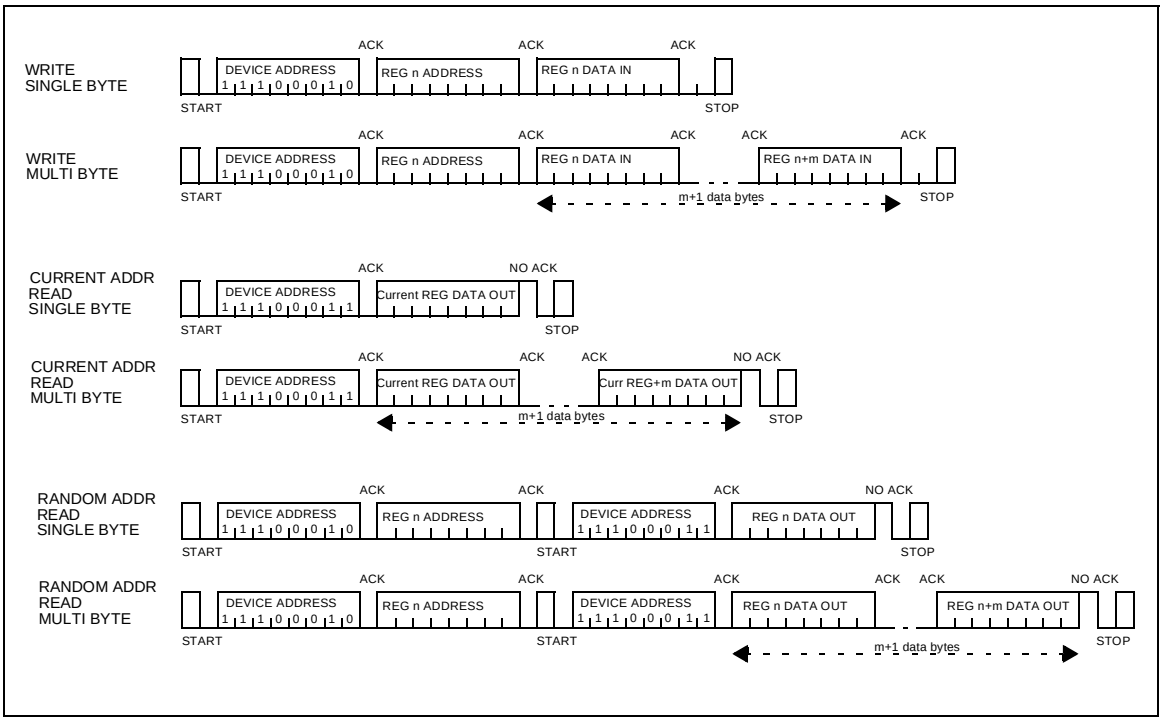


Figure 7. Control Interface (I^2C I/F) Timing

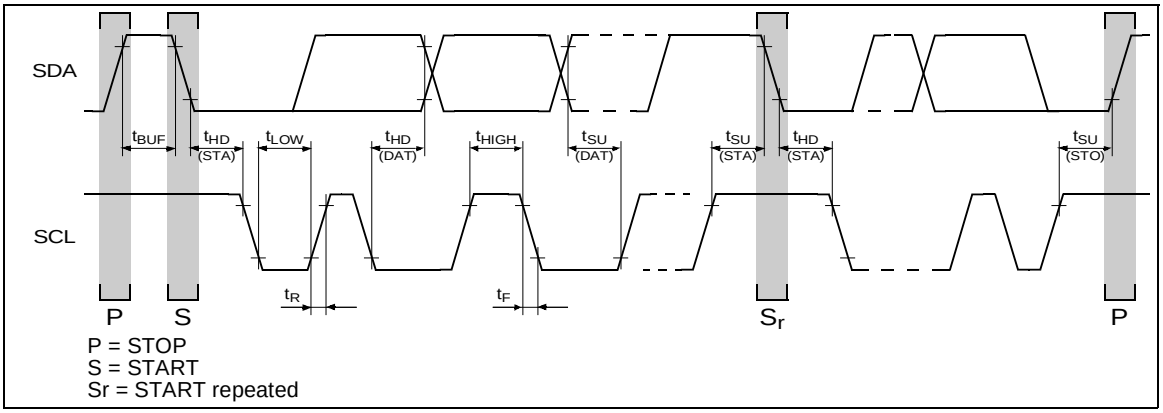
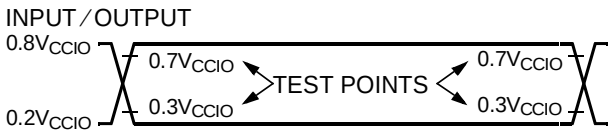


Figure 8. A.C. TESTING INPUT, OUTPUT WAVEFORM



AC Testing: inputs are driven at 0.8VCCIO for a logic "1" and 0.2VCCIO for a logic "0".
Timing measurements are made at 0.7VCCIO for a logic "1" and 0.3VCCIO for a logic "0".

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	4.6	V
Voltage at MIC ($V_{CC} \leq 3.3V$)	V_{CC} +0.5 to GND -0.5	V
Current at LSP/N	± 240	mA
Current at HPR,HPL	± 100	mA
Current at any digital output	± 50	mA
Voltage at any digital input ($V_{CCIO} \leq 3.3V$); limited at ± 50mA	V_{CCIO} + 0.5 to GND -0.5	V
Storage temperature range	- 65 to + 150	°C

OPERATIVE SUPPLY VOLTAGES

Symbol	Min.	Max.	Unit
$V_{CC} = V_{CCA} = V_{CCP}$	2.7	3.3	V
V_{CCIO}	1.8	V_{CC}	V

TIMING SPECIFICATIONS (unless otherwise specified, V_{CCIO} = 1.8V to 3.3V,T_{amb} = -30°C to 85°C; typical characteristics are specified at V_{CCIO} = 3.0V, T_{amb} = 25 °C; all signals are referenced to GND, see next Note for timing definitions)

NOTICE: All timing specifications subject to change.

OCK and Audio Interface Signals Timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{OCK}	Frequency of OCK (frequency depends on the selected Audio sample rate in **CR6**)	Audio Fs 8kHz or 16kHz Audio Fs 11.025kHz or 22.05kHz Audio Fs 12kHz or 24kHz Audio Fs 32kHz Audio Fs 44.1kHz Audio Fs 48kHz		4.096 5.6648 6.144 8.192 11.2896 12.288		MHz MHz MHz MHz MHz MHz
t_{HOCK}	Period of OCK high	Measured from V_{IH} to V_{IH}	35			ns
t_{LOCK}	Period of OCK low	Measured from V_{IL} to V_{IL}	35			ns
t_{DAI}	Delay of SCK,SDI and LRCK from OCK active edge		0		20	ns

MCLK and AUXCLK Timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK, AUXCLK	Frequency is programmable with bits **F** in **CR0**		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK, AUXCLK high	Measured from V_{IH} to V_{IH}	150			ns
t_{WML}	Period of MCLK, AUXCLK low	Measured from V_{IL} to V_{IL}	150			ns
t_{RM}	Rise Time of MCLK, AUXCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK, AUXCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM Interface Timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		10			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 20pF			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		10		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 20pF; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, DR valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to DR invalid		10			ns
t_{HMFR}	Hold Time MCLK High to FS low		30			ns
t_{SFMR}	Setup Time, FS high to MCLK High		30			ns
t_{DMDR}	Delay Time, MCLK low to data valid	Load = 20pF			100	ns
t_{DMZR}	Delay Time, MCLK High to DX disabled		10		100	ns
t_{HMDR}	Hold Time, MCLK High to DR invalid		20			ns

I^2C Bus Control Port Timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Clock Frequency				400	kHz
t_{HIGH}	Clock High Time		600			ns
t_{LOW}	Clock Low Time		1300			ns
t_R	SDA and SCL Rise Time				1000	ns
t_F	SDA and SCL Fall Time				300	ns
$t_{HD:STA}$	Start Condition Hold Time		600			ns
$t_{SU:STA}$	Start Condition Setup Time		600			ns
$t_{HD:DAT}$	Data Input Hold Time		0			ns
$t_{SU:DAT}$	Data Input Setup Time		250			ns
$t_{SU:STO}$	Stop Condition Setup Time		600			ns
t_{BUF}	Bus Free Time		1300			ns

Note:

A signal is valid if it is above VIH or below VIL and invalid if it is between VIL and VIH.For the purpose of this specification the following conditions apply (see Fig. 8):

a) All input signal are defined as: VIL = 0.2VCCIO, VIH = 0.8VCCIO, tR < 10ns, tF < 10ns.

b) Delay times are measured from the inputs signal valid to the output signal valid.

c) Setup times are measured from the data input valid to the clock input invalid.

d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CCIO} = 1.8V to 3.3V, T_{amb} = -30°C to 85°C; typical characteristic are specified at V_{CCIO} = 3.0V, T_{amb} = 25°C; all signals are referenced to GND)

Digital Interfaces (See Figure 8)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs except REMIN	DC AC			$0.3V_{CCIO}$ $0.2V_{CCIO}$	V V
V_{IH}	Input High Voltage	All digital inputs except REMIN	DC AC	$0.7V_{CCIO}$ $0.8V_{CCIO}$			V V
V_{ILREM}	Input Low Voltage	REMIN input				0.5	V
V_{IHREM}	Input High Voltage	REMIN input		1.4			V
V_{OL}	Output Low Voltage	All digital outputs, I_L = 10µA All digital outputs, I_L = 2mA				0.1 0.4	V V
V_{OH}	Output High Voltage	All digital outputs, IL = 10µA All digital outputs, IL = 2mA		V_{CCIO}-0.1 V_{CCIO}-0.4			V V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}		-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CCIO}		-10		10	µA
I_{OZ}	Output Current in High impedance (Tristate)	DX and CO		-10		10	µA

Analog Interfaces

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{MBIAS}	MBIAS Output Resistance	MBIAS 100mV under V_{CC}			150	Ω
I_{MIC}	MIC Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	MIC Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{FM}	FM Input Resistance	FML, FMR to CAP2	30			kΩ
R_{LHP}	Single Ended Drivers Load Resistance	HPL, HPR to GNDP	30			Ω
C_{LHP}	Single Ended Drivers Load Capacitance	HPL, HPR to GNDP		100 50*		pF nF
R_{OVHP}	Single Ended Drivers Output Resistance	Steady zero PCM code applied to DR; I = ±1mA		1		Ω
R_{LLS}	Differential Driver Load Resistance	LSP to LSN	8			Ω
C_{LLS}	Differential Driver Load Capacitance	LSP to LSN		100 50*		pF nF
R_{OLS}	Differential Driver Output Resistance	Steady zero PCM code applied to DR; I = ±1mA		1		Ω
V_{OSLS}	Differential offset Voltage at LSP, LSN	Alternating ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	-50		+50	mV

* with series resistor

ANALOG INPUT/OUTPUT OPERATIVE RANGES

Microphone Input Levels - Absolute levels at MIC1, MIC2

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBm0 level	Transmit gain 0dB		493		mV_{RMS}
	Overload level	Transmit gain 0dB		707 2		mV_{RMS} V_{pp}
	0 dBm0 level	Transmit gain 20dB		49		mV_{RMS}
	Overload level	Transmit gain 20dB		71 200		mV_{RMS} mV_{pp}
	0 dBm0 level	Transmit gain 42.5dB		3.7		mV_{RMS}
	Overload level	Transmit gain 42.5dB		5.3 15		mV_{RMS} mV_{pp}

Line Input Level - Absolute levels at MIC3

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Overload level	Transmit gain 0dB		354 1		mV_{RMS} V_{pp}

FM Input Levels - Absolute levels at FML, FMR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Overload level	FML, FMR gain 18 dB		177 0.5		mV_{RMS} V_{pp}
	Overload level	FML, FMR gain from 6 to -20dB		707 2		mV_{RMS} V_{pp}

Power Output Levels - Absolute levels at HPL, HPR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Maximum undistorted level	30Ω Load	707 2			mV_{RMS} V_{pp}

Power Output Levels - Absolute levels at LSP-LSN (Differentially measured)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	0 dBm0 level	LS gain 0dB		984		mV_{RMS}
	0 dBm0 level	LS gain -24dB		62.1		mV_{RMS}
	Maximum undistorted level	8Ω Load	1.06 3			V_{RMS} V_{pp}

Tones Levels

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Tone level at LSP-LSN	Single tone, sinusoidal waveform, tone gain 0dB, LS gain 0dB		1.41 4		V_{RMS} V_{pp}
	Tone level at HPL, HPR	Single tone, sinusoidal waveform, tone gain 0dB, HPL, HPR gain -6dB		707 2		mV_{RMS} V_{pp}
	Tone level at DX	Voice mode, Single tone, sinusoidal waveform, tone gain 0dB		-1.64		dBFS

Note: when 2 tones are enabled the amplitude of f1 is lowered by 5dB and the amplitude of f2 is lowered by 7dB with respect to the amplitude of a single tone.

VOICE CODEC CHARACTERISTICS (unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C; FS Frequency = 8kHz; typical characteristics are specified at V_{CC} = 3.0V, T_{amb} = 25°C, MIC1/2 = 0dBm0, DR = -6dBm0 PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE

Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for minimum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at DX	-0.5		0.5	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog.} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Minimum gain	-0.1		0.1	dB
G_{XAF8}	Transmit Gain Variation with frequency. FS Frequency = 8kHz (VFS=0)	Digital filter characteristics f = 60 Hz f = 100 Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz (*) f = 8000 Hz (*)	 -1.5 -0.5 -1.5 		 -30 -20 -6 0.5 0.5 0.0 -14 -35 -47	 dB dB dB dB dB dB dB dB dB
G_{XAF16}	Transmit Gain Variation with frequency. FS Frequency = 16kHz (VFS=1)	Digital filter characteristics f = 100 Hz f = 200 Hz to 6000 Hz f = 6800 Hz f = 8000 Hz f = 9200 Hz (*) f = 16000 Hz (*)	 -1.5 -0.5 -1.5 		 0.5 0.5 0.0 -14 -35 -47	 dB dB dB dB dB dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = -10 dBm0 V_{MIC} = -40 dBm0 to +3 dBm0 V_{MIC} = -50 dBm0 to -40 dBm0 V_{MIC} = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB

(*) The limit at frequencies between 4600Hz and 8000Hz lies on a straight line connecting the two frequencies on a linear (dB) scale versus log (Hz) scale.

AMPLITUDE RESPONSE (continued)

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAHPL} G_{RAHPR} G_{RALS}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply -6 dBm0 PCM code to DR Measure HPL, HPR, LSP-LSN	-0.5		0.5	dB
G_{RAGHPL} G_{RAGHPR} G_{RAGLS}	Receive Gain Variation with programmed gain	Measure HPL, HPR, LSP-LSN Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to G_{RA}, i.e. $G_{RAGLS} = G_{actual} - G_{prog.} - G_{RALS}$	-0.5		0.5	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (HPL, HPR and LSP-LSN) min. gain < G_R < Max. gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (HPL, HPR and LSP-LSN) G_R = Maximum Gain	-0.1		0.1	dB
G_{RAF8}	Receive Gain Variation with frequency (HPL, HPR and LSP-LSN) FS frequency = 8kHz (VFS=0). High Pass Filter enabled (HPB = 0).	Digital filter characteristics f = 60Hz f = 100Hz f = 200 Hz f = 300 Hz f = 400 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 -20 -12 -2 0.5 0.5 0.0 -14	 dB dB dB dB dB dB dB
	Receive Gain Variation with frequency (HPL, HPR and LSP-LSN) FS frequency = 8kHz (VFS=0). High Pass Filter disabled (HPB = 1).	Digital filter characteristics f = 50Hz f = 100 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14	 dB dB dB dB
G_{RAF16}	Receive Gain Variation with frequency (HPL, HPR and LSP-LSN) FS frequency = 16kHz (VFS=1).	Digital filter characteristics f = 100Hz f = 200 Hz to 6000 Hz f = 6800 Hz f = 8000 Hz	 -1.5 -0.5 -1.5		 0.5 0.5 0.0 -14	 dB dB dB dB
G_{RALHPL} G_{RALHPR} G_{RALLS}	Receive Gain Variation with signal level (HPL, HPR and LSP-LSN)	Sinusoidal Test Method Reference Level = -10 dBm0 DR = -40 dBm0 to -3 dBm0 DR = -50 dBm0 to -40 dBm0 DR = -55 dBm0 to -50 dBm0	 -0.5 -0.5 -1.2		 0.5 0.5 1.2	 dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		290 180 50 20 55 80 180		µs µs µs µs µs µs µs
DRA	Rx Delay, Absolute	f = 1600 Hz		280		µs
DRR	Rx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		200 110 50 20 65 100 220		µs µs µs µs µs µs µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXP	Tx Noise, P weighted (up to 35dB)	V_{MIC} = 0V, DE = 0		-75	-70	dBm0p
NRP	Rx Noise, C-message weighted 8Ω Load (gain for max. undistorted output level)	Receive PCM code = Zero, SI = 0, RTE = 0 and LSA='0100' (gain -2dB)		30	50	μV_{RMS}
PSRTX	PSRR, Tx	MIC = 0V, V_{CC} = 3.0 V_{DC} + 50 mV_{RMS}; f = 100Hz to 50kHz	30			dB
PSRRX	PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 3.0V_{DC} + 50 mV_{RMS} f = 100 Hz - 4 kHz f = 4 kHz - 50 kHz	 30 30			 dB dB
SOS	Spurious Out-Band signal at the output	Digital filter characteristics 4600 Hz - 5600 Hz 5600 Hz - 7600 Hz 7600 Hz - 8400 Hz			 -40 -50 -50	 dB dB dB

CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CT_{X-R}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = Quiet PCM Code		-100	-65	dB
CT_{R-X}	Receive to Transmit	Receive Level = -6 dBm0, f = 300 - 3400 Hz MIC = 0V		-80	-65	dB

DISTORTION Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDRLS} (*)	Signal to Total Distortion (LSP-LSN) (up to 14dB attenuation) 8Ω Load Typical values are measured with 14dB attenuation.	Sinusoidal Test Method (measured using linear 300 Hz to 3400 Hz weighting, FS=8kHZ)				
		Level = +3 dBm0		77		dB
		Level = -6 dBm0	65	70		dB
		Level = -10 dBm0	62	67		dB
		Level = -20 dBm0	54	59		dB
		Level = -30 dBm0	44	49		dB
		Level = -40 dBm0	34	39		dB
		Level = -45 dBm0	29	34		dB
		Level = -55 dBm0	19	24		dB
	Signal to Total Distortion (LSP-LSN) (up to 14dB attenuation) 8Ω Load Typical values are measured with 14dB attenuation.	Sinusoidal Test Method (measured using linear 300 Hz to 6800 Hz weighting, FS=16kHZ)				
		Level = +3 dBm0		74		dB
		Level = -6 dBm0		67		dB
		Level = -10 dBm0		64		dB
		Level = -20 dBm0		56		dB
		Level = -30 dBm0		46		dB
		Level = -40 dBm0		36		dB
		Level = -45 dBm0		31		dB
		Level = -55 dBm0		21		dB
	Signal to Total Distortion (HPL, HPR) (up to 14dB attenuation) Typical values are measured with 14dB attenuation	Sinusoidal Test Method (measured using linear 300 Hz to 3400 Hz weighting, FS=8kHZ)				
		Level = +3 dBm0		74		
		Level = -6 dBm0		67		dB
		Level = -10 dBm0		64		dB
		Level = -20 dBm0		56		dB
		Level = -30 dBm0		46		dB
		Level = -40 dBm0		36		dB
		Level = -45 dBm0		31		dB
		Level = -55 dBm0		21		dB
	Signal to Total Distortion (HPL, HPR) (up to 14dB attenuation) Typical values are measured with 14dB attenuation	Sinusoidal Test Method (measured using linear 300 Hz to 6800 Hz weighting, FS=16kHZ)				
		Level = +3 dBm0		71		
		Level = -6 dBm0		64		dB
		Level = -10 dBm0		61		dB
		Level = -20 dBm0		53		dB
		Level = -30 dBm0		43		dB
		Level = -40 dBm0		33		dB
		Level = -45 dBm0		28		dB
		Level = -55 dBm0		17		dB

(*) The limit curve shall be determined by straight lines joining successive coordinates given in the table.

DISTORTION Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDX} (*)	Signal to Total Distortion (up to 35dB gain) FS frequency = 8kHz.	Sinusoidal Test Method (measured using linear 300 Hz to 3400 Hz weighting) FSS = 0				
		Level = +3 dBm0		75		dB
	Typical values are measured with 30.5dB gain	Level = 0 dBm0	68	73		dB
		Level = -6 dBm0	64	68		dB
		Level = -10 dBm0	59	64		dB
		Level = -20 dBm0	49	54		dB
		Level = -30 dBm0	40	44		dB
		Level = -40 dBm0	30	34		dB
		Level = -45 dBm0	25	29		dB
		Level = -55 dBm0	15	19		dB
	Signal to Total Distortion FS frequency = 16kHz.	Sinusoidal Test Method (measured using linear 300 Hz to 6800 Hz weighting) FSS = 1				
	Typical values are measured with 30.5dB gain	Level = +3 dBm0		72		dB
		Level = 0 dBm0		70		dB
		Level = -6 dBm0		65		dB
		Level = -10 dBm0		61		dB
		Level = -20 dBm0		51		dB
		Level = -30 dBm0		41		dB
		Level = -40 dBm0		31		dB
		Level = -45 dBm0		26		dB
		Level = -55 dBm0		16		dB

(*) The limit curve shall be determined by straight lines joining successive coordinates given in the table.

STEREO AUDIO DAC and FM CHARACTERISTICS (Unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C; typical characteristics are specified at V_{CC} = 3V, T_{amb} = 25°C; OCK = 12.288MHz; Full-Scale Input Sine Waves, 1015.625Hz; Input Sample Rate (Fs) = 48kHz; Input Data = 18Bits; SCK = 3.072 MHz; Measurement Bandwidth is 20Hz to 20kHz, unweighted. Resistive load on HPL, HPR = 30Ω)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
N	Resolution (*)				18	Bits
DYNR	Dynamic Range	A-weighted	89	92		dB
THDL	Total Harmonic Distortion maximum load	$2V_{pp}$ output HPL, HPR gain set to -6dB 30Ω load		0.01	0.03	%
THD	Total Harmonic Distortion	$2V_{pp}$ output HPL, HPR gain set to -6dB 1kΩ load		0.004		%
	Deviation from Linear Phase (*)	Measurement Bandwidth 20Hz to 20kHz, Fs= 48kHz.Combined digital and analog filter characteristics.			1	°
f_{PB}	Passband (*)	Combined Digital and Analog filter characteristics.	0		0.45Fs	kHz
	Passband Ripple (*)	Combined Digital and Analog filter characteristics.			0.2	dB
f_{SB}	StopBand (*)	Combined Digital and Analog filter characteristics.	0.55Fs			kHz
	StopBand Attenuation (*)	Combined Digital and Analog filter characteristics. Measurement Bandwidth up to 3.45Fs	50			dB
TSF	Transient suppression filter cutoff frequency			20		Hz
	Out Of Band Noise	Measurement Bandwidth 20kHz to 100kHz. Zero input signal		-90		dBr
t_{gd}	Group Delay (*)			0.4		ms
	Interchannel Isolation (*)	HPR, HPL unloaded		100		dB
	Interchannel Gain Mismatch				0.2	dB
	Gain Error				0.5	dB
SUT	Startup Time from Power Up				11	ms

(*) Valid for I^2S input (Audio Mode).

NOTE: Fs range: 8kHz - 48kHz.

POWER DISSIPATION (Unless otherwise specified, V_{CC} = 2.7V to 3.3V, T_{amb} = -30°C to 85°C, LSP, LSN and HPL, HPR outputs not loaded; typical characteristics are specified at V_{CC} = 3V, T_{amb} = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current, REMOCON off	SDA, SCL= V_{CCIO}-0.1V REMOCON function disabled (REN = 0)		0.4		µA
I_{CC0R}	Power down Current, REMOCON on	SDA, SCL= V_{CCIO}-0.1V REMOCON function enabled (REN = 1) REMIN = V_{ILREM} or REMIN = V_{IHREM}		2		µA
I_{CC1}	Power Up Current in Voice Codec Mode	Fs=8kHz. LSP/N output selected		4	6	mA
I_{CC2}	Power Up Current in Stereo Audio Mode	Fs=48kHz. HPL,HPR outputs selected		5	8	mA
I_{CC3}	Power Up Current in FM Stereo Mode	HPL,HPR outputs selected		2	3	mA

TYPICAL PERFORMANCE CHARACTERISTICS

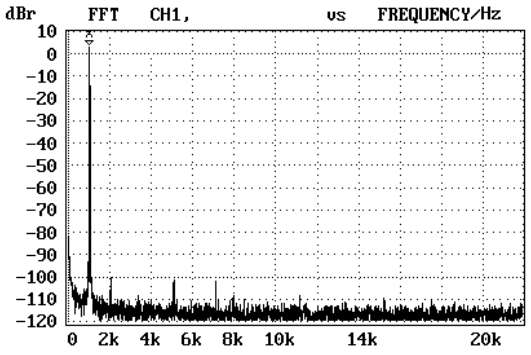


Figure 1. Stereo DAC performance
FFT audio mode (8192 points). Full scale input/output sinewave at 1 kHz (+3dBr)
VCC=2.7V, Fs=48kHz, 18 bits input word.

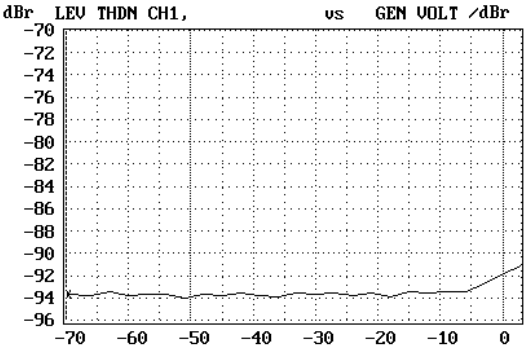


Figure 2. Stereo DAC performance
Dynamic range: Noise + THD [dBr] versus signal amplitude [dBm0]
VCC=2.7V, Fs=48kHz, 18 bits input word.

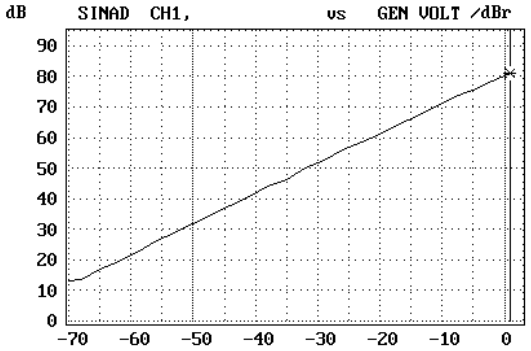


Figure 3. Voice RX performance
S/(N+THD) [dB] versus signal amplitude [dBm0] with 8Ω output load
VCC=2.7V, Fs=8kHz

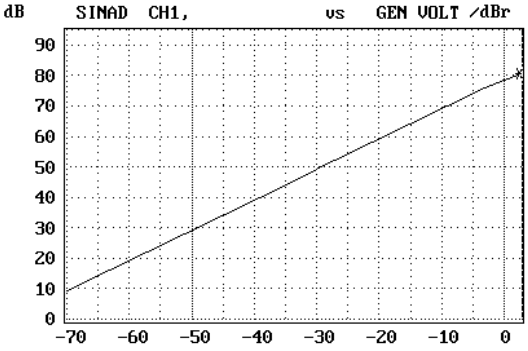


Figure 4. Voice TX performance
S/(N+THD) versus signal amplitude
VCC=2.7V, Fs=8kHz

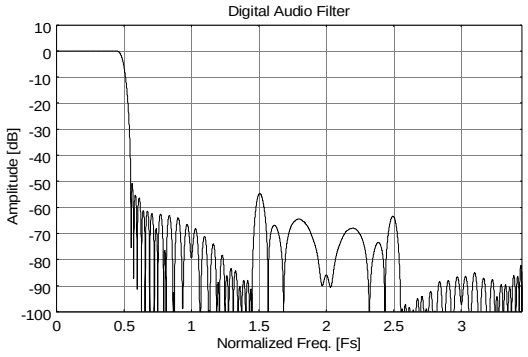


Figure 5. Digital Audio Filter characteristic
Frequency response up to 3.45 Fs

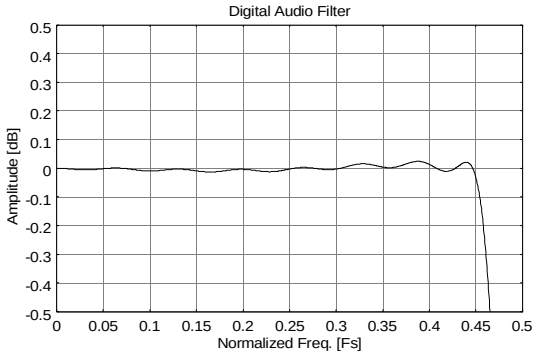


Figure 6. Digital Audio Filter characteristic
In band Frequency response

TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

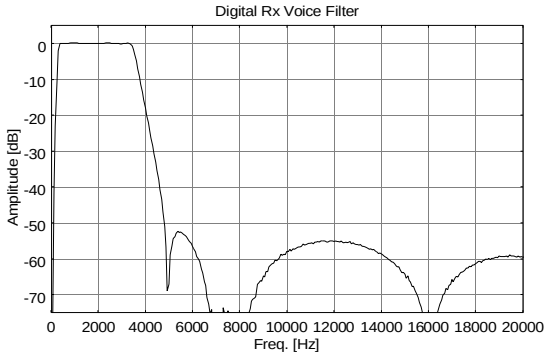


Figure 7. Digital Rx Voice Filter characteristic
Frequency response up to 2.5Fs (Fs=8kHz)

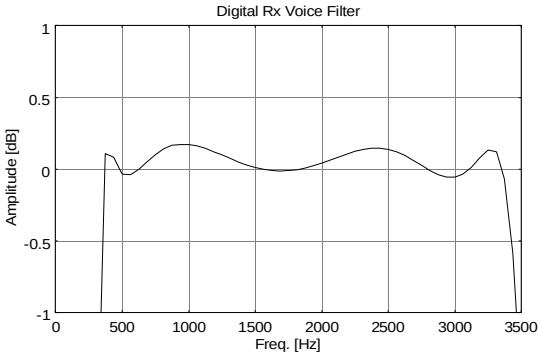


Figure 8. Digital Rx Voice Filter characteristic
In band Frequency response (Fs=8kHz).

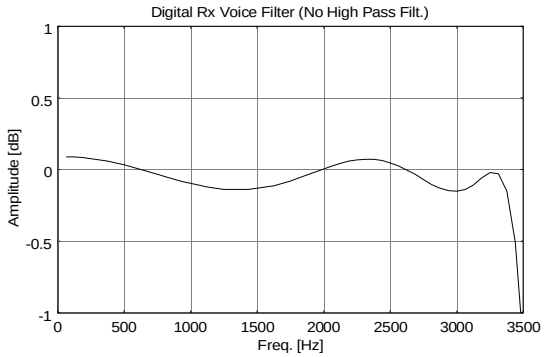


Figure 9. Digital Rx Voice Filter characteristic
In band Frequency response (Fs=8kHz).
High Pass filter disabled (HPB=1).

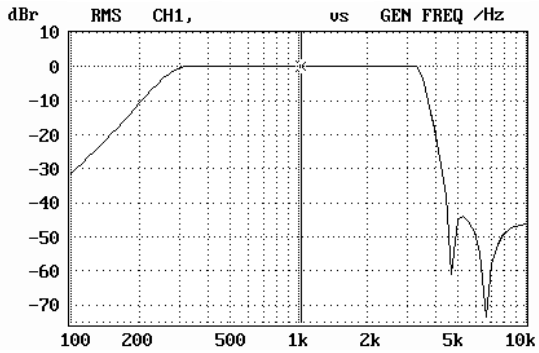
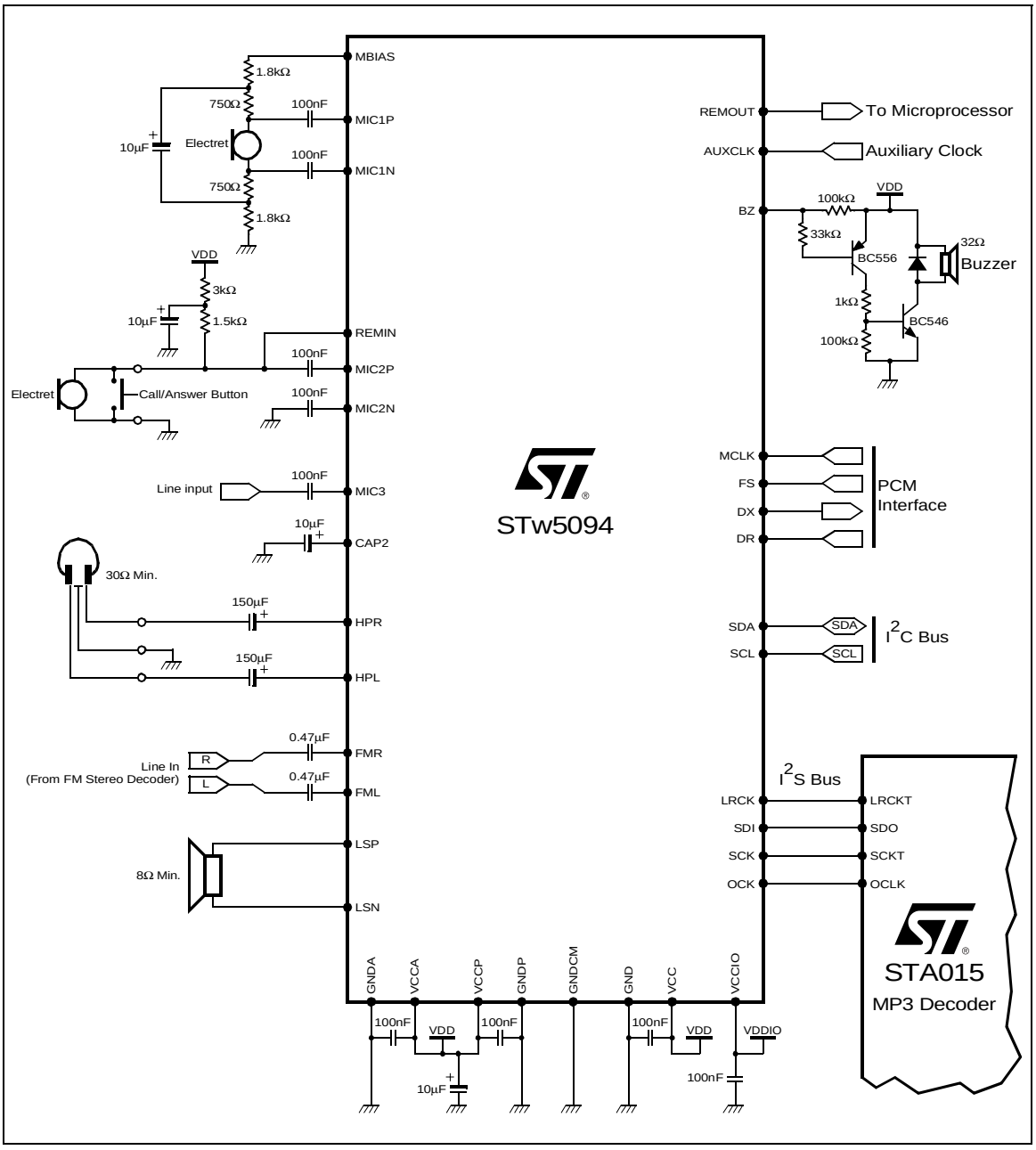


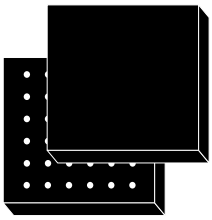
Figure 10. Tx Voice Filter characteristic
Full Tx path frequency response (Fs=8kHz).

APPLICATION NOTE



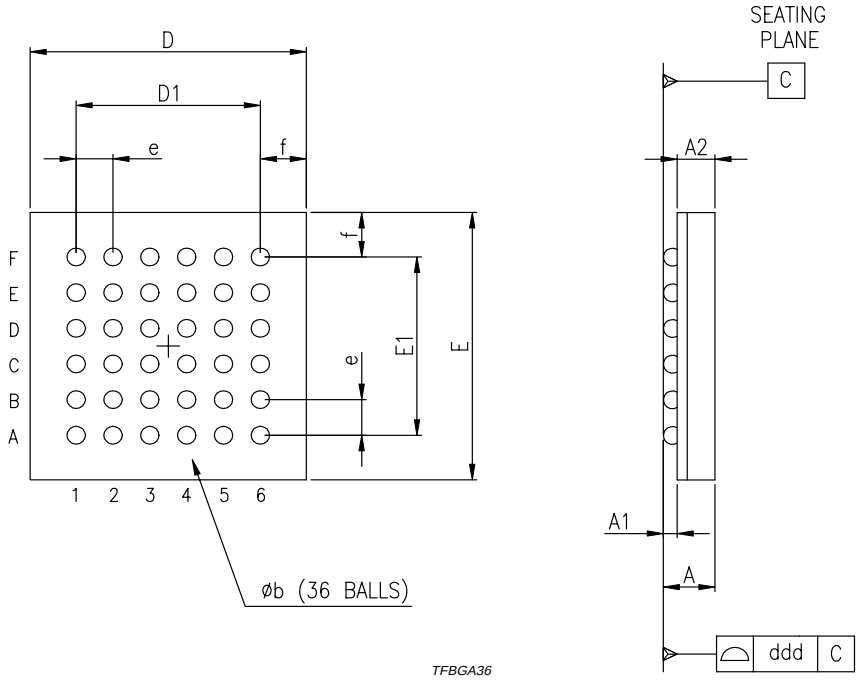
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.01		1.20	0.040		0.047
A1	0.21			0.008		
A2		0.82			0.032	
b	0.35	0.40	0.45	0.014	0.016	0.018
D	5.85	6.00	6.15	0.23	0.236	0.242
D1		4.00			0.157	
E	5.85	6.00	6.15	0.23	0.236	0.242
E1		4.00			0.157	
e	0.72	0.80	0.88	0.028	0.031	0.035
f	0.85	1.00	1.15	0.033	0.039	0.045
ddd			0.10			0.004

OUTLINE AND MECHANICAL DATA



Body: 6 x 6 x 1.2mm

TFBGA36
Fine Pitch Ball Grid Array



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