DS1248/DS1248P
1024k NV SRAM with Phantom Clock

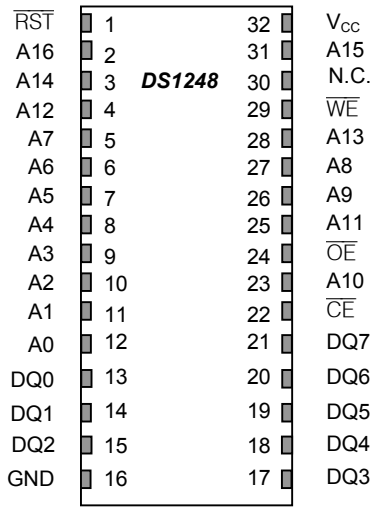
FEATURES

- Real-Time Clock (RTC) Keeps Track of Hundredths of Seconds, Minutes, Hours, Days, Date of the Month, Months, and Years
- 128k x 8 NV SRAM Directly Replaces Volatile Static RAM or EEPROM
- Embedded Lithium Energy Cell Maintains Calendar Operation and Retains RAM Data
- Watch Function is Transparent to RAM Operation
- Month and Year Determine the Number of Days in Each Month; Valid Up to 2100
- Full 10% Operating Range
- Operating Temperature Range: 0°C to +70°C
- Over 10 Years of Data Retention in the Absence of Power
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DIP Module Only
- Standard 32-Pin JEDEC Pinout
- Underwriters Laboratory (UL) Recognized
- Available in Lead-Free Package
- PowerCap® Module Board Only
  Surface Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Pin-for-Pin Compatible with DS1244P and DS1251P

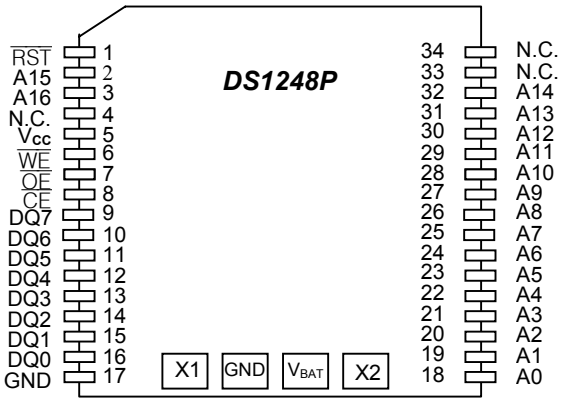
PowerCap is a registered trademark of Dallas Semiconductor Corp.

PIN CONFIGURATIONS

TOP VIEW



Encapsulated DIP
(740-mil Flush)



PowerCap Module Board
(Uses DS9034PCX PowerCap)

ORDERING INFORMATION

PART	TEMP RANGE	V_{CC} RANGE	PIN-PACKAGE	TOP MARK***
DS1248Y-70	0°C to +70°C	5V ±10%	32 EDIP	DS1248Y-70
DS1248Y-70IND	-40°C to +85°C	5V ±10%	32 EDIP	DS1248Y-70 IND
DS1248Y-100IND	-40°C to +85°C	5V ±10%	32 EDIP	DS1248Y-100 IND
DS1248YP-70	0°C to +70°C	5V ±10%	34 PowerCap*	DS1248YP-70
DS1248W-120	0°C to +70°C	3.3V ±10%	32 EDIP	DS1248W-120
DS1248W-120IND	-40°C to +85°C	3.3V ±10%	32 EDIP	DS1248W-120 IND
DS1248WP-120	0°C to +70°C	3.3V ±10%	34 PowerCap*	DS1248WP-120
DS1248WP-120IND	-40°C to +85°C	3.3V ±10%	34 PowerCap*	DS1248WP-120**
DS1248Y-70+	0°C to +70°C	5V ±10%	32 EDIP	DS1248Y-70
DS1248Y-70IND+	-40°C to +85°C	5V ±10%	32 EDIP	DS1248Y-70 IND
DS1248Y-100IND+	-40°C to +85°C	5V ±10%	32 EDIP	DS1248Y-100 IND
DS1248YP-70+	0°C to +70°C	5V ±10%	34 PowerCap*	DS1248YP-70
DS1248W-120+	0°C to +70°C	3.3V ±10%	32 EDIP	DS1248W-120
DS1248W-120IND+	-40°C to +85°C	3.3V ±10%	32 EDIP	DS1248W-120 IND
DS1248WP-120+	0°C to +70°C	3.3V ±10%	34 PowerCap*	DS1248WP-120
DS1248WP-120IND+	-40°C to +85°C	3.3V ±10%	34 PowerCap*	DS1248WP-120**

+ Denotes a lead-free/RoHS-compliant device.
** DS9034PCX (PowerCap) required. Must be ordered separately.*
*** An "IND" is located in the lower right-hand corner of the label.*
**** The top mark will include a "+" symbol on lead-free devices.*

DETAILED DESCRIPTION

The DS1248 1024k NV SRAM with phantom clock is a fully static, nonvolatile RAM (organized as 128k words by 8 bits) with a built-in real-time clock. The DS1248 has a self-contained lithium energy source and control circuitry, which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and writes protection is unconditionally enabled to prevent garbled data in both the memory and real-time clock.

PACKAGES

The DS1248 is available in two packages: 32-pin DIP and 34-pin PowerCap module. The 32-pin DIP style module integrates the crystal, lithium energy source, and silicon in one package. The 34-pin PowerCap module board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1248P after completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery because of the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap module board and PowerCap are ordered separately and shipped in separate containers.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Storage Temperature Range……40ºC to +85ºC (noncondensing)
Soldering Temperature..……...+260°C for 10 seconds (EDIP) (Note 13);
See IPC/JEDEC Standard J-STD-020 for Surface-Mount Devices

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

OPERATING RANGE

RANGE	TEMP RANGE (NONCONDENSING)	V_{CC} (V)
Commercial	0°C to +70°C	3.3 ±10% or 5 ±10%
Industrial	-40°C to +85°C	3.3 ±10% or 5 ±10%

RECOMMENDED DC OPERATING CONDITIONS

Over the Operating Range

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{CC} = 5V ±10%	V_{IH}	2.2		V_{CC} + 0.3V	V	11
	V_{CC} = 3.3V ±10%		2.0		V_{CC} + 0.3V		
Logic 0	V_{CC} = 5V ±10%	V_{IL}	-0.3		+0.8	V	11
	V_{CC} = 3.3V ±10%		-0.3		+0.6		

DC ELECTRICAL CHARACTERISTICS

Over the Operating Range (5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5	10	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current t_{CYC} = 70ns	I_{CC01}			85	mA	
Write Protection Voltage	V_{PF}	4.25	4.37	4.50	V	11
Battery Switchover Voltage	V_{SO}		V_{BAT}		V	11

DC ELECTRICAL CHARACTERISTICS

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	12
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current at 2.4V	I_{OH}	-1.0			mA	
Output Current at 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5	7	mA	
Standby Current $\overline{CE} = V_{CC}$ - 0.5V	I_{CCS2}		2.0	3.0	mA	
Operating Current t_{CYC} = 70ns	I_{CC01}			50	mA	
Write Protection Voltage	V_{PF}	2.80	2.86	2.97	V	11
Battery Switchover Voltage	V_{SO}		V_{BAT} or V_{PF}		V	11

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

MEMORY AC ELECTRICAL CHARACTERISTICS

Over the Operating Range (5V)

PARAMETER	SYMBOL	DS1248Y-70		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	70		ns	
Access Time	t_{ACC}		70	ns	
$\overline{OE}$ to Output Valid	t_{OE}		35	ns	
$\overline{CE}$ to Output Valid	t_{CO}		70	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High-Z from Deselection	t_{OD}		25	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	70		ns	
Write Pulse Width	t_{WP}	50		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	0		ns	
Output High-Z from $\overline{WE}$	t_{ODW}		25	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	30		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	5		ns	4

PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS

Over the Operating Range (5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	65			ns	
$\overline{CE}$ Access Time	t_{CO}			55	ns	
$\overline{OE}$ Access Time	t_{OE}			55	ns	
$\overline{CE}$ to Output Low-Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low-Z	t_{OEE}	5			ns	
$\overline{CE}$ to Output High-Z	t_{OD}			25	ns	5
$\overline{OE}$ to Output High-Z	t_{ODO}			25	ns	5
Read Recovery	t_{RR}	10			ns	
Write Cycle Time	t_{WC}	65			ns	
Write Pulse Width	t_{WP}	55			ns	3
Write Recovery	t_{WR}	10			ns	10
Data Setup Time	t_{DS}	30			ns	4
Data Hold Time	t_{DH}	0			ns	4
$\overline{CE}$ Pulse Width	t_{CW}	60			ns	
$\overline{RST}$ Pulse Width	t_{RST}	65			ns	

POWER-DOWN/POWER-UP TIMING

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from $V_{PF(max)}$ to $V_{PF(min)}$($\overline{CE}$ at V_{PF})	t_F	300			µs	
V_{CC} Slew from $V_{PF(min)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Slew from $V_{PF(max)}$ to $V_{PF(min)}$($\overline{CE}$ at V_{PF})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	1.5		2.5	ms	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time	t_{DR}	10			years	9

Warning: Under no circumstances are negative undershoots of any amplitude allowed when device is in battery-backup mode.

MEMORY AC ELECTRICAL CHARACTERISTICS

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	DS1248W-120		UNITS	NOTES
		MIN	MAX		
Read Cycle Time	t_{RC}	120		ns	
Access Time	t_{ACC}		120	ns	
$\overline{OE}$ to Output Valid	t_{OE}		60	ns	
$\overline{CE}$ to Output Valid	t_{CO}		120	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		ns	5
Output High-Z from Deselection	t_{OD}		40	ns	5
Output Hold from Address Change	t_{OH}	5		ns	
Write Cycle Time	t_{WC}	120		ns	
Write Pulse Width	t_{WP}	90		ns	3
Address Setup Time	t_{AW}	0		ns	
Write Recovery Time	t_{WR}	20		ns	10
Output High-Z from $\overline{WE}$	t_{ODW}		40	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		ns	5
Data Setup Time	t_{DS}	50		ns	4
Data Hold Time from $\overline{WE}$	t_{DH}	20		ns	4

PHANTOM CLOCK AC ELECTRICALCHARACTERISTICS

Over the Operating Range (3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	120			ns	
$\overline{CE}$ Access Time	t_{CO}			100	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ to Output Low-Z	t_{COE}	5			ns	
$\overline{OE}$ to Output Low-Z	t_{OEE}	5			ns	
$\overline{CE}$ to Output High-Z	t_{OD}			40	ns	5
$\overline{OE}$ to Output High-Z	t_{ODO}			40	ns	5
Read Recovery	t_{RR}	20			ns	
Write Cycle Time	t_{WC}	120			ns	
Write Pulse Width	t_{WP}	100			ns	3
Write Recovery	t_{WR}	20			ns	10
Data Setup Time	t_{DS}	45			ns	4
Data Hold Time	t_{DH}	0			ns	4
$\overline{CE}$ Pulse Width	t_{CW}	105			ns	
$\overline{RST}$ Pulse Width	t_{RST}	120			ns	

POWER-DOWN/POWER-UP TIMING

Over the Operating Range (3.3V)

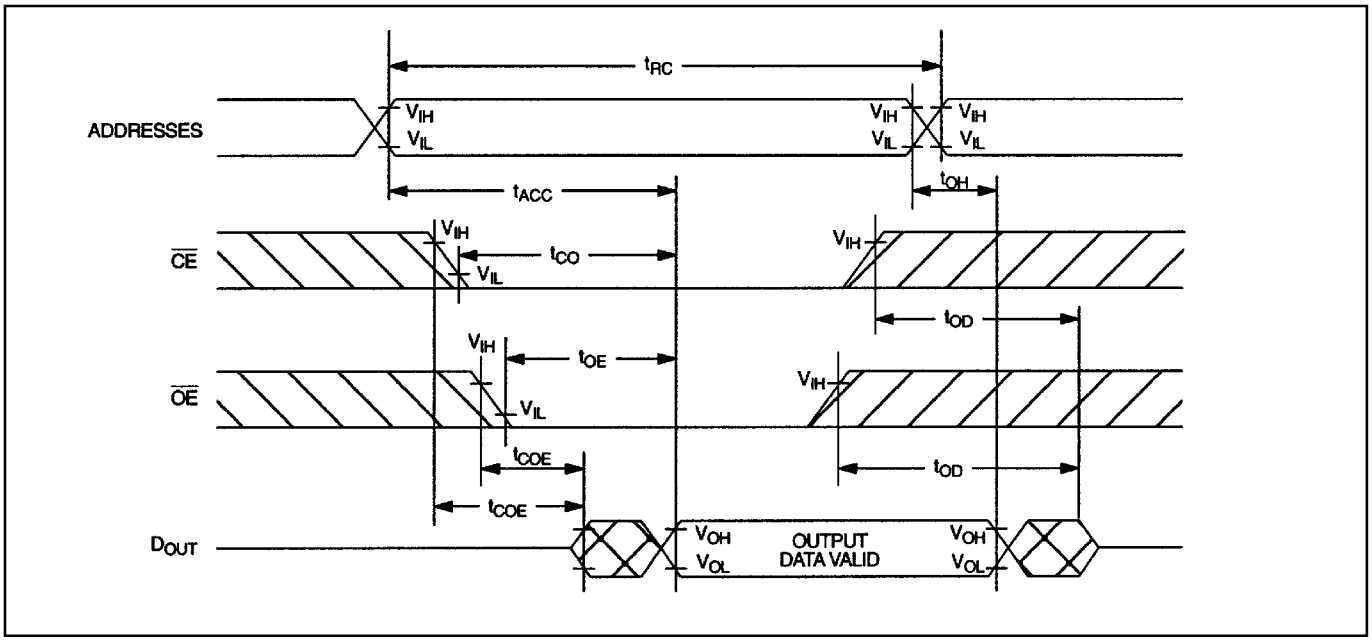
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	
V_{CC} Slew from $V_{PF(MAX)}$ to $V_{PF(MIN)}$($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from $V_{PF(MAX)}$ to $V_{PF(MIN)}$($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-Up	t_{REC}	1.5		2.5	ms	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data-Retention Time	t_{DR}	10			years	9

Warning: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

MEMORY READ CYCLE (Note 1)



AC TEST CONDITIONS

Output Load: 50pF + 1TTL Gate
Input Pulse Levels: 0 to 3V

Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) $\overline{WE}$ is high for a read cycle.
2) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{CE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3) t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5) These parameters are sampled with a 50pF load and are not 100% tested.
6) If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high-impedance state during this period.
7) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
8) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9) The expected t_{DR} is defined as cumulative time in the absence of V_{CC} with the clock oscillator running.
10) t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11) Voltages are referenced to ground.
12) $\overline{RST}$ (Pin 1) has an internal pullup resistor.
13) RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used. See the PowerCap package drawing for details regarding the PowerCap package.