# MAX8556, MAX8557

4A Ultra-Low-Input-Voltage LDO Regulators

## Description

The MAX8556/MAX8557 low-dropout linear regulators operate from input voltages as low as 1.425V and are able to deliver up to 4A of continuous output current with a typical dropout voltage of only 100mV. The output voltage is adjustable from 0.5V to $V_{IN}$ - 0.2V.

Designed with an internal p-channel MOSFET pass transistor, the MAX8556/MAX8557 maintain a low 800µA typical supply current, independent of the load current and dropout voltage. Using a p-channel MOSFET eliminates the need for an additional external supply or a noisy internal charge pump. Other features include a logic-controlled shutdown mode, built-in soft-start, short-circuit protection with foldback current limit, and thermal-overload protection. The MAX8556 features a POK output that transitions high when the regulator output is within ±10% of its nominal output voltage. The MAX8557 offers a power-on reset output that transitions high 140ms after the output has achieved 90% of its nominal output voltage.

The MAX8556/MAX8557 are available in a 16-pin thin QFN 5mm x 5mm package with exposed paddle.

## Key Features

## Applications / Uses

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- 1.425V to 3.6V Input Voltage Range
- Guaranteed 4A Output Current
- ±1% Output Accuracy Over Load/Line/Temperature
- 100mV Dropout at 4A Load (typ)
- Built-In Soft-Start
- 800µA (typ) Operating Supply Current
- 150µA (max) Shutdown Supply Current
- Short-Circuit Current Foldback Protection
- Thermal-Overload Protection
- ±10% Power-OK (MAX8556)
- 140ms Power-On Reset Output (MAX8557)
- Fast Transient Response
- 16-Pin Thin QFN (5mm x 5mm) Package

Automated Test Equipment (ATE)
Networking
Optical Modules
Point-of-Load Supplies
Servers and Storage Devices
Wireless Base Stations

**Key Specifications: Linear Regulators**

| Part Number | Regulators per Pkg. | Min. $V_{IN}$ (V) | Max. $V_{IN}$ (V) | Min. Adjustable $V_{OUT}$ (V) | Max. Adjustable $V_{OUT}$ (V) | Typ. $V_{DROPOUT}$@ Rated $I_{LOAD}$ (V) | Rated $I_{LOAD}$ (mA) | Max. $I_{CC}$ (µA) | Low Battery/ Power Fail Output | Nominal POK/ Reset Threshold (V) | Watchdog | Reverse Battery Protection | Package | Operating Temp. Range (°C) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MAX8556 | 1 | 1.4 | 3.6 | 0.5 | 3.4 | 0.1 | 4,000 | 1600 | No | Vout-10% | No | No | THIN QFN/16 | -40 to +85 | |
| MAX8557 | | | | | | | | | | | | | | | |

See All Linear Regulators (145)

**Notes:**
**This pricing is BUDGETARY, for comparing similar parts. Prices are in U.S. dollars and subject to change. Quantity pricing may vary substantially and international prices may differ due to local duties, taxes, fees, and exchange rates. For volume-specific prices and delivery, please see the price and availability page or contact an authorized distributor.

**Diagram**

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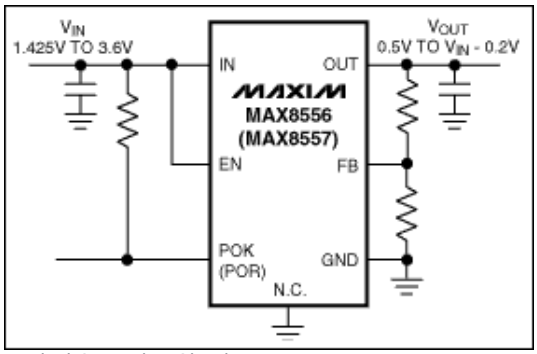

*Typical Operating Circuit*

## Evaluation Kits

MAX8556EVKIT

## Design Guides

Power Management for Battery-Powered Equipment (PDF)

## Reliability Reports

Show FIT data for:
Reliability Report: MAX8556ETE.pdf MAX8557ETE.pdf

## Software / Models

none

## Ordering Information

Notes:

1. Other options and links for purchasing parts are listed at:
2. Didn't Find What You Need? Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
3. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: SeeFull Data Sheet or Part Naming Conventions.
4. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses. Note that "+", "#", "-" in the part number suffix describes RoHS status. Package drawings may show a different suffix character.

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**Devices: 1-8 of 8**

| MAX8556 | Free Sample | Buy | Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR * | Temp | RoHS/Lead-Free? Materials Analysis |
|---|---|---|---|---|---|
| MAX8556ETE | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655-2* | -40°C to +85°C | RoHS/Lead-Free: No<br>Materials Analysis |
| MAX8556ETE-T | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655-2* | -40°C to +85°C | RoHS/Lead-Free: No<br>Materials Analysis |
| MAX8556ETE+ | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655+2* | -40°C to +85°C | RoHS/Lead-Free: Lead Free<br>Materials Analysis |
| MAX8556ETE+T | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655+2* | -40°C to +85°C | RoHS/Lead-Free: Lead Free<br>Materials Analysis |
| **MAX8557** | **Free Sample** | **Buy** | **Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *** | **Temp** | **RoHS/Lead-Free? Materials Analysis** |
| MAX8557ETE | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655-2* | -40°C to +85°C | RoHS/Lead-Free: No<br>Materials Analysis |
| MAX8557ETE-T | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655-2* | -40°C to +85°C | RoHS/Lead-Free: No<br>Materials Analysis |
| MAX8557ETE+ | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655+2* | -40°C to +85°C | RoHS/Lead-Free: Lead Free<br>Materials Analysis |
| MAX8557ETE+T | | | THIN QFN;16 pin;<br>Dwg: 21-0140 (PDF)<br>Use pkgcode/variation: T1655+2* | -40°C to +85°C | RoHS/Lead-Free: Lead Free<br>Materials Analysis |

## More Information

Product Ad:
MAX8516

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EVALUATION KIT AVAILABLE

# 4A Ultra-Low-Input-Voltage LDO Regulators



## General Description

The MAX8556/MAX8557 low-dropout linear regulators operate from input voltages as low as 1.425V and are able to deliver up to 4A of continuous output current with a typical dropout voltage of only 100mV. The output voltage is adjustable from 0.5V to $V_{IN}$ - 0.2V.

Designed with an internal p-channel MOSFET pass transistor, the MAX8556/MAX8557 maintain a low 800µA typical supply current, independent of the load current and dropout voltage. Using a p-channel MOSFET eliminates the need for an additional external supply or a noisy internal charge pump. Other features include a logic-controlled shutdown mode, built-in soft-start, short-circuit protection with foldback current limit, and thermal-overload protection. The MAX8556 features a POK output that transitions high when the regulator output is within ±10% of its nominal output voltage. The MAX8557 offers a power-on reset output that transitions high 140ms after the output has achieved 90% of its nominal output voltage.

The MAX8556/MAX8557 are available in a 16-pin thin QFN 5mm x 5mm package with exposed paddle.

## Features

- ♦ **1.425V to 3.6V Input Voltage Range**
- ♦ **Guaranteed 4A Output Current**
- ♦ **±1% Output Accuracy Over Load/Line/ Temperature**
- ♦ **100mV Dropout at 4A Load (typ)**
- ♦ **Built-In Soft-Start**
- ♦ **800µA (typ) Operating Supply Current**
- ♦ **150µA (max) Shutdown Supply Current**
- ♦ **Short-Circuit Current Foldback Protection**
- ♦ **Thermal-Overload Protection**
- ♦ **±10% Power-OK (MAX8556)**
- ♦ **140ms Power-On Reset Output (MAX8557)**
- ♦ **Fast Transient Response**
- ♦ **16-Pin Thin QFN (5mm x 5mm) Package**

## Applications

Servers and Storage Devices

Networking

Base Stations

Optical Modules

Point-of-Load Supplies

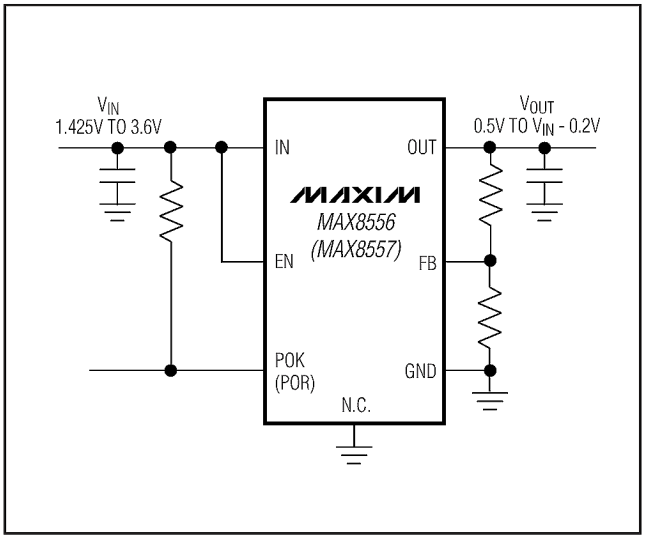
ATE

## Ordering Information

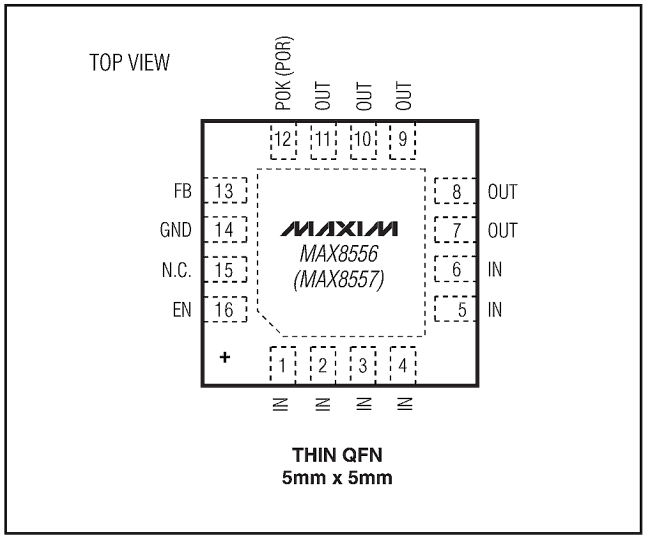
| PART | TEMP RANGE | PIN-PACKAGE | FEATURE |
|---|---|---|---|
| **MAX8556**ETE+ | -40°C to +85°C | 16 Thin QFN 5mm x 5mm | POK |
| **MAX8557**ETE+ | -40°C to +85°C | 16 Thin QFN 5mm x 5mm | POR |

*+Denotes a lead-free/RoHS-compliant package.*

## Typical Operating Circuit




## Pin Configuration




**THIN QFN 5mm x 5mm**



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# 4A Ultra-Low-Input-Voltage LDO Regulators

## ABSOLUTE MAXIMUM RATINGS

IN, EN, POK, POR to GND .....-0.3V to +4V
FB, OUT to GND .....-0.3V to ($V_{IN}$ + 0.3V)
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation ($T_A$ = +70°C)
16-Pin Thin QFN (derate 33.3mW/°C above +70°C) (Note 1).....2666.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**Note 1:** Maximum power dissipation is obtained using JEDEC JESD51-5 and JESD51-7 standards.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{EN}$ = $V_{IN}$ = 1.8V, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 2mA, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **IN** | | | | | | |
| Input Voltage Range | | | 1.425 | | 3.600 | V |
| Input Undervoltage Lockout | $V_{IN}$ rising, 70mV hysteresis | | 1.30 | 1.35 | 1.40 | V |
| | $V_{IN}$ falling | | 1.23 | 1.28 | 1.33 | |
| **OUT** | | | | | | |
| Output Voltage Range | | | 0.5 | | 3.4 | V |
| Load Regulation | $I_{OUT}$ = 2mA to 4A | | | 0.1 | | %/A |
| Line Regulation | $V_{IN}$ = 1.425V to 3.6V, $V_{OUT}$ = 1.225V | | -0.15 | 0 | +0.15 | %/V |
| Dropout Voltage | $V_{IN}$ = 1.425V, $I_{OUT}$ = 4A, $V_{FB}$ = 480mV | | | 100 | 200 | mV |
| Regulated Output-Voltage Current Limit | $V_{IN}$ = 3.6V, $V_{OUT}$ = 3V, $V_{FB}$ = 460mV | | 5 | 7 | 9 | A |
| Load Capacitance | ESR < 50mA | | 16 | | 120 | µF |
| **FB** | | | | | | |
| FB Threshold Accuracy (Note 3) | $V_{OUT}$ = 1.225V to 3V, $V_{IN}$ = $V_{OUT}$ + 0.2V to 3.6V, $I_{OUT}$ = 2mA to 4A | | 495 | 500 | 505 | mV |
| FB Input Bias Current | $V_{FB}$ = 0.5V, $V_{IN}$ = 3.6V | | | 0.001 | 1 | µA |
| **GND** | | | | | | |
| GND Supply Current | $V_{IN}$ = 1.425V to 3.6V, $V_{OUT}$ = 1.225V | | | 800 | 1600 | µA |
| | Dropout, $V_{IN}$ = 3.6V, $V_{FB}$ = 480mV | | | 1000 | 2000 | |
| GND Shutdown Current | $V_{IN}$ = 3.6V, EN = GND | | | | 150 | µA |
| **POK** | | | | | | |
| FB Power-OK Fault Threshold | FB moving out of regulation, $V_{IN}$ = 1.425V to 3.6V, 10mV hysteresis | FB high | 540 | 550 | 560 | mV |
| | | FB low | 440 | 450 | 460 | |
| POK Output Voltage, Low | $V_{FB}$ = 0.4V or 0.6V, $I_{POK}$ = 2mA | | | 25 | 200 | mV |



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## ELECTRICAL CHARACTERISTICS (continued)

($V_{EN}$ = $V_{IN}$ = 1.8V, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 2mA, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

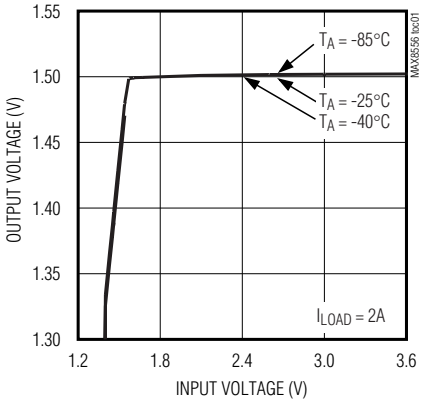
| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| POK Output Current, High | $V_{POK}$ = 3.6V $V_{FB}$ = 0.5 | | | 0.001 | 1 | µA |
| POK Delay Time | From FB rising to POK high | | 25 | 50 | 100 | µs |
| **EN** | | | | | | |
| Enable Input Threshold | $V_{IN}$ = 1.425V to 3.6V | EN rising | | | 1.25 | V |
| | | EN falling | 0.4 | | | |
| Enable Input Bias Current | $V_{EN}$ = 0V or 3.6V | | -1 | | +1 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal-Shutdown Threshold | Output on and off | $T_J$ rising | | +160 | | °C |
| | | $T_J$ falling | | +115 | | |
| **POR** | | | | | | |
| FB Power-On Reset Fault Threshold | FB falling, $V_{IN}$ = 1.425V to 3.6V, 10mV hysteresis | | 440 | 450 | 460 | mV |
| POR Output Voltage, Low | $V_{FB}$ = 0.4V, $I_{POR}$ = 2mA | | | 25 | 200 | mV |
| POR Output Current, High | $V_{POR}$ = 3.6V, $V_{FB}$ = 0.5V | | | 0.001 | 1 | µA |
| POR Rising Delay Time | FB rising to POR high impedance | | 100 | 140 | 200 | ms |
| **SOFT-START** | | | | | | |
| Soft-Start Time | | | | 100 | | µs |

**Note 2:** Specifications to $T_A$ = -40°C are guaranteed by design and not production tested.
**Note 3:** Minimum supply voltage for output accuracy must be at least 1.425V.

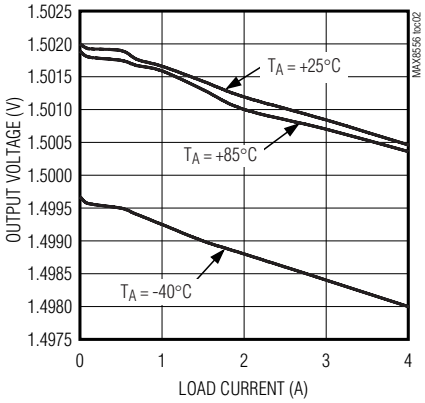
## Typical Operating Characteristics

($V_{EN}$ = $V_{IN}$ = +1.8V, $V_{OUT}$ = +1.5V, $I_{OUT}$ = 4A, $C_{OUT}$ = 20µF, $C_{IN}$ = 20µF, and $T_A$ = +25°C, unless otherwise noted.)

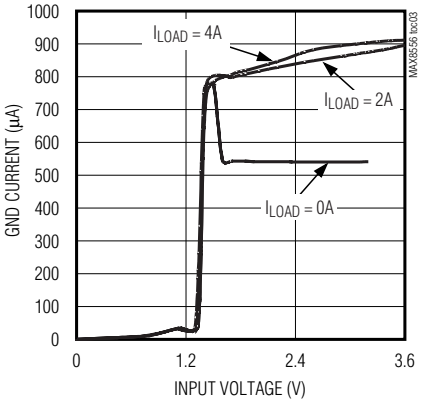
**OUTPUT VOLTAGE vs. INPUT VOLTAGE**




**OUTPUT VOLTAGE vs. LOAD CURRENT**




**GND CURRENT vs. INPUT VOLTAGE**



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### Thermal Considerations in PC Board Layout

How much power the package can dissipate strongly depends on the mounting method of the IC to the PC board and the copper area for cooling. Using the JEDEC test standard, the maximum power dissipation allowed in the package is 2667mW. This data is obtained with +70°C ambient temperature and +150°C maximum junction temperature. The test board has dimensions of 3in x 3in with four layers of 2oz copper and FR-4 material with 62mil finished thickness. Nine thermal vias are used under the thermal paddle with a diameter of 12mil and 1mil plated copper thickness. Top and bottom layers are used to route the traces. Two middle layers are solid copper and isolated from the nine thermal vias.

More power dissipation can be handled by the package if great attention is given during PC board layout. For example, using the top and bottom copper as a heatsink and connecting the thermal vias to one of the middle layers (GND) transfers the heat from the package into the board more efficiently, resulting in lower junction temperature at high power dissipation in some MAX8556/MAX8557 applications. Furthermore, the solder mask around the IC area on both top and bottom layers can be removed to radiate the heat directly into the air. The maximum allowable power dissipation in the IC is as follows:

$$P_{MAX} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), $T_A$ is the ambient air temperature, $\theta_{JC}$ (1.7°C/W for the 16-pin TQFN) is the thermal resistance from the junction to the case, and $\theta_{CA}$ is the thermal resistance from the case to the surrounding air through the PC board, copper traces, and the package materials. $\theta_{CA}$ is directly related to system level variables and can be modified to increase the maximum power dissipation. The TQFN package has an exposed thermal pad on its underside. This pad provides a low thermal resistance path for heat transfer into the PC board. This low thermally resistive path carries a majority of the heat away from the IC. The PC board is effectively a heatsink for the IC.

The exposed paddle should be connected to a large ground plane for proper thermal and electrical performance. The minimum size of the ground plane is dependent upon many system variables. To create an efficient path, the exposed paddle should be soldered to a thermal landing, which is connected to the ground plane by thermal vias. The thermal landing should be at least as large as the exposed paddle and can be made larger depending on the amount of free space from the exposed paddle to the other pin landings.

A sample layout is available on the MAX8556 evaluation kit to speed designs.

## Chip Information

TRANSISTOR COUNT: 3137
PROCESS: BiCMOS

## Package Information

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 16 TQFN | T1655-2 | 21-0140 |



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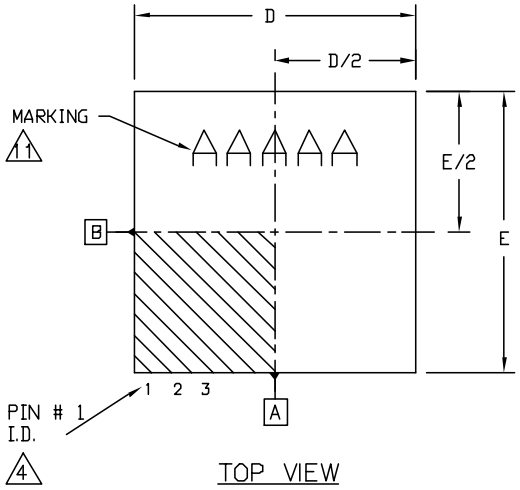
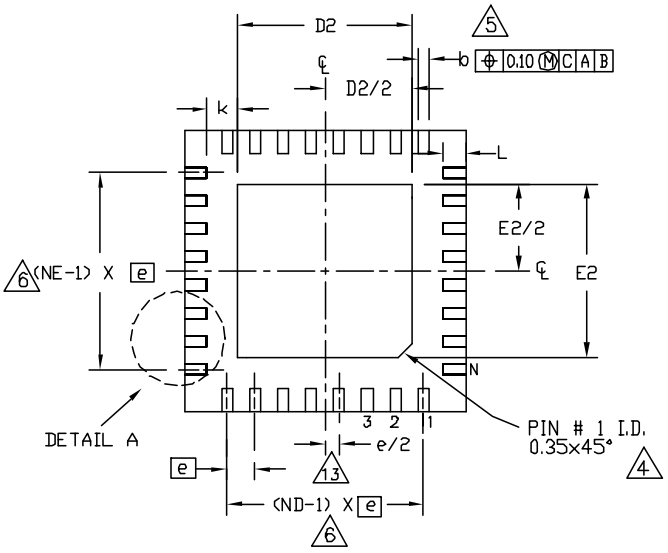
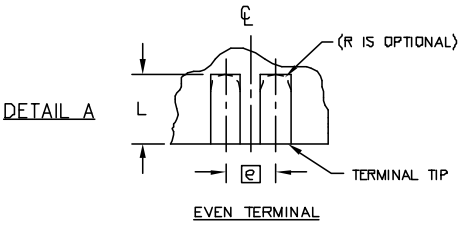


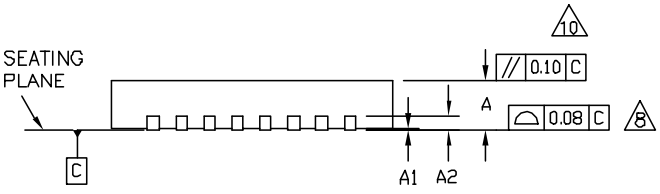

TOP VIEW




BOTTOM VIEW




EVEN TERMINAL




SIDE VIEW

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE:
PACKAGE OUTLINE,
16,20,28,32,40L THIN QFN, 5x5x0.80mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | L | 1/2 |

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| COMMON DIMENSIONS | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PKG. | 16L 5x5 | | | 20L 5x5 | | | 28L 5x5 | | | 32L 5x5 | | | 40L 5x5 | | | |
| SYMBOL | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | 0 | 0.02 | 0.05 | |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.20 | 0.25 | 0.30 | 0.15 | 0.20 | 0.25 | |
| D | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | |
| E | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | 4.90 | 5.00 | 5.10 | |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | | 0.40 BSC. | | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | |
| L | 0.30 | 0.40 | 0.50 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 | 0.30 | 0.40 | 0.50 | |
| N | 16 | | | 20 | | | 28 | | | 32 | | | 40 | | | |
| ND | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | | |
| NE | 4 | | | 5 | | | 7 | | | 8 | | | 10 | | | |
| JEDEC | WHHB | | | WHHC | | | WHHD-1 | | | WHHD-2 | | | ----- | | | |

| EXPOSED PAD VARIATIONS | | | | | | |
|---|---|---|---|---|---|---|
| PKG. CODES | D2 | | | E2 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1655-2 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T1655N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T2055-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2055MN-5 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-3 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-4 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-5 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-6 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855-7 | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |
| T2855-8 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T2855N-1 | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |
| T3255-3 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255M-4 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255-5 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T3255N-1 | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |
| T4055-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055-2 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |
| T4055MN-1 | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE:
PACKAGE OUTLINE,
16,20,28,32,40L THIN QFN, 5x5x0.80mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0140 | L | 2/2 |

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