National Semiconductor

May 1998

DS92LV222A
Two Channel Bus LVDS MUXed Repeater

General Description

The DS92LV222A is a repeater designed specifically for the bridging of multiple backplanes in a rack. The DS92LV222A utilizes low voltage differential signaling to deliver high speed while consuming minimal power with reduced EMI. The RSEL pin and DE pins allow maximum flexibility as to which receiver/driver are used. The DS92LV222A repeats signals between backplanes and accepts or drives signals onto the local bus. It also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

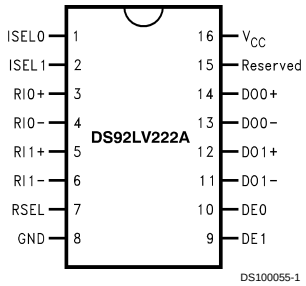
The driver is selectable between 3.5 mA (100Ω load) and 8.5 mA (27Ω load) output loop currents depending upon the level applied to the ISEL pin. This allows for single termination (point-to-point) and also double termination (multipoint) applications while maintain similar differential levels.

The receiver threshold is ±100 mV, while providing ±1V common mode range.

Features

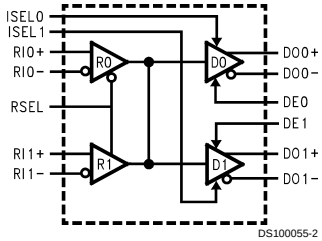
- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- Ultra Low Power Dissipation (13.2 mW quiescent)
- Balanced Output Impedance
- Lite Bus Loading 5 pF typical
- Selectable Drive Capability (3.5 mA or 8.5 mA)
- 3.3V operation
- ±1V Common Mode Range
- ±100 mV Receiver Sensitivity
- Available in 16 pin SOIC package.

Connection Diagram



Order Number DS92LV222ATM
See NS Package Number M16A

Block Diagram



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Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.0V
Enable Input Voltage (DE)	−0.3V to (V_{CC} + 0.3V)
Current Select Voltage (ISEL)	−0.3V to (V_{CC} + 0.3V)
Receiver Select Voltage (RSEL)	−0.3V to (V_{CC} + 0.3V)
Bus Pin Voltage (DO/RI±)	−0.3V to +3.9V
Driver Short Circuit Current	Continuous
ESD (HBM 1.5 kΩ, 100 pF)	>2 kV
Maximum Package Power Dissipation at 25˚C	
SOIC	970 mW
Derate SOIC Package above 25˚C	8mW/˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	260˚C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free Air Temperature	−40	+85	˚C

DC Electrical Characteristics

T_A = −40˚C to +85˚C unless otherwise noted, V_{CC} = 3.3V ± 0.3V (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
V_{OD}	Output Differential Voltage	R_L = 27Ω *Figure 1* Isel = 0V	DO+, DO−	170	220	280	mV
ΔV_{OD}	VOD Magnitude Change				2	10	mV
V_{OS}	Offset Voltage			1.0	1.25	1.6	V
ΔV_{OS}	Offset Magnitude Change				10	20	mV
V_{OD}	Output Differential Voltage	R_L = 100Ω *Figure 1* Isel = 3.3V		250	360	480	mV
ΔV_{OD}	VOD Magnitude Change				2	10	mV
V_{OS}	Offset Voltage			0.9	1.25	1.6	V
ΔV_{OS}	Offset Magnitude Change				10	20	mV
I_{OZD}	TRI-STATE ® Leakage	V_O = V_{CC} or GND, DE = 0			±1	±10	µA
I_{OXD}	Power-Off Leakage	V_O = 2.9V or GND, V_{CC} = 0V			±1	±10	µA
I_{OSD}	Output Short Circuit Current	ISEL = V_{CC} V_O = 0V			−11	−13	mA
DIFFERENTIAL RECEIVER CHARACTERISTICS							
V_{TH}	Input Threshold High		RI+, RI−			+100	mV
V_{TL}	Input Threshold Low			−100			mV
I_{IN}	Input Current	V_{IN} = +2.9V, or 0V, V_{CC} = 3.6 V or 0 V		−10	±1	+10	µA
DEVICE CHARACTERISTICS							
V_{IH}	Minimum Input High Voltage		DE0, DE1, RSEL, ISEL0, ISEL1	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V			±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA		−1.5	−0.8		V

DC Electrical Characteristics (Continued)

T_A = −40˚C to +85˚C unless otherwise noted, V_{CC} = 3.3V ± 0.3V (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
I_{CCD}	Power Supply Current	No Load; DE = RSEL = V_{CC} Isel = 0 V	V_{CC}		25	45	mA
		R_L = 27Ω; DE = RSEL = V_{CC} Isel = 0 V			24	40	mA
I_{CCZ}		DE = 0V; RSEL = V_{CC}			4	8	mA
C_{input}	Capacitance at		RO+/RO-		5		pF
C_{output}	Capacitance at		DO+/DO-		5		pF

Note 1: "Absolute Maximum Ratings" are these beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = +3.3V and T_A = +25˚C, unless otherwise stated.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) > 2 kV EIAJ (0Ω, 200 pF) > 200V

Note 5: CL includes probe and fixture capacitance.

Note 6: Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50Ω, t_f = < 6.0 ns (0%–100%).

Note 7: The DS92LV222A is a current mode device and only functions datasheet specifications when a resistive load is applied to the drivers outputs.

Note 8: During receiver select transition(s), data must be held in a steady state 15 ns before and 15 ns after the RSEL pin changes state.

Note 9: Channel-to-channel skew is the measurement between outputs of D0 and D1.

AC Electrical Characteristics

T_A = −40˚C to +85˚C, V_{CC} = 3.3V ± 0.3V (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Transition Time Low to High	R_L = 27Ω *Figures 2, 3* C_L = 10 pF *Figures 2, 3*	0.15	0.4	2.0	ns
t_{THL}	Transition Time High to Low		0.15	0.4	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω *Figures 4, 5* C_L = 10 pF *Figures 4, 5*	2.0	6.0	9.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	6.0	9.0	ns
t_{PZH}	Enable Time Z to High		2.0	6.0	9.0	ns
t_{PZL}	Enable Time Z to Low		2.0	6.0	9.0	ns
DIFFERENTIAL RECEIVER TO DRIVER TIMING REQUIREMENTS						
t_{PHL_RD}	Differential Prop. Delay High to Low	R_L = 27Ω *Figures 2, 3* C_L = 10 pF *Figures 2, 3*	3.0	7.7	13	ns
t_{PLH_RD}	Differential Prop. Delay Low to High		3.0	8.0	13	ns
t_{SK_RD}	Pulse SKEW $\|t_{PHL} - t_{PLH}\|$		0	0.3	2.0	ns
t_{PHL_RS0}	Prop. Delay High to Low	RSEL to Driver Outputs R_L = 27Ω *Figures 6, 7* C_L = 10 pF (Note 8)	2.0	7.5	13	ns
t_{PLH_RS1}	Prop. Delay Low to High		2.0	8.0	13	ns
$t_{PHL\_R_0\ D_X}$	Channel-to-Channel Skew R_0 to D_X	R_L = 27Ω C_L = 10 pF (Note 9)		0.3	0.8	ns
$t_{PLH\_R_0\ D_X}$	Channel-to-Channel Skew R_0 to D_X			0.3	0.8	ns
$t_{PHL\_R_1\ D_X}$	Channel-to-Channel Skew R_1 to D_X			0.3	0.8	ns
$t_{PLH\_R_1\ D_X}$	Channel-to-Channel Skew R_1 to D_X			0.3	0.8	ns

Test Circuits and Timing Waveforms

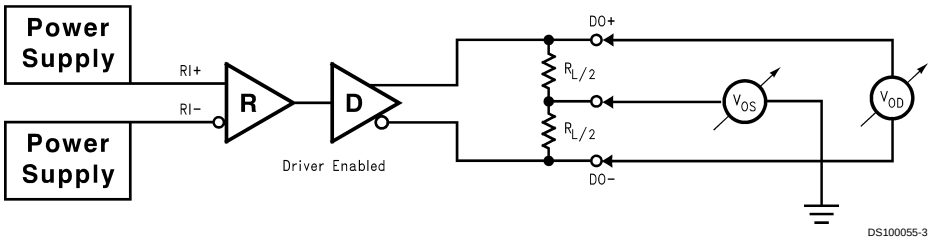


FIGURE 1. Differential Driver DC Test Circuit

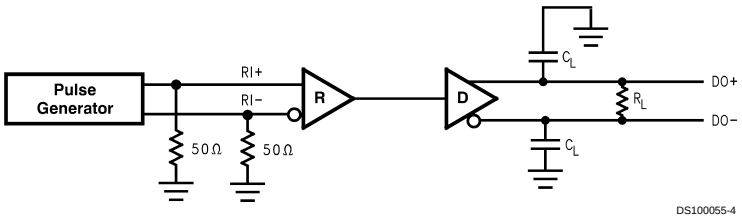


FIGURE 2. Differential Receiver to Driver Propagation Delay and Driver Transition Time Test Circuit

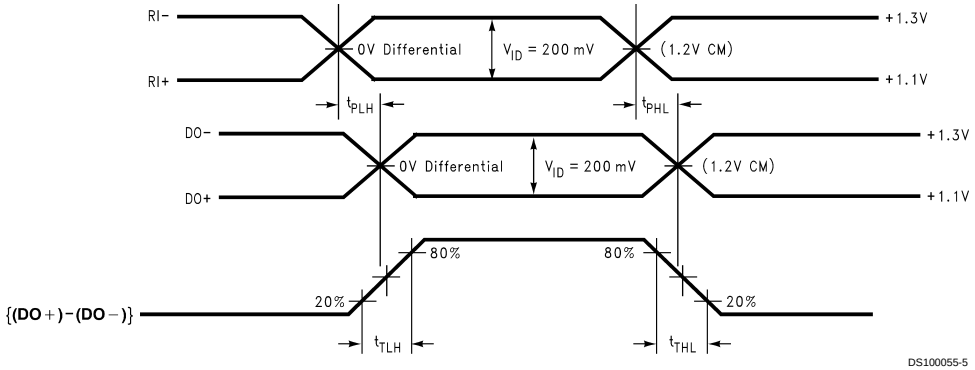


FIGURE 3. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms

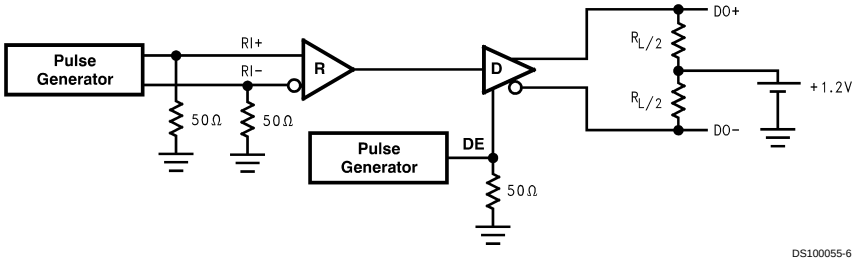


FIGURE 4. Driver TRI-STATE Delay Test Circuit

Test Circuits and Timing Waveforms (Continued)

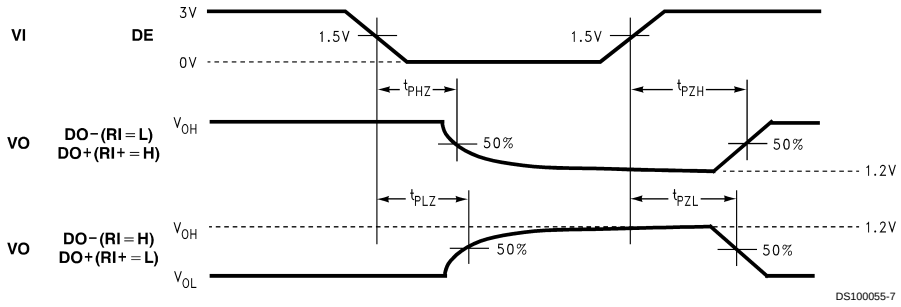


FIGURE 5. Driver TRI-STATE Delay Waveforms

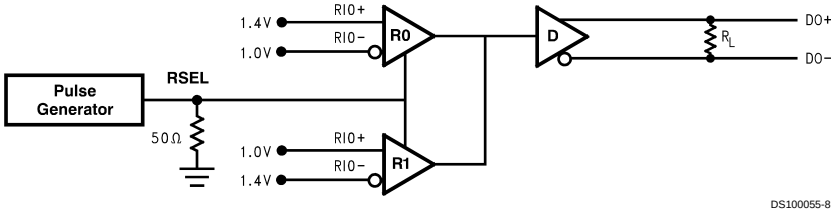


FIGURE 6. Receiver Select to Driver Propagation Delay Test Circuit

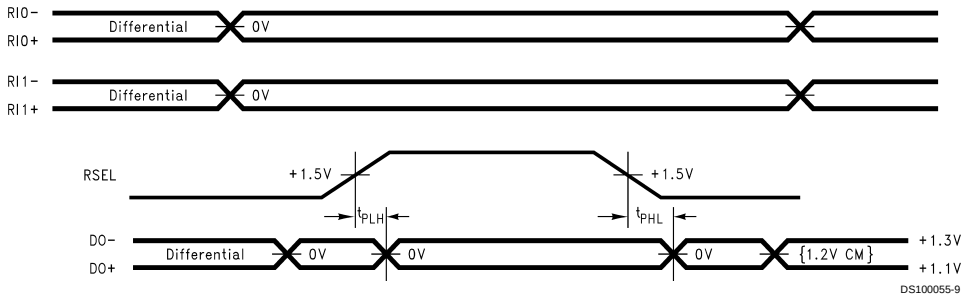


FIGURE 7. Receiver Select to Driver Propagation Delay Waveforms

Pin Description

Pin Name	Number of Pins	Input/ Output	Description
RI±	4	I	Bus LVDS Receiver Inputs
DO±	4	O	Bus LVDS Driver Outputs
RSEL	1	I	Receiver Select TTL Input, (see Truth Tables)
DE	2	I	Driver Enable TTL Input, Active High
ISEL	2	I	IOL Control Pin (Select High = 3.5 mA (100Ω Load), Select Low = 8.5mA (27Ω Load))
GND	1	NA	Ground Reference
V_{CC}	1	NA	Power Supply
Reserved	1	NA	Reserved Pin

Function Select Table

MODE SELECTED	DE0	DE1	RSEL
Receiver Zero ON, Driver Zero ON, Driver One OFF	H	L	L
Receiver Zero ON, Driver Zero OFF, Driver One ON	L	H	L
Receiver One ON, Driver Zero ON, Driver One OFF	H	L	H
Receiver One ON, Driver Zero OFF, Driver One ON	L	H	H
Receiver Zero ON, Driver Zero ON, Driver One ON	H	H	L
Receiver One ON, Driver Zero ON, Driver One ON	H	H	H
Driver Zero and Driver One TRI-STATE	L	L	X

Truth Table for Receiver Zero

INPUTS			OUTPUTS	
DE0	RSEL	(RI0+)−(RI0−)	DO+	DO−
H	L	L	L	H
H	L	H	H	L
H	L	100 mV > & > −100 mV	X	X
L	X	X	Z	Z

X = High or low logic state
Z = High impedance state
L = Low state

Truth Table for Receiver One

INPUTS			OUTPUTS	
DE1	RSEL	(RI1+)−(RI1−)	DO+	DO−
H	H	L	L	H
H	H	H	H	L
H	H	100 mV > & > −100 mV	X	X
L	X	X	Z	Z

X = High or low logic state
Z = High impedance state
L = Low state

Truth Table for Current Drive

Driver	Current Drive	ISEL0	ISEL1
Driver 0	3.5 mA	H	X
Driver 0	8.5 mA	L	X
Driver 1	3.5 mA	X	H
Driver 1	8.5 mA	X	L

Applications Information

There are few common practices which should be employed when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best. Two or three multilayer ceramic (MLC) surface mount capacitors (0.1µ and 0.01 µF in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
- Use controlled impedance traces which match the differential impedance of your transmission medium (i.e., Cable) and termination resistor.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating).
- Isolate TTL signals from Bus LVDS signals.

MEDIA (CABLE, CONNECTOR OR BACKPLANE) SELECTION:

- Use controlled impedance media. The cables and connectors should have a matched differential impedance.
- Balanced cables (e.g., twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality.
-
- There are different types of failsafe situations to consider, these are Open Input, Terminated Input, and other special cases. The first, Open input failsafe occurs when only one receiver is being used (R0 for example). The unused receiver (R1) inputs should be left open for noise minimization. The second case is for terminated inputs. This occurs when the inputs have a low impedance (typically 100 Ohm) termination (R_T) across them, and the cable is unplugged. For this case, and if the output state needs to maintain a known state, two external bias resistors may be used to provide a strong common mode bias point. For this a 10K Ohm pull up and pull down resistor may be used to set the output high. Note that R_1 and R_2 should be much larger (2 orders of magnitude) compared to R_T to minimize loading effects to the Bus LVDS driver when it is active.

Applications Information (Continued)

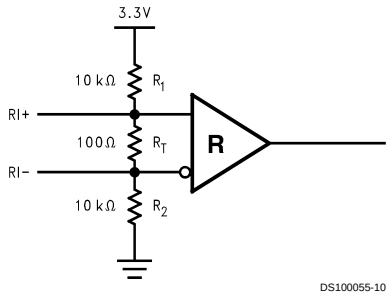
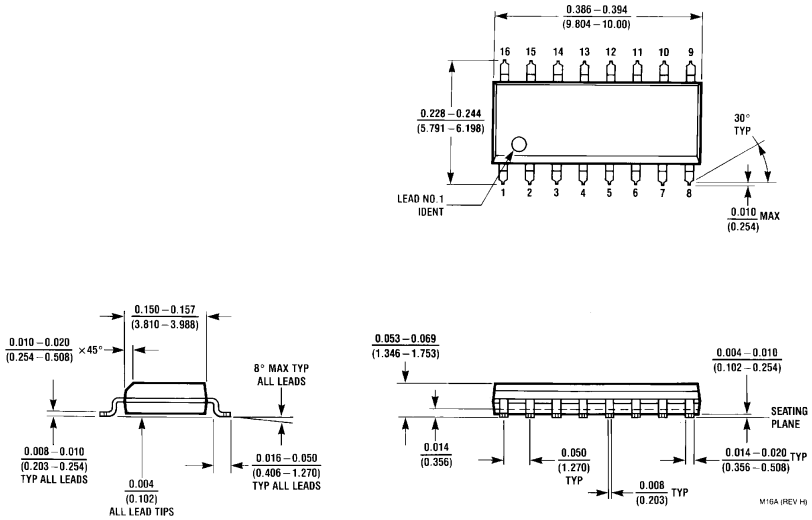


FIGURE 8. Terminated Input Failsafe Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS92LV222ATM
NS Package Number M16A

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