19-5810; Rev 0; 3/11

EVALUATION KIT AVAILABLE

Audio Amplifier with Jack Detection

General Description

The MAX97236 is an audio amplifier with volume control and microphone preamplifier intended for use in portable audio systems employing a headphone jack. The audio circuit is powered from a single, dual-mode charge pump, allowing the output signals to be ground referenced, and eliminating the need for large and expensive DC-blocking capacitors. The configuration of a 3.5mm jack is determined by autoconfigure circuitry. The IC's functional blocks are auto-enabled after the configuration of the jack is determined.

The audio amplifier is powered from a single 1.8V power supply that reduces overall power consumption. The microphone preamplifier and bias are powered from a separate power-supply input accommodating bias voltages that are greater than 2.4V.

The automatic jack detection determines when a 3.5mm plug is inserted into the system jack and determines the configuration of the installed load. The configuration of the load is then reported to the system through the I²C interface. Multiple popular jack and load configurations are detectable with this scheme. The IC detects headsets, headphones, and A/V cables.

The headphone amplifier is capable of over 35mW into 16Ω. The device is available in a small, 25-bump WLP package with a 0.4mm pitch and is specified over the extended -40°C to +85°C temperature range.

Applications

Smartphones

Mobile Handsets

Notebooks

Portable Gaming Devices

Tablets

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	I²C ADDRESS
MAX97236EWA+	-40°C to +85°C	25 WLP	0x80

+Denotes a lead(Pb)-free/RoHS-compliant package.

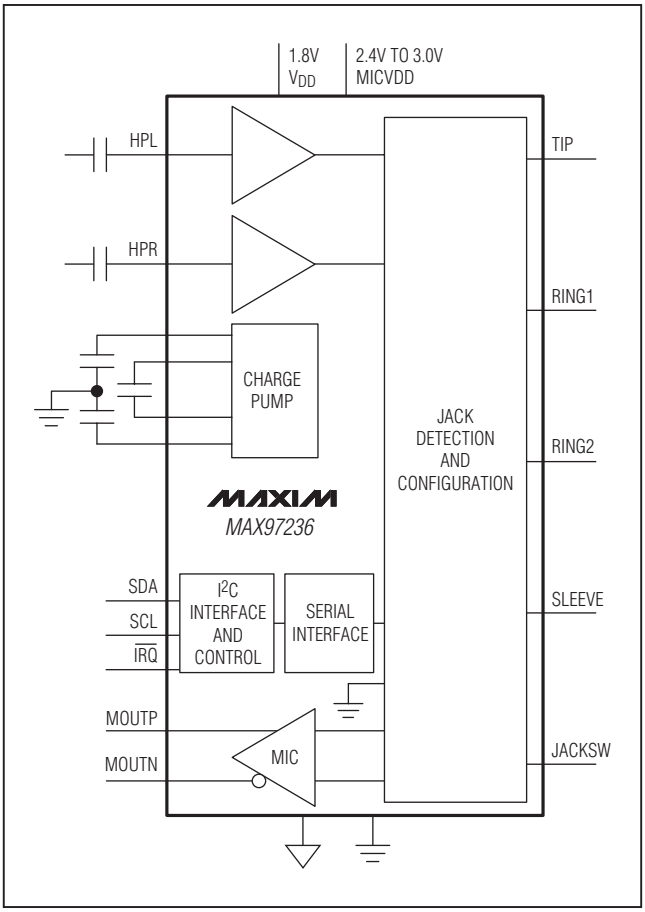
Functional Diagram/Typical Application Circuit appears at end of data sheet.

Features

- **30mW Headphone Amplifier Employs Second-Generation DirectDrive® with Dual-Mode Charge-Pump Architecture**
- **Automatic Jack Detection Circuitry**
- **Microphone Amplifier and Bias**
- **1.8V Power Supply**
- **2.4V to 3.6V Microphone Power Supply**
- **Headphone Amplifier Volume Control**
- **Decodes Data from a Passive Multibutton Headset Remote Control**
- **25-Bump, 2.4mm x 2.3mm, 0.4mm Pitch WLP**

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Audio Amplifier with Jack Detection

ABSOLUTE MAXIMUM RATINGS

V_{DD} to PGND .....-0.3V to +2V
MICVDD to PGND .....-0.3V to +5.5V
PVDD to PGND..... -0.3V to (V_{DD} + 0.3V)
PVSS to PGND .....-2V to +0.3V
GND to PGND .....-0.1V to +0.1V
TIP, RING1, IN_ to PGND..... (V_{PVSS} - 0.3V) to (V_{PVDD} + 0.3V)
RING2, SLEEVE to PGND ..... (GND - 0.3V) to (V_{MICVDD} + 0.3V)
JACKSW to PGND..... (V_{PVSS} - 0.3V) to (V_{MICVDD} + 0.3V)
MBIAS to PGND ..... -0.3V to (V_{DD} + 0.3V)
MOUT+ and MOUT- to PGND .....-0.3V to (V_{MICVDD} + 0.3V)
C1P to PGND .....-0.3V to (V_{PVDD} + 0.3V)
C1N to PGND..... (V_{PVSS} - 0.3V) to +0.3V
SDA, SCL, EXTCLK, and IRQ to PGND.....-0.3V to +6V
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (Mulitlayer Board, T_A = +70°C)
25-Bump WLP (derate 19.2mW/°C above +70°C)....1536mW
Junction Temperature .....+150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+230°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF. Typical values tested at T_A = +25°C, unless otherwise noted. See the *Functional Diagram/Typical Application Circuit*.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range	V_{DD}	Guaranteed by PSRR test	1.62	1.8	1.98	V
Undervoltage Lockout	UVLO	Rising V_{DD}, T_A = +25°C			1.6	V
Shutdown Supply Current	I_{VDD_SDF}	In jack detect mode, T_A = +25°C, fast detect mode, external clock disabled		14	25	µA
	I_{VDD_SDS}	In jack detect mode, T_A = +25°C, slow detect mode, external clock disabled		14	25	
Sleep Supply Current	I_{VDD_SL}	T_A = +25°C, external clock disabled			25	µA
Quiescent Supply Current	I_{VDD}	T_A = +25°C, state = LRGM		2.3	3.9	mA
SDA, SCL Input Logic-High	V_{IH}	1.8V logic compliant	1.4			V
SDA, SCL Input Logic-Low	V_{IL}	1.8V logic compliant			0.4	V
SDA, SCL, EXTCLK Input Leakage Current High	I_{IH}	T_A = +25°C	-1		+1	µA
SDA, SCL, EXTCLK Input Leakage Current Low	I_{IL}	T_A = +25°C	-1		+1	µA
SDA, SCL Output Logic-Low	V_{OLI2C}	I_{OLI2C} = 2.3mA		0.2 x V_{DD}		V
IRQ Output High Current	I_{OH}	V_{IRQ_OUT} = 3.3V, T_A = +25°C			1	µA
IRQ Output Logic-Low	V_{OL}	I_{OL} = 3mA			0.2 x V_{DD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF. Typical values tested at T_A = +25°C, unless otherwise noted. See the *Functional Diagram/Typical Application Circuit*.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTCLK Input High Voltage			1.4			V
EXTCLK Input Low Voltage					0.4	V
EXTCLK Frequency Range	f_{EXTCLK}	T_A = +25°C	1	19.2	26	MHz
EXTCLK Duty Cycle	D_EXTCLK	T_A = +25°C	45		55	%
Maximum EXTCLK Slew Rate		f_{EXTCLK} = 1MHz, 0.4V to 1.4V		50		ns
		f_{EXTCLK} = 10MHz, 0.4V to 1.4V		5		
Turn-On Time	t_{ON}	(Note 3)		1	10	ms
JACK DETECTION						
Turn-On Time	t_{ONTIME}	Jack detect time from insertion to interrupt (Note 4)		500		ms
AUDIO AMPLIFIER (Gain = 0dB, Unless Otherwise Noted)						
Output Offset Voltage	V_{OS}	T_A = +25°C, state = LRGM	-500		+500	µV
Output Power	P_{OUT}	R_L = 32Ω, THD+N = 1%, f_{IN} = 1kHz		30		mW
		R_L = 16Ω, THD+N = 1%, f_{IN} = 1kHz		35		
Line Output Voltage	V_{O_LINE}	R_L = 10kΩ		1		V_{RMS}
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω, P_{OUT} = 10mW, f_{IN} = 1kHz		0.05		%
		R_L = 16Ω, P_{OUT} = 0.1mW, f_{IN} = 1kHz		0.04		
		R_L = 10kΩ, V_{OUT} = 1V_{RMS}, f_{IN} = 1kHz		0.03		
Signal-to-Noise Ratio	SNR	Referenced to 32Ω load, 1V_{RMS} input signal, A-weighted		103		dB
		Referenced to 32Ω load, 1V_{RMS} input signal, A-weighted (gain = -30dB)		85		
Power-Supply Rejection Ratio	PSRR	DC 1.62V to 1.98V, gain = 0dB, T_A = +25°C		87		dB
		f_{IN} = 217Hz, 100mV_{P-P} ripple, gain = 0dB		78		
		f_{IN} = 10kHz, 100mV_{P-P} ripple, gain = 0dB		74		
Output Noise	V_N	A-weighted		6		$µV_{RMS}$
		A-weighted, gain = -30dB		1.7		
		A-weighted, gain = -60dB		1.4		
Peak Output Current	I_{OUT}	Peak current needed to output the rated typical power		40		mA
Minimum Headphone Impedance	Z_{OUT}			12		Ω
Crosstalk	XTALK	R_L = 16Ω, f_{IN} = 1kHz, P_{OUT} = 5mW, crosstalk between audio channels, gain = 0dB, with ground sense		-51		dB
		R_L = 32Ω, f_{IN} = 1kHz, P_{OUT} = 25mW, crosstalk between audio channels, gain = 0dB, with ground sense		-56		

Audio Amplifier with Jack Detection

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF. Typical values tested at T_A = +25°C, unless otherwise noted. See the *Functional Diagram/Typical Application Circuit*.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Capacitive Load Drive	C_L	R_L = 10kΩ, gain ≥ 0dB			470		pF
		R_L = 10kΩ, gain < 0dB			200		
		R_L = 32Ω			200		
Power Consumption		Per channel	P_{OUT} = 0.5mW, R_L = 32Ω		4.5		mW
			P_{OUT} = 4.5mW, R_L = 32Ω, (Note 5)		6.8		
			P_{OUT} = 20mW, R_L = 32Ω, (Note 6)		23		
Charge-Pump Switch Threshold		Output voltage needed to toggle the charge-pump outputs	THSH = 0		0.4		V
			THSH = 1		0.55		
Click-and-Pop Level	KCP	R_L = 32Ω, peak voltage, A-weighted, 32 samples/second	Into shutdown		-74		dBV
			Out of shutdown		-74		
Input Capacitance	C_{IN}	Gain = 6dB			150		pF
Input Impedance	Z_{IN}			16		75	kΩ
AUDIO AMPLIFIER VOLUME CONTROL							
Gain Range		From min to max volume setting		-60		+6	dB
Maximum Volume Setting				5.5	6	6.5	dB
Minimum Volume Setting				-60.5	-60	-59.5	dB
Mute Attenuation					80		dB
Channel-to-Channel Gain Matching				-0.5		+0.5	dB
Gain Change per Step		Volume setting -54dB ≤ _VOL ≤ 6dB			1		dB
		Volume setting -60dB ≤ _VOL ≤ -54dB			2		
MICROPHONE BIAS							
MIC Bias Supply Voltage	V_{MICVDD}	Guaranteed by MIC bias PSRR test		2.4		3.6	V
Bias Output Voltage	V_{BIAS}	High output voltage		2.4	2.6	2.8	V
		Low output voltage		1.84	2	2.16	
Bias Output Current	I_{BIAS_OUT}	$R_{MICBIAS}$ = 2.2kΩ, high (2.6V) output voltage, T_A = +25°C		1.2			mA
MIC Supply Current Consumption	I_{MBIAS}				150	400	µA
Bias Output Resistance	R_{MBIAS}	MICR = 0b00, V_{MBIAS} = 2.6V, T_A = +25°C		2.02	2.2	2.38	kΩ
		MICR = 0b01, V_{MBIAS} = 2.6V, T_A = +25°C		2.39	2.6	2.81	
		MICR = 0b10, V_{MBIAS} = 2.6V, T_A = +25°C		2.76	3	3.24	
		MICR = 0b11, V_{MBIAS} = 2.6V, T_A = +25°C			0.07		
Bias Output Noise	V_{N_BIAS}	With external capacitor, V_{MBIAS} = 2.6V			2.8		$µV_{RMS}$

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF. Typical values tested at T_A = +25°C, unless otherwise noted. See the *Functional Diagram/Typical Application Circuit*.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bias Power-Supply Rejection	$PSRR_{MBIAS}$	R_{MBIAS} = 2.2kΩ	V_{MICVDD} = 2.4V to 3.6V, T_A = +25°C	74	90		dB
			f_{IN} = 2kHz, 100mV_{P-P} ripple		75		
MICROPHONE PREAMPLIFIER							
MIC Preamp Gain	A_{MIC}	Gain = high, f_{IN} = 997Hz		23	24	25	dB
		Gain = low, f_{IN} = 997Hz		11	12	13	
Supply Current Consumption	I_{DD_MAMP}				200	300	µA
MIC Preamp Noise	V_{N_MAMP}	Input referred (Note 7), gain = 24dB, A-weighted 0.1kHz to 7kHz			3		µV
Total Harmonic Distortion Plus Noise	$THD+N_{MICPRE}$	f_{IN} = 1kHz, V_{IN} = 1V_{RMS}				3	%
Low Corner Frequency Response	f_{-3dB}	Relative to 997Hz			15		Hz
High Corner Frequency Response	f_{-3dB}	Relative to 997Hz			> 300		kHz
MIC Preamplifier Power-Supply Rejection	PSR_{MAMP}	V_{MICVDD} = 2.4V to 3.6V, T_A = +25°C, gain = +24dB, R_{MIC} = 500Ω		74	90		dB
		f_{IN} = 2kHz, 100mV_{P-P} ripple (Note 7)			58		
Output Common-Mode Voltage	V_{CM_MIC}	Voltage measured from MOUTP or MOUTN to GND			0.8		V
Input Capacitance	C_{MAMP}	AC-coupling capacitance			85		pF
Input Resistance	R_{MAMP}	Input resistance			100		MΩ
Output Impedance	Z_{OUT}				10		Ω
6-BIT KEY ENCODER ADC							
ADC Trip Level		Level at which the mic bias must drop to trigger a conversion			0.64		V
Minimum ADC Course Range		LSB 10mV			0.128		V
Maximum ADC Course Range		LSB 10mV			0.64		V
Minimum ADC Fine Range		LSB 2mV			0		V
Maximum ADC Fine Range		LSB 2mV			0.128		V
CHARGE PUMP							
Oscillator Frequency	f_{OSC1}	V_{OUT} = 0V, R_L = open, T_A = +25°C		78	83	88	kHz
	f_{OSC2}	V_{OUT} = 0.2V, R_L = open			665		
ESD CHARACTERISTICS							
ESD Protection		Pins connected to the jack: TIP, RING1, RING2, SLEEVE, JACKSW			±2		kV
		All other pins			±2		

Audio Amplifier with Jack Detection

I²C TIMING CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R		$20 + 0.1C_B$		300	ns
SDA and SCL Receiving Fall Time	t_F		$20 + 0.1C_B$		300	ns
SDA Transmitting Fall Time	t_F		$20 + 0.1C_B$		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 2: All specifications are 100% tested at T_A = +25°C. Temperature limits are guaranteed by design.

Note 3: The current listed t_{ON} is the time from the system sending the enable signal, after receiving the DDONE signal, to when the amplifier outputs turn on.

Note 4: Total turn-on time from jack insert to output enable is dependent upon the search algorithm.

Note 5: Power consumption numbers taken with the THRH bit set high, fixing the power-supply switchover threshold at its highest value.

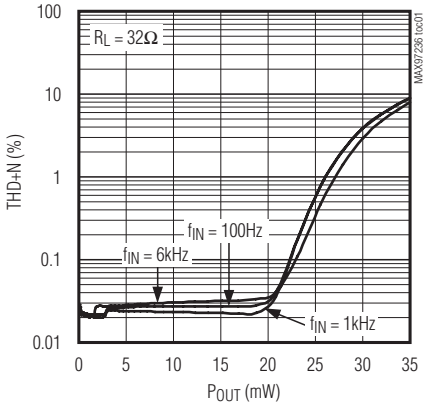
Note 6: Power consumption numbers taken with the high efficiency bit set low, fixing the power-supply switchover threshold at its lowest value, providing the least amount of dynamic distortion.

Note 7: Tested with R_{MIC} = 6kΩ in parallel with 5pF connected from SLEEVE to RING2.

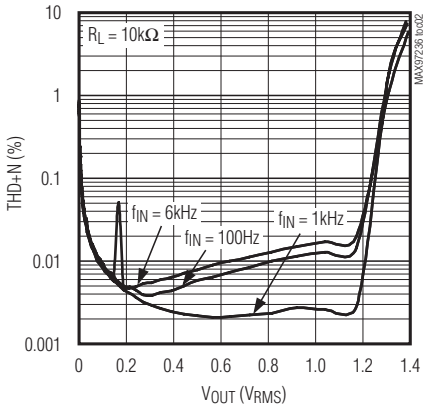
Typical Operating Characteristics

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF.)

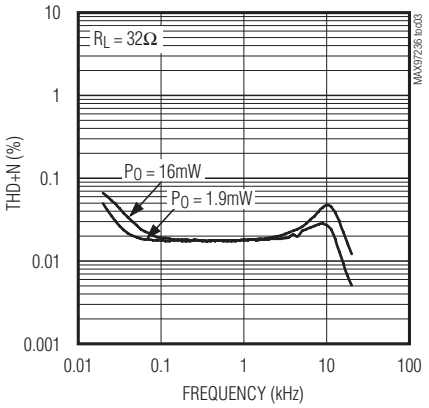
THD+N vs. OUTPUT POWER



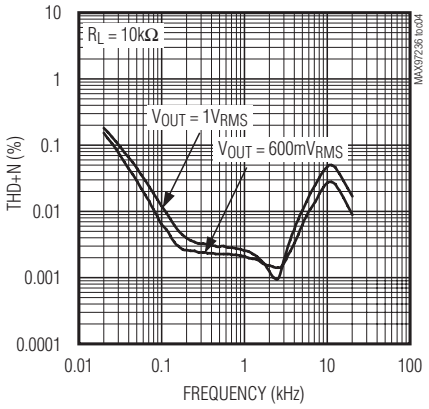
THD+N vs. OUTPUT VOLTAGE



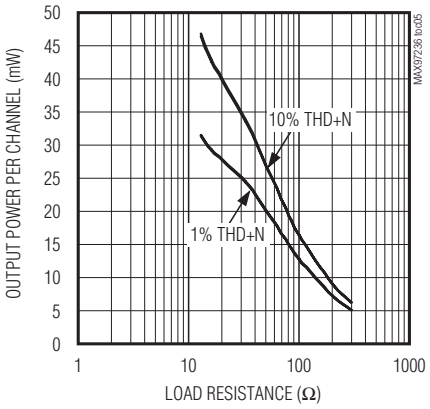
THD+N vs. FREQUENCY



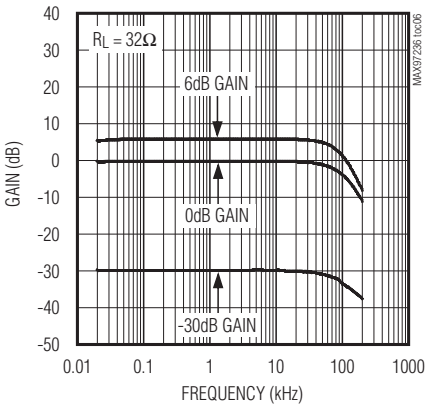
HEADPHONE AMPLIFIER THD+N vs. FREQUENCY



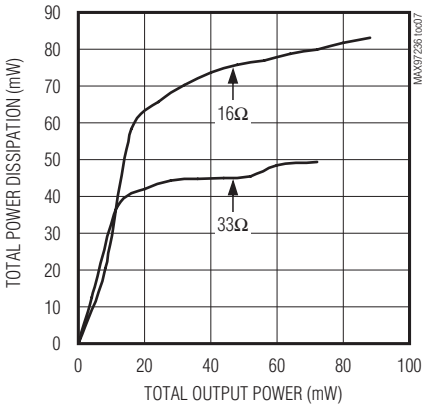
OUTPUT POWER vs. LOAD RESISTANCE



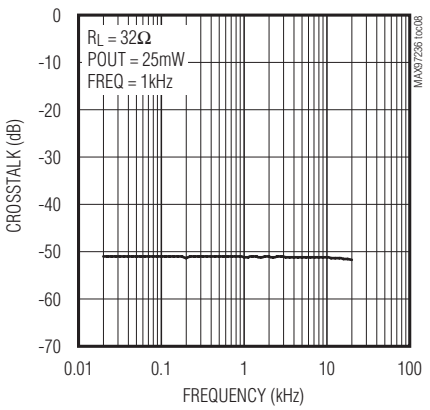
GAIN vs. FREQUENCY



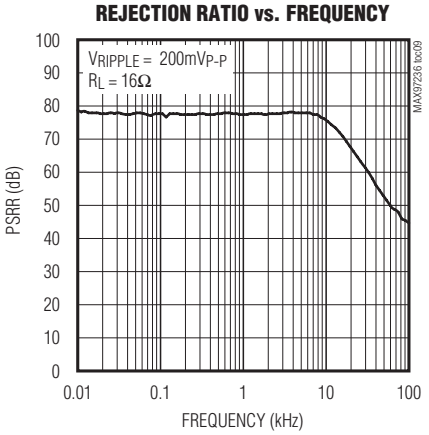
TOTAL POWER DISSIPATION vs. TOTAL OUTPUT POWER



HEADPHONE CROSSTALK vs. FREQUENCY



HEADPHONE AMPLIFIER POWER-SUPPLY REJECTION RATIO vs. FREQUENCY

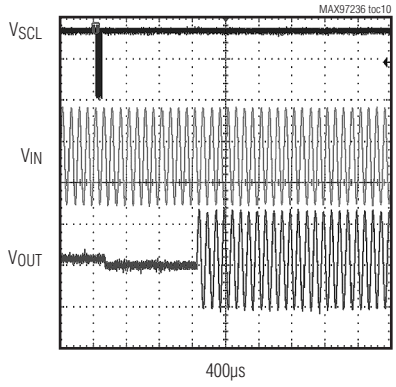


Audio Amplifier with Jack Detection

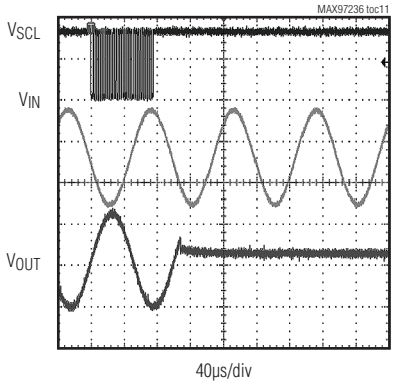
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF.)

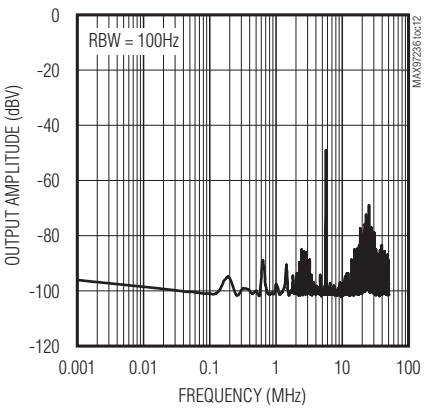
HEADPHONE AMPLIFIER TURN-ON RESPONSE



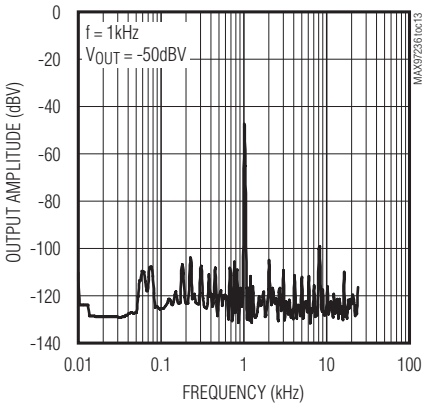
HEADPHONE AMPLIFIER TURN-OFF RESPONSE



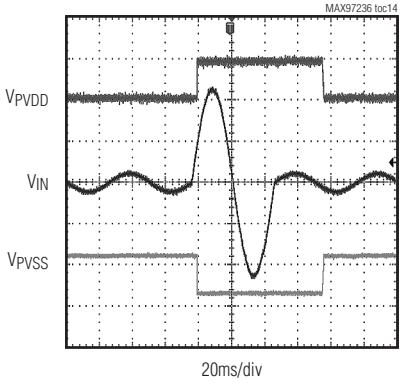
WIDEBAND OUTPUT SPECTRUM



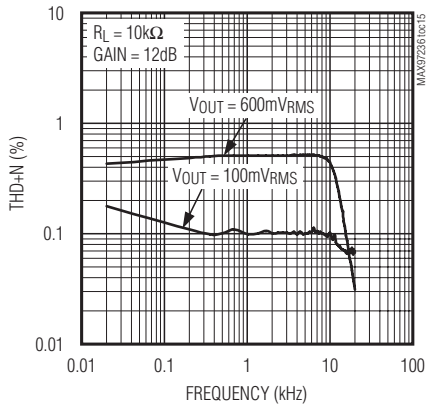
INBAND OUTPUT SPECTRUM



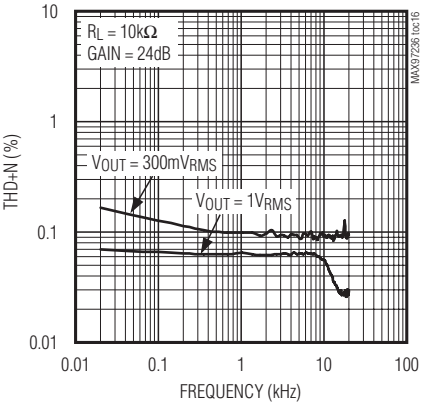
CLASS H OPERATION



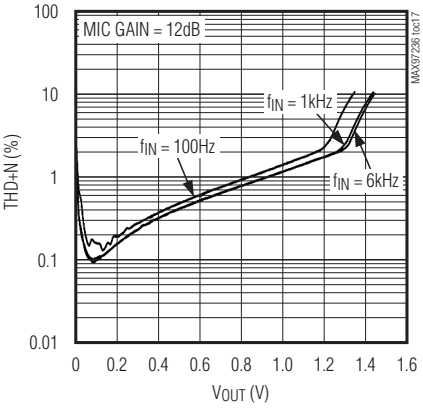
MICROPHONE AMPLIFIER THD+N vs. FREQUENCY



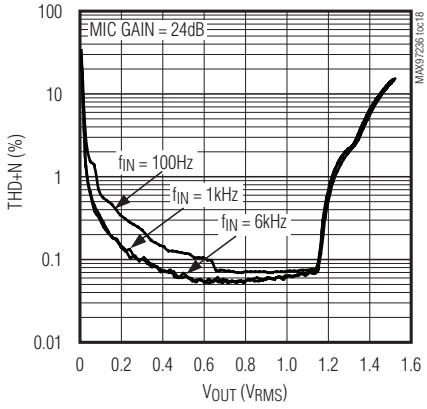
MICROPHONE AMPLIFIER THD+N vs. FREQUENCY



MICROPHONE PREAMPLIFIER THD+N vs. OUTPUT VOLTAGE



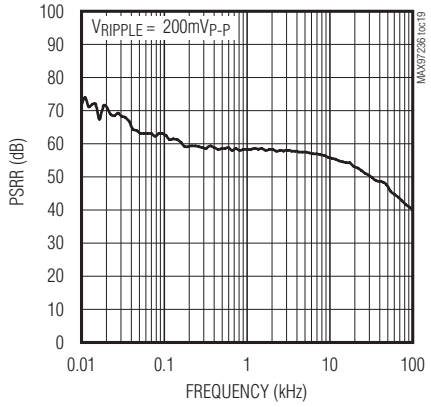
MICROPHONE PREAMPLIFIER THD+N vs. OUTPUT VOLTAGE



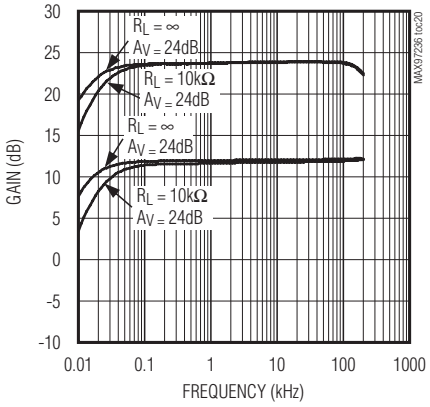
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{MICVDD} = 3.0V, V_{GND} = V_{PGND} = 0V, C_{FLY} = C_{PVDD} = C_{PVSS} = 1µF.)

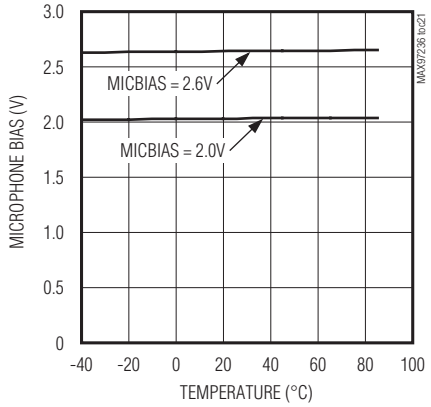
MICROPHONE PREAMPLIFIER POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



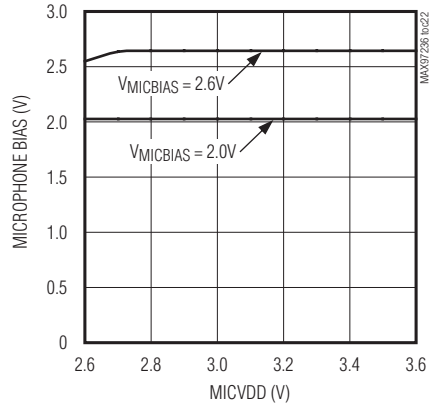
MICROPHONE AMPLIFIER GAIN vs. FREQUENCY



MICROPHONE BIAS vs. TEMPERATURE

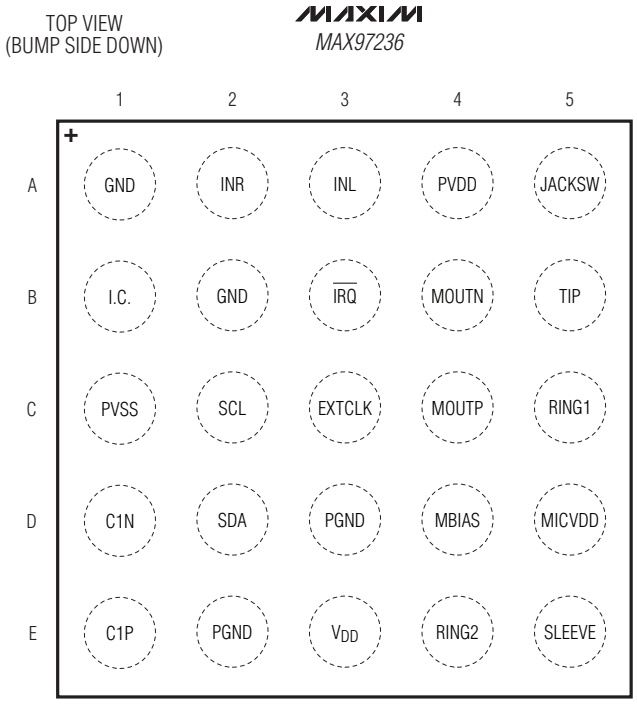


MICROPHONE BIAS vs. MICVDD



Audio Amplifier with Jack Detection

Pin Configuration



WLP

Pin Description

BUMP	NAME	FUNCTION
A1, B2	GND	Analog Ground
A2	INR	Right Audio Input
A3	INL	Left Audio Input
A4	PVDD	Charge-Pump Positive Output. Bypass to PGND with 1µF.
A5	JACKSW	Jack Switch. Connect to the mechanical switch.
B1	I.C.	Internally Connected. Leave unconnected.
B3	$\overline{IRQ}$	Interrupt Request Flag. Open-drain, active-low digital output. Pullup with 10kΩ to system logic voltage.
B4	MOUTN	Negative Microphone Output
B5	TIP	Left Headphone Output. Connect to the first ring of the four-pole jack.
C1	PVSS	Charge-Pump Negative Output. Bypass to PGND with 1µF.
C2	SCL	I²C Serial-Clock Input
C3	EXTCLK	External System Clock Input. All internal digital clocks are derived from EXTCLK.

Pin Description (continued)

BUMP	NAME	FUNCTION
C4	MOUTP	Positive Microphone Output
C5	RING1	Jack Input 2/Right Headphone Output. Connect to the first ring of the four-pole jack.
D1	C1N	Charge-Pump Flying Capacitor Negative Connection. Connect 1µF between C1N and C1P.
D2	SDA	Serial-Data I/O
D3, E2	PGND	Power Ground. Ground Return for the charge pump.
D4	MBIAS	Microphone Bias Capacitor Connection. Connect 1µF to GND.
D5	MICVDD	Microphone Power-Supply Input. Bypass to GND with 1µF.
E1	C1P	Charge-Pump Flying Capacitor Positive Connection. Connect 1µF between C1N and C1P.
E3	V_{DD}	Main Power-Supply Input. Connect to 1.8V and bypass to GND with 1µF.
E4	RING2	Microphone Input Headset GND. Connect to the second ring of the four-pole jack.
E5	SLEEVE	Microphone Input Headset GND. Connect to the sleeve of the four-pole jack.

Detailed Description

Class H DirectDrive Headphone Amplifier with Dual-Mode Charge Pump

The headphone amplifier is optimized for low-power consumption and low noise. A charge pump generates a negative and positive supply voltage that powers the headphone amplifier and eliminates the need for a large output coupling capacitor.

The headphone amplifier has volume control from -60dB to +6dB. A single-pole filter, f_{-3dB} = 85kHz, attenuates signals outside the audio band.

Dual-Mode Charge Pump

The charge pump powers the headphone amplifier. When a headphone load is connected and the audio output signal is small, the charge pump outputs a ±0.9V negative and positive supply voltage. When a large audio signal is applied, the output rails of the charge pump switch to a higher voltage mode, ±1.8V. The higher voltage rails accommodate the higher voltage swing necessary to amplify line level audio signals. The lower voltage rails reduce the power consumption of the headphone amplifier when higher rails are not needed.

Class H Operation

The Class H amplifier employs a class AB output stage with power-supply voltages that shift based on the output signal needs (Figure 1). The lower power supply rails are used when the output voltage requirements are below the 0.5V threshold. The higher supply rails are used when the output voltage is above the 0.5V threshold, maximizing output power and voltage swing. The switch between available power-supply voltages occurs on a cycle-by-cycle basis.

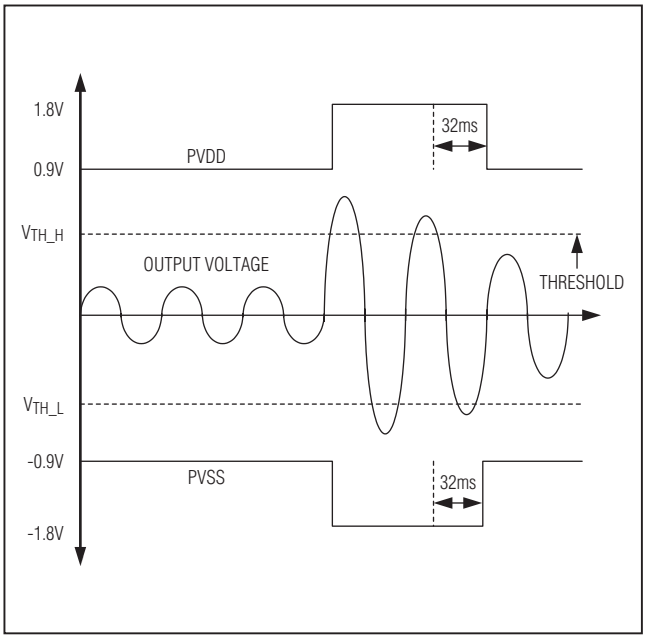


Figure 1. Class H Power-Supply Operation

Audio Amplifier with Jack Detection

Audio Short-Circuit Protection

A short on the right audio output does not shut down the left audio channel. A short on the audio output does not shut down the right audio channel. This ensures that a mono audio plug does not damage the chip, but allows audio to be heard through the other channel output. A short is considered anything below 4Ω for a time period of 100ms.

Ground Sense

The headphone amplifier features output ground sensing for improved crosstalk performance. Crosstalk is improved by at least 20dB, between the audio channels, which all share a common jack ground. Figure 2 shows the audio signal path from the filter through the amplifier with volume control and the ground sense.

Headphone Amplifier Input Filter

The headphone amplifiers employ a lowpass filter to remove out-of-band noise from the audio DAC driving the headphone inputs. The filter attenuates frequencies above 85kHz.

Headphone Amplifier Volume Control

The IC features a 64-step volume control with a resolution of 1dB/step from +6dB down to -54dB and 2dB/step from -54dB to -60dB. Figure 3 shows the I/O curve of the volume control.

Headphone Volume Slewing

Volume slewing breaks up large volume changes into the smallest available step size as it goes through each gain level between the initial and final volume setting. Volume slewing also occurs at device turn-on and turn-off when enabled. During turn-on, the volume is set to mute before the output is enabled. Once the output is on, the volume ramps to the programmed level. At turn-off, the volume is ramped to mute before the output is disabled.

As briefly described in the last section, the $\overline{VSEN}$ (volume slew enable) bit decides whether each volume step is used when changing volume settings or whether the final volume setting jumps to the new value after writing. The volume slew enable function is used in conjunction with the zero-crossing detection enable ($\overline{ZDEN}$).

Examples:

$\overline{VSEN}$ = 0, $\overline{ZDEN}$ = 0, both functions on: The volume changes one gain step at a time. The gain only changes at the zero crossing of the audio signal.

$\overline{VSEN}$ = 0, $\overline{ZDEN}$ = 1: The volume changes one gain step at a time.

$\overline{VSEN}$ = 1, $\overline{ZDEN}$ = 0: New volume is asserted as soon as audio signal has gone through a zero crossing (or 100ms after the last gain change, whichever comes first).

$\overline{VSEN}$ = 1, $\overline{ZDEN}$ = 1: New volume is asserted as soon as the I²C command is received.

Headphone Volume Zero-Crossing Detection

Zero-crossing detection is implemented on the headphone amplifier volume control to prevent large glitches when volume changes are made. Instead of making a volume change immediately when requested, the change is made when the audio signal has a zero crossing or after 100ms, whichever comes first.

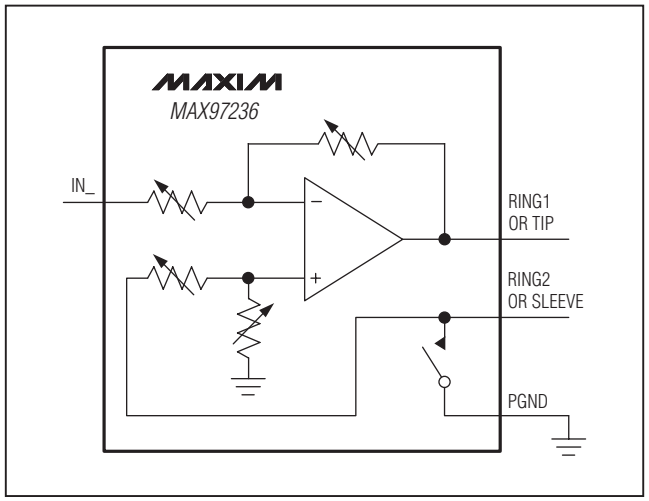


Figure 2. Headphone Amplifier Signal Path

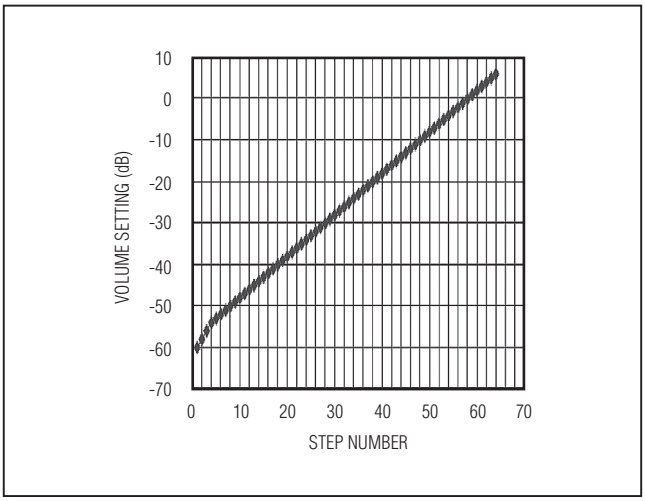


Figure 3. Headphone Volume Control Input/Output Transfer Function

Microphone Bias

The IC features a low-noise microphone bias generator and amplifier. The bias voltage resistors are selectable through I²C register 0x09.

Ensure that V_{MICVDD} is greater than the desired microphone bias voltage.

The microphone bias line is also used by passive single button and passive multibutton headsets.

Microphone Preamplifier

A microphone preamplifier provides an additional gain of 12dB or 24dB (programmable) with low input-referred noise and high power-supply rejection. Figure 4 shows the configuration of the microphone bias, amplifier, and microphone. Internal AC-coupling capacitors connect both the microphone output and also the MBIAS line to a differential amplifier, giving improved PSRR.

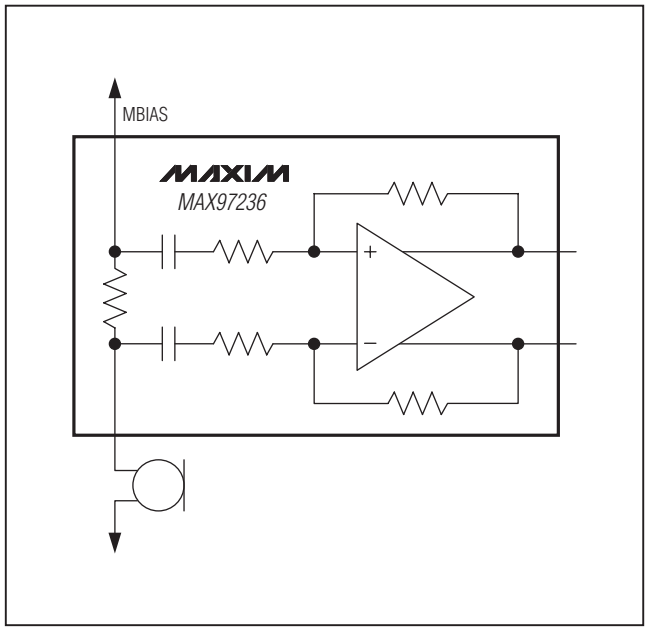


Figure 4. Microphone Preamplifier Simplified Schematic

Jack Detection and Configuration Algorithm

The IC features a detection scheme that senses when a 3.5mm plug is inserted into the system jack. After sensing insertion, a configuration detection algorithm takes over and reads the makeup of the installed plug. Information regarding the makeup of the plug is reported back through the I²C status registers. The device can also be placed in autoconfigure mode. This mode allows the IC to automatically enable the correct functional blocks depending upon the class of cable that has been inserted.

Jack Insertion Testing

The jack insertion detection uses an inaudible AC waveform output on the jack pins to sense when a load is plugged in. This electrical test is used to verify and work in conjunction with a mechanical switch (JACKSW). The mechanical switch, while not used as the main sensing mechanism, can be used to save system power. When a jack is plugged into a device, the switch at JACKSW is closed. When no jack is plugged in, the switch at JACKSW is open. When the jack switch at JACKSW is working, the electrical polling of the jack can be done less often. A test is done every time a jack is sensed to check if the switch at JACKSW is working correctly. If the IC deems that the switch at JACKSW is broken, the system is flagged. At that point, the system can decide whether to ignore JACKSW results and poll more quickly.

Jack Configuration Detection

The jack detection and configuration is bounded by certain load resistance and capacitance limitations. The correct detection and configuration cannot be guaranteed outside those limitations. The limitations are shown in Table 1.

Table 1 shows each load case that is detectable with the IC's jack configuration algorithm and which class of cable is found. The status bits of the I²C register (0x01, 0x02, 0x03) report the load found during testing. The functional blocks are set automatically if AUTO = 10 or 01 (register 0x01E bits 0 and 1), according to what class of cable is detected.

Table 1. Jack Detection and Configuration Load Limits

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Cable Shield Capacitance	C_{CABLE}	150		500	pF
Headphone Load Resistance	R_{HP}	12		650	Ω
Headphone Load Inductance	L_{HP}	30		1600	µH
Audio Line Load Resistance	R_{LINE}	6		50	kΩ
Microphone Load Resistance	R_{MIC}	0.5		15	kΩ

Audio Amplifier with Jack Detection

Case 9 is a special case that requires subsequent testing of the load pins while servicing the left audio load that has been found. In this case only, the status bits report that a line level audio load had been found on TIP while tests continue to run on RING1 and SLEEVE. Once a load is found with one of the subsequent tests, enough information about the cable class is known to stop testing. The status bits reflect what is found, and the signal paths are configured according to the cable class and testing stops.

Detecting Jack Removal

There are two main jack removal detection methods: an electrical method and a mechanical method. The electrical unplug detection method varies, depending on which load is plugged in. Cases with a microphone wait for the microphone bias to fly up to its full value. The audio only headphones wait for SLEEVE to fly up when the jack is removed.

For cases with an AV cable and audio only connected, the IC can only rely on JACKSW to sense removal or to wait for user input to shut down audio.

The electrical unplug detection (JKIN bit) is not available when the IC is running the jack configuration algorithm, when in FORCE mode, or when in test mode. In those cases, an unplug can only be detected mechanically through the JACKSW bit.

Table 2. Jack Configurations and Status Registers (After DDONE Bit Has Been Reset)

CASE NO.	CABLE CLASS	PINS				JACKSW STATE	REGISTER 0x00	REGISTER 0x01	REGISTER 0x02
		1	2	3	4				
1	Nothing	F	F	F	F	Short	0x00	0x00	0x00
2	Extension cable	C	C	C	C	Open	0x84	0x00	0x00
3	Stereo headset (headphones with microphone), GND on P3	L	R	G	M	Open	0x8C	0x30	0x01
4	Stereo headset (headphones with microphone), GND on P4	L	R	M	G	Open	0x8C	0x30	0x02
5	Line audio cable	L	R	G	G	Open	0x84	0xC0	0x03
6	Mono headset, GND on P3	L	G	G	M	Open	0x8C	0x20	0x01
7	Mono headset, GND on P4	L	G	M	G	Open	0x8C	0x20	0x02
8	Mono headset, GND on P3	L	L	G	M	Open	0x8C	0x20	0x01
9	Mono headset, GND on P4	L	L	M	G	Open	0x8C	0x20	0x02
10	Mono headset, GND on P3	L	F	G	M	Open	0x8C	0x20	0x01
11	Mono headset, GND on P4	L	F	M	G	Open	0x8C	0x20	0x02
12	Stereo headphones	L	L	G	G	Open	0x84	0x30	0x03
13	Stereo headphones, right channel open	L	F	G	G	Open	0x84	0x20	0x03
14	Stereo headphones, left channel open	F	L	G	G	Open	0x84	0x10	0x03

Key Switch Encoder

There are two types of keypads that can be connected to the IC:

- A single-button hook switch or MIC switch that grounds out the microphone bias when pressed
- A passive multibutton headset

Key Switch Encoder Timing

Two registers, 0x15 and 0x16, control the key switch debounce time, t_{DEB}, and delay time, t_{DELAY}.

The debounce time, 0x15, is the time from when the switch stops bouncing and when the ADC converts.

The delay time, 0x16, is set long to ensure that an unplug event is not encoded as a keypress. See Figure 9.

The PRESS Bit

The PRESS bit alerts the system to whether the current interrupt was caused by a button press or release.

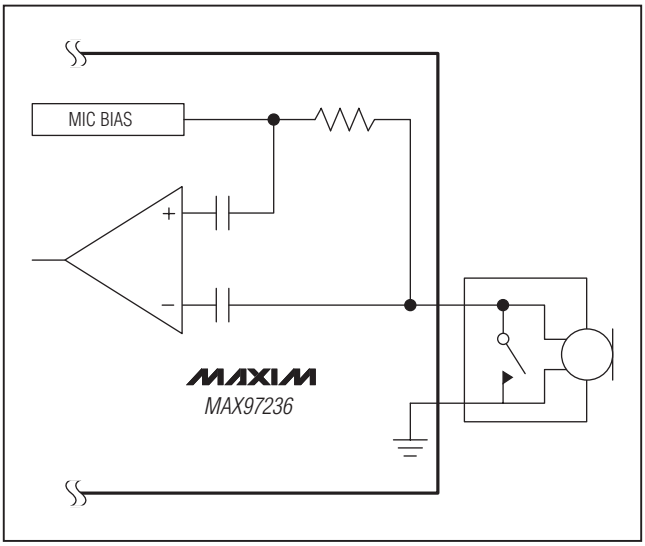


Figure 5. Passive Single-Button Hook Switch

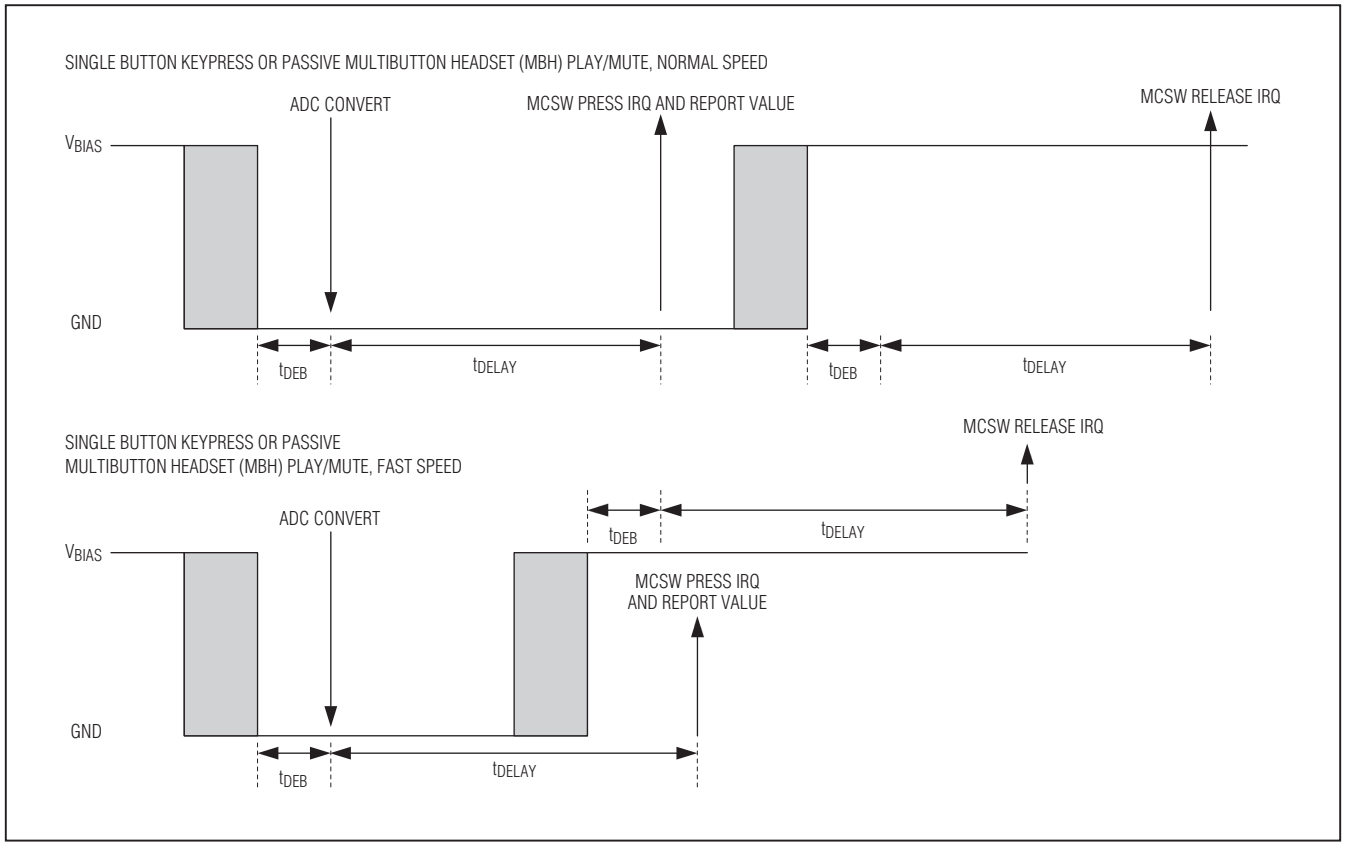


Figure 6. Single-Button, Passive Multibutton Hook Switch/Microphone Switch Timing

Audio Amplifier with Jack Detection

Passive Multibutton Headset (MBH)

A passive MBH consists of a microphone with numerous switches that connect different value resistors to ground. The switched resistor and the microphone bias resistor set up a voltage-divider that creates a unique voltage. The on-chip ADC then encodes the voltage and reports to the system.

A maximum 0.5Ω resistance between IC pins RING2 and SLEEVE and the headset is required for proper operation of the passive multibutton headset.

Figure 7 shows the circuit diagram of a passive MBH.

Figure 8 shows the timing for a fast or normal speed keypress on a passive MBH. Note that a keypress develops a voltage that is above ground. The switch that shorts the microphone bias to ground is handled like the hook switch in the previous section.

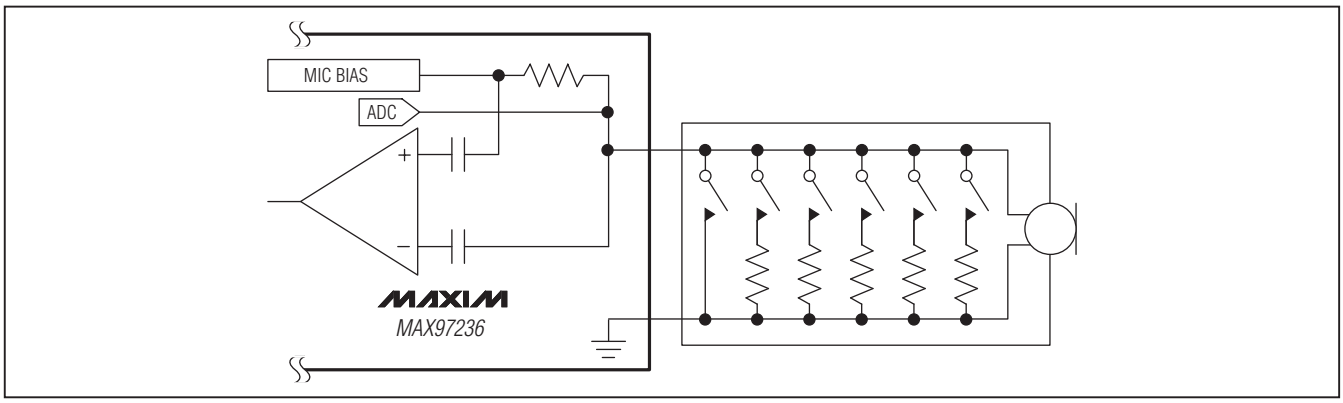


Figure 7. Passive MBH

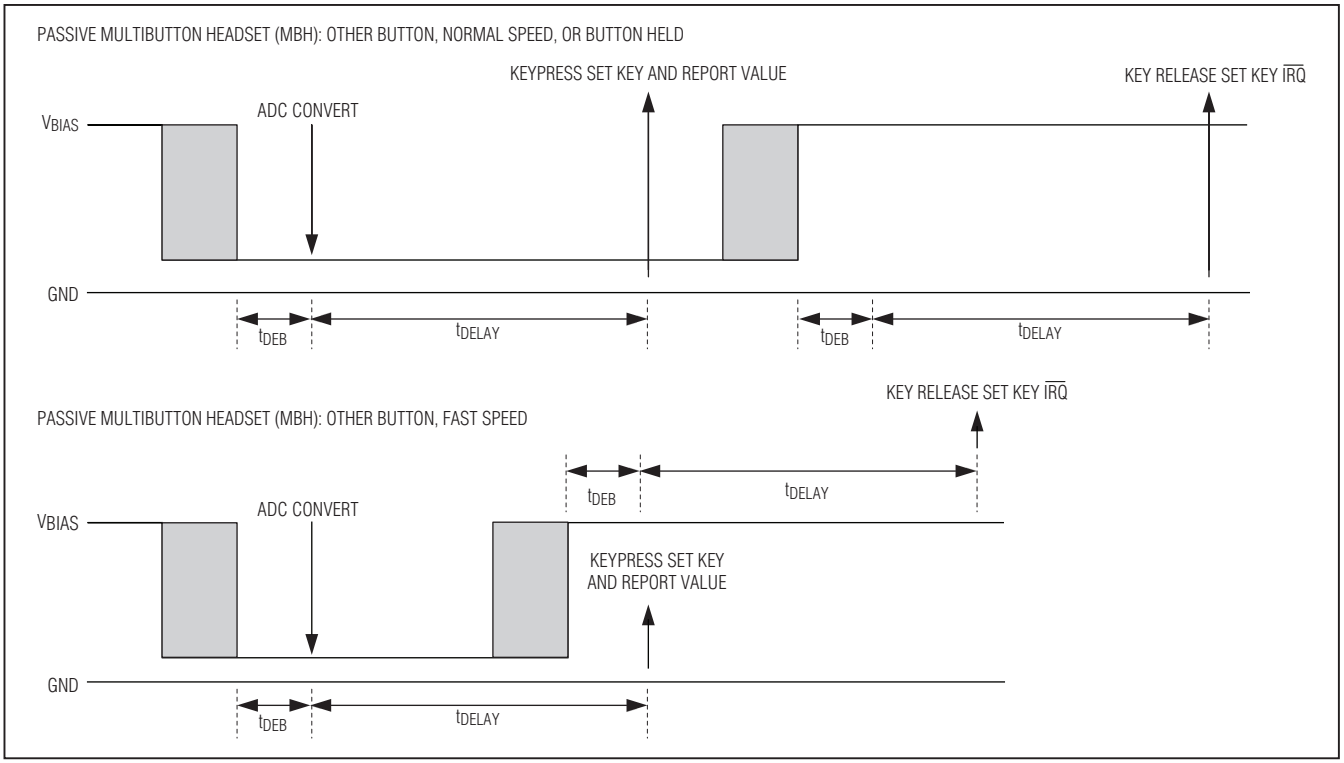


Figure 8. MBH Timing

Slow Jack Removal

Removing the headphone jack slowly can cause a false trigger of the key switch encoder because the right speaker between RING1 and RING2 shorts between microphone bias and ground. The programmable delay time must be set by the system to mask out this slow removal so that an interrupt does not flag until the JKIN status bit tells the system the jack is unplugged. Figure 9 shows the timing and interrupt reporting for a slow jack removal event. The act of microphone bias flying all the way up is the trigger for a microphone removal event. The *Jack Detection and Configuration Algorithm* section explains more about sensing jack removal.

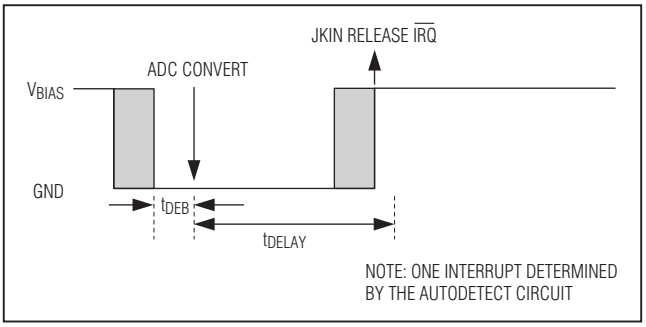


Figure 9. Slow Jack Removal Timing

Register and Bit Descriptions

Table 3. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W
Status1	JKIN	DDONE	VOL	—	MIC_IN	JACKSW	MCSW	MBH	0x00	0x00	R
Status2	LINE_L	LINE_R	HP_L	HP_R	JACKSWINC	KEY	—	—	0x01	0x00	R
Status3	—	—	—	—	—	—	GND		0x02	0x00	R
For Expansion	—	—	—	—	—	—	—	—	0x03	—	—
IRQ Mask1	IJKIN	IDDONE	IVOL	—	IMIC	JACKSW	IMCSW	IMBH	0x04	0x00	R/W
IRQ Mask2	ILINE_L	ILINE_R	IHP_L	IHP_R	IJACKSW	IKEY	—	—	0x05	0x00	R/W
For Expansion	—	—	—	—	—	—	—	—	0x06	—	—
Left Volume	L = R	MUTEL	LVOL						0x07	0xC0	R/W
Right Volume	—	MUTER	RVOL						0x08	0x40	R/W
Microphone	—	GAIN	MICR			BIAS	—	—	0x09	0x00	R/W
For Expansion	For expansion								0x0A	0x00	R/W
Vendor ID Register	ID				—	—	—	—	0x0B	0x90	R
For Expansion	For expansion								0x0C	0x00	R/W
For Expansion	For expansion								0x0D	0x00	R/W
For Expansion	For expansion								0x0E	0x00	R/W
For Expansion	For expansion								0x0F	0x00	R/W
For Expansion	For expansion								0x10	0x00	R/W
For Expansion	For expansion								0x11	0x00	R/W
Keyscan Clock Divider 1	KEY_DIV_HIGH								0x12	0x00	R/W
Keyscan Clock Divider 2	KEY_DIV_LOW								0x13	0x00	R/W
Keyscan Clock Divider ADC	KEY_DIV_ADC								0x14	0x00	R/W
Keyscan Debounce	KEY_DEB								0x15	0x00	R/W
Keyscan Delay	KEY_DEL								0x16	0x00	R/W

Audio Amplifier with Jack Detection

Table 3. Register Map (continued)

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W
Passive MBH Keyscan Data	PRESS	RANGE	KEYDATA						0x17	0x00	R
DC Test Slew Control	DC_SLEW								0x18	0x00	R/W
State Forcing	—	—	$\overline{FORCE}$	STATE				—	0x19	0x20	R/W
AC Test Control	—	—	AC_REPEAT_		PULSE_WIDTH_		PULSE_AMP_		0x1A	0x05	R/W
For Expansion	—	—	—	—	—	—	—	—	0x1B	—	—
For Expansion	—	—	—	—	—	—	—	—	0x1C	—	—
Enable1	$\overline{SHDN}$	RESET	—	MIC_ BIAS	MIC_AMP	KS	—	—	0x1D	0x00	R/W
Enable2	LFTEN	RGHEN	$\overline{VSEN}$	$\overline{ZDEN}$	FAST	THRH	AUTO		0x1E	0x00	R/W

Device Status Registers

Registers 0x00 and 0x01 are used to report the makeup of the inserted jack as well as report when a microphone switch has been pressed or the jack has been removed. The IC uses registers 0x00, 0x01, 0x02, and $\overline{IRQ}$ to report the status of various device functions. The Status_ register bits are set when their respective event occurs. Device status can be determined either by polling registers 0x00, 0x01, and 0x02 or configuring the $\overline{IRQ}$ to go low when specific events occur. Registers 0x04 and 0x05 determine which bits in the Status_ register trigger $\overline{IRQ}$ to go low. $\overline{IRQ}$ is cleared upon reading the register.

Table 4. Configuration and Device Status Registers

REGISTER	BIT	NAME	DESCRIPTION
Status1 0x00 (Read Only)	7	JKIN	**Jack Detected** JKIN changes state when the jack detect circuit senses a load at the left headphone output and $\overline{SHDN}$ = high 0 = No load at TIP. 1 = Load detected at TIP.
	6	DDONE	**Jack Configuration Detect Done** DDONE changes state when the jack detect algorithm finishes and the jack configuration is known and reported in the status registers 0x00, 0x01, and 0x02. **Resets after reading.** 0 = Jack detect algorithm is not complete. 1 = Jack detection algorithm is complete.
	5	VOL	**Volume Slew Complete** VOL goes high after the headphone volume has slewed to its final programmed value. VOL sets every time a gain change is complete whether the gain change is positive or negative. Ramp the volume down and wait for VOL to set to ensure clickless turn off. **Resets after reading.** 0 = No volume slewing sequences have completed since any register was last read. 1 = Volume slewing complete.
	4	—	—

Table 4. Configuration and Device Status Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
Status1 0x00 (Read Only)	3	MIC_IN	**Microphone Connected/Disconnected** MIC_IN reports when a microphone is connected or removed. Set the MIC_INM interrupt mask to alert the system when the microphone load status has changed. 0 = Microphone is removed. 1 = Microphone is connected.
	2	JACKSW	**JACKSW Status** JACKSW reports the mechanical jack switch status. For an operational mechanical jack switch, JACKSW flags at the same time. If the switch is broken, or if the jack is not plugged in all the way, JACKSW and JKIN do not report the same value. The JACKSW bit also reports when a jack has been removed. Set the PIN5M interrupt mask bit to signal the system when the status of JACKSW changes. 0 = Mechanical jack switch reports no jack is connected. 1 = Mechanical jack switch shows that the jack is connected.
	1	MCSW	**Microphone Switch Status** MCSW goes high when the microphone bias goes low for the debounce period plus the delay period. This happens when a switch shorts across the microphone, pulling the micbias node down, indicating a keypress from a hook switch, ADC ≤ 4 LSB. **Resets after reading.** 0 = No change in microphone bias, no switch press. 1 = Microphone bias has been pulled to ground and debounced since the last status read. Debounce time set by KEY_DEB. Delay time set by KEY_DEL.
	0	MBH	**Multibutton Headset Status** MBH reports when a keypress from a multibutton headset is ready to be read. **Resets after reading.** 0 = No active keypress detected. 1 = Active keypress has been detected.
Status2 0x01 (Read Only)	7	LINE_L	**Line-Level Load on TIP Detected** 0 = Line-level load on TIP not detected. 1 = Line-level load on TIP detected.
	6	LINE_R	**Line-Level Load on ROUT Detected** 0 = Line-level load on RING1 not detected. 1 = Line-level load on RING1 detected.
	5	HP_L	**Headphone Load on TIP Detected** 0 = Headphone load on TIP not detected. 1 = Headphone load on TIP detected.
	4	HP_R	**Headphone Load on RING1 Detected** 0 = Headphone load on RING1 not detected. 1 = Headphone load on RING1 detected.
	3	JACKSWINC	**JACKSW Incorrect** JACKSWINC reports when there are inconsistencies between the mechanical switch and the electrical plug and unplug detection. The exception is when a plug-in occurs and $\overline{SHDN}$ is LOW. **JACKSWINC does NOT clear when the STATUS register is read. JACKSW is checked at jack plug-in and unplug JACKSWINC is updated when JACKSW is checked.** 0 = JACKSW reporting is correct and correlates with JKIN. 1 = JACKSW reporting is not correct and does not correlate with JKIN.

Table 4. Configuration and Device Status Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
Status2 0x01 (Read Only)	2	KEY	**Passive Multibutton Headset KEY Status** KEY reports when the passive multibutton has been pressed. Data is available in KEYDATA. See Figure 8. **Resets after reading.** 0 = No button pressed. 1 = Button has been pressed/released. Debounce and delay times have occurred.
	1	—	—
	0	—	—
Status3 0x02 (Read Only)	7	—	—
	6	—	—
	5	—	—
	4	—	—
	3	—	—
	2	—	—
	1	GND	**Jack Common Location Identifier** The two GND bits tell the system whether the jack's common connection is at RING2 or SLEEVE. GND is also used to indicate when a jack has been removed. 00 = No common connection sensed, jack has been removed or nothing has been inserted yet. 01 = The common jack connection is RING2. 10 = The common jack connection is SLEEVE. 11 = Common on both RING2 and SLEEVE.
	0		

Interrupt Mask Registers

The Interrupt Mask registers control which status bits flag a system interrupt. Setting an interrupt mask bit causes $\overline{IRQ}$ to pull low whenever the target status bits set. The $\overline{IRQ}$ output resets to high, after I^2C register is read.

Table 5. Interrupt Mask Registers

REGISTER	BIT	NAME	DESCRIPTION
IRQ Mask1 0x04	7	IJKIN	**Jack Detect Interrupt Enable** 0 = Disabled 1 = Enabled
	6	IDDONE	**Jack Configuration Detect Done Interrupt Enable** 0 = Disabled 1 = Enabled
	5	IVOL	**Volume Slew Interrupt Enable** 0 = Disabled 1 = Enabled
	4	—	—
	3	IMIC	**Microphone Interrupt Enable** 0 = Disabled 1 = Enabled
	2	JACKSW	**JACKSW Status Interrupt Enable** 0 = Disabled 1 = Enabled
	1	IMCSW	**Microphone Switch Interrupt Enable** 0 = Disabled 1 = Enabled
	0	IMBH	**Multibutton Release Status Interrupt Enable** 0 = Disabled 1 = Enabled
IRQ Mask2 0x05	7	ILINE_L	**Line-Level Load TIP Interrupt Enable** 0 = Disabled 1 = Enabled
	6	ILINE_R	**Line-Level Load RING1 Interrupt Enable** 0 = Disabled 1 = Enabled
	5	IHP_L	**Headphone Load TIP Interrupt Enable** 0 = Disabled 1 = Enabled
	4	IHP_R	**Headphone Load RING1 Interrupt Enable** 0 = Disabled 1 = Enabled
	3	IJACKSW	**JACKSW Incorrect Interrupt Enable** 0 = Disabled 1 = Enabled
	2	IKEY	**KEY Interrupt Enable** 0 = Disabled 1 = Enabled
	1	—	—
	0	—	—

Audio Amplifier with Jack Detection

Headphone Volume Control Registers

The Headphone Volume registers independently control and report the gain of the left and right headphone amplifiers. Set B7 in Register 0x04 to have the right-channel gain track the left-channel gain.

Table 6. Headphone Volume Registers

REGISTER	BIT	NAME	DESCRIPTION			
Left Volume 0x07	7	L = R	**Left/Right Tracking** 0 = The right-channel volume control is independent of the left. 1 = The left and right volume controls track each other allowing for only one register to be written to change both channel volumes. Control both volume controls by writing to LVOL.			
Left Volume/ Right Volume 0x07/0x08	6	MUTEL/ MUTER	**Headphone Mute** 0 = Disable. 1 = Enable, output is muted.			
	5	LVOL/ RVOL	**Left/Right Headphone Output Volume Level**			
			HEX VALUE	**GAIN (dB)**	**HEX VALUE**	**GAIN (dB)**
			0x00	-60	0x20	-25
			0x01	-58	0x21	-24
			0x02	-56	0x22	-23
	4		0x03	-54	0x23	-22
			0x04	-53	0x24	-21
			0x05	-52	0x25	-20
			0x06	-51	0x26	-19
			0x07	-50	0x27	-18
			0x08	-49	0x28	-17
	3		0x09	-48	0x29	-16
			0x0A	-47	0x2A	-15
			0x0B	-46	0x2B	-14
			0x0C	-45	0x2C	-13
			0x0D	-44	0x2D	-12
			0x0E	-43	0x2E	-11
	2		0x0F	-42	0x2F	-10
			0x10	-41	0x30	-9
			0x11	-40	0x31	-8
			0x12	-39	0x32	-7
			0x13	-38	0x33	-6
			0x14	-37	0x34	-5
	1		0x15	-36	0x35	-4
			0x16	-35	0x36	-3
			0x17	-34	0x37	-2
			0x18	-33	0x38	-1
			0x19	-32	0x39	0
			0x1A	-31	0x3A	1
	0		0x1B	-30	0x3B	2
			0x1C	-29	0x3C	3
			0x1D	-28	0x3D	4
			0x1E	-27	0x3E	5
			0x1F	-26	0x3F	6

Microphone Bias Control and Gain Register

The Microphone Bias Control and Gain register controls which microphone bias voltage and bias resistors are used as well as the microphone amplifier gain.

Table 7. Microphone Bias and Gain Register

REGISTER	BIT	NAME	DESCRIPTION
Microphone 0x09	7	—	—
	6	GAIN	**Microphone Preamplifier Gain Select** 0 = 12dB 1 = 24dB
	5	MICR	**Microphone Bias Resistor Select** 000 = 2.2kΩ 001 = 2.6kΩ 010 = 3.0kΩ 011 = Bypassed 1XX = High impedance (sleep mode)
	4		
	3		
	2	BIAS	**Microphone Bias Voltage Select** 0 = 2.0V 1 = 2.6V
	1	—	—
	0	—	—

Vendor ID Register

Vendor ID bits are shown in Table 8.

Table 8. Vendor ID Register

REGISTER	BIT	NAME	DESCRIPTION
Vendor ID Register 0x0B	7	ID	**Vendor ID** 0x9 = Maxim's vendor ID
	6		
	5		
	4		
	3	—	—
	2	—	
	1	—	
	0	—	

Audio Amplifier with Jack Detection

Keyscan Clock Divider Registers

The Keyscan Clock Divider register sets the clock frequency that is used for the conversion clock for the keyscan 1kHz generator.

Table 9. Keyscan Clock Divider Registers

REGISTER	BIT	NAME	DESCRIPTION
Keyscan Clock Divider 1/2 0x12/0x13	7	KEY_DIV_HIGH/ KEY_DIV_LOW	**Keyscan Clock Divider** The keyscan 1kHz clock is generated by dividing down the frequency of EXTCLK. The divider is set with the 16 bits contained within registers 0x12 and 0x13, where 0x12 is the high byte and 0x13 is the low byte. Since 1kHz (1ms) is desired, then: $N = f_{IN}/2kHz$ e.g., f_{IN} = 20MHz, then N = 10,000 e.g., f_{IN} = 1MHz, then N = 500 e.g., f_{IN} = 19.2MHz, then N = 9600 For the low input frequencies, resolution is about 0.2%.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Keyscan Divider ADC Register

The Keyscan ADC Clock Divider register sets the clock frequency that is used for the conversion clock for the keyscan 6-bit ADC.

Table 10. Keyscan ADC Clock Divider Registers

REGISTER	BIT	NAME	DESCRIPTION
Keyscan Clock Divider ADC 0x14	7	KEY_DIV_ADC	**Keyscan ADC Clock Divider** The keyscan ADC clock is generated by dividing down the frequency of EXTCLK. The divider is set with the 8 bits contained within register 0x14. Since 100kHz (10µs) is desired, then: $N = f_{IN}/200kHz$ e.g., f_{IN} = 20MHz, then N = 100 e.g., f_{IN} = 1MHz, then N = 5 e.g., f_{IN} = 19.2MHz, then N = 96 For the low input frequencies, resolution is about 20%.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Keyscan Debounce Register

The Keyscan Debounce register controls the debounce time when a keypress is detected. See Figure 6.

Table 11. Keyscan Clock Divider Registers

REGISTER	BIT	NAME	DESCRIPTION
Keyscan Debounce 0x15	7	KEY_DEB	**Keyscan Debounce Register** Debounce time set from 1ms to 256ms in 1ms increments. The programmed code plus one represents the debounce time directly. t_{DEB} = KEY_DEB + 1 e.g., code 0x13 represents 20ms of debounce.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Keyscan Delay Register

The Keyscan Delay register sets the timeout that the microphone button press is masked from the system. At the end of the delay time, the IC checks to see if a microphone is still present. If the microphone is present, the system is alerted by setting the MCSW bit in the status register flagging an interrupt if IMCSW is set. If the microphone is not present after the delay time, the system is flagged with an interrupt by setting MICROPHONE_IN signifying that the microphone has been removed and no keypress was made.

Table 12. Keyscan Delay Register

REGISTER	BIT	NAME	DESCRIPTION
Keyscan Delay 0x16	7	KEY_DEL	**Keyscan Delay Register** Delay time set from 4ms to 1024ms in 4ms increments. The programmed code plus one multiplied by 4ms represents the delay time. tDELAY = (KEY_DEL + 1) x 4ms e.g., code 0x63 represents 400ms of delay.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Passive Multibutton Keyscan Data Register

The Keyscan Data register contains the data read from a keypress after the 6-bit ADC encodes the input voltage level. The read keypress could come from a single switch or a passive multibutton device.

Table 13. Keyscan Data Register

REGISTER	BIT	NAME	DESCRIPTION
Passive MBH Keyscan Data 0x17 (Read Only)	7	PRESS	**Release** Tells if a KEY status was PRESS or RELEASE. 0 = Key release. 1 = Keypress.
	6	RANGE	0 = Coarse range. 1 = Fine range.
	5	KEYDATA	**Keyscan Data** B6–B0 are read-only bits that contain the data read from a passive keypress that shorts the microphone to ground. There is a coarse range (10mV/LSB) and a fine range (2mV/LSB). See Figure 7 and the *Passive Multibutton Headset (MBH)* section.
	4		
	3		
	2		
	1		
	0		

Audio Amplifier with Jack Detection

Ramp Test Slew Control

The ramp test slew control programs the period of the jack configuration algorithm's ramp test. Slow slew rates ensure test inaudibility, but increase test time to complete the configuration algorithm.

Table 14. Ramp Test Slew Control

REGISTER	BIT	NAME	DESCRIPTION
DC Test Slew Control 0x18	7	DC_SLEW	**DC Slew Control** Program the DC test slew rate from 5.12ms to 1305.6ms in 5.12ms steps. Recommend value to be used is 0x04 to 0x08.
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Load State Forcing

Use the Load State Forcing register to force a state and ignore the results of the jack detection algorithm. It forces the required blocks to be on (bypassing the Enable registers).

Table 15. Load State Forcing

REGISTER	BIT	NAME	DESCRIPTION
State Forcing 0x19	7	—	—
	6	—	—
	5	$\overline{\text{FORCE}}$	**Load State Force Enable** 0 = Forces the IC into a configuration defined by 0b4–0b0. 1 = State forcing disabled.

Table 15. Load State Forcing (continued)

REGISTER	BIT	NAME	DESCRIPTION	
State Forcing 0x19	4	STATE	**State Value** Bits 0b4–0b0 programs the configuration of the IC. The columns show all the possible configurations.	
			CODE [B4:B0]	**STATE (F = Float, L = Left Audio, R = Right Audio, G = Ground, M = Microphone)**
	3		0x01	FFFF
			0x02	LRGM
			0x03	LRMG
			0x07	LRGG_AC
	2		0x08	LRGF
			0x09	LFGF
			0x0A	FRGF
			0x0C	LGGM
			0x0D	LGMG
	1		0x0E	LLGM
			0x0F	LLMG
			0x10	LFGM
			0x11	LFMG
	0		0x12	LRGG_DC
			0x13	LFGG
			0x14	FRGG

Audio Amplifier with Jack Detection

Pulse Test Hardware Settings

The Jack Detect Test Hardware Settings register programs the amplitude and width of the pulse used in the jack detection tests and jack insertion algorithm.

Table 16. Jack Detect Test Hardware Settings

REGISTER	BIT	NAME	DESCRIPTION
AC Test Control 0x1A	7	—	—
	6	—	—
	5	AC_REPEAT1	**AC_Repeat** 00 = 1, 01 = 3, 10 = 5, 11 = 7. Programs number of pulses sent for each jack detection test.
	4	AC_REPEAT0	
	3	PULSE_WIDTH1	**Pulse Width** 00 = 50µs, 01 = 100µs, 10 = 150µs, 11 = 300µs. Test 1 and 4 pulse width is fixed at 10µs.
	2	PULSE_WIDTH0	
	1	PULSE_AMP1	**Pulse Amplitude** For tests 1 and 4, pulse amplitude is 00 = 25mV, 01 = 50mV, 10 = 100mV, 11 = 200mV. Tests 6, 7, and 8 pulse amplitude is 00 = 37mV, 01 = 75mV, 10 = 150mV, 11 = 220mV.
	0	PULSE_AMP0	

Enable Registers

The Enable_ registers contain all of the bits that control the separate functional blocks for the IC. The system can either directly control these bits, or it can allow the IC to automatically configure itself and report in the Enable_ register which blocks are enabled. When the AUTO bits (B1, B0) are set to 01 or 10, the Enable_ registers are read-only (except the $\overline{SHDN}$ and SLEEP bits). The block enable bits need to be set to sense a jack removal. The jack removal circuitry is active after the jack configurations detect algorithm has completed.

Table 17. Enable Registers

REGISTER	BIT	NAME	DESCRIPTION
Enable1 0x1D	7	$\overline{SHDN}$	**Full Device Shutdown Control** $\overline{SHDN}$ turns the IC on and off. When $\overline{SHDN}$ is low, the device is in shutdown mode and the jack insertion detect circuitry is active. Pull $\overline{SHDN}$ high to turn on the device and run the jack configuration detect algorithm. Typically, $\overline{SHDN}$ is held low until the system gets an interrupt from the IC, indicating that a jack has been inserted. The system then pulls $\overline{SHDN}$ high. 0 = The IC is in shutdown mode with jack detection circuitry active. 1 = The IC is active. The jack configuration algorithm runs immediately after a load has been detected.
	6	RESET	**RESET Jack Detection** Cycle RESET (low → high → low) to repeat the jack detection and configuration algorithm.

Table 17. Enable Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
Enable1 0x1D	5	—	—
	4	MIC_BIAS	**Microphone Bias Enable/Status** Set MIC_BIAS to enable the microphone block. This bit is read-only when AUTO (0b0 or 0b1) is set. 0 = Microphone bias is disabled. 1 = Microphone bias is enabled.
	3	MIC_AMP	**Microphone Amplifier Enable/Status** Set MIC_AMP to enable the microphone amplifier. This bit is read-only when AUTO (0b0 or 0b1) is set. 0 = Microphone amplifiers are disabled. 1 = Microphone amplifiers are enabled.
	2	KS	**Keyscan Enable/Status** KS enables the circuitry that decodes passive multibutton keypad or simple microphone switch. This bit is read only when AUTO (0b0 or 0b1) is set. 0 = Keyscan ADC is disabled. 1 = Keyscan ADC is enabled.
	1	—	—
	0	—	—
Enable2 0x1E	7	LFTEN	**Left Headphone Enable/Status** Set LFTEN to enable the left channel of the DirectDrive headphone amplifier. This bit is read-only when AUTO (0b0 or 0b1) is set. 0 = Headphone amplifier left channel is disabled. 1 = Headphone amplifier left channel is enabled.
	6	RGHEN	**Right Headphone Enable/Status** Set RGHEN to enable the left channel of the DirectDrive headphone amplifier. This bit is read-only when AUTO (B0) is set. 0 = Headphone amplifier right channel is disabled. 1 = Headphone amplifier right channel is enabled.

Table 17. Enable Registers (continued)

REGISTER	BIT	NAME	DESCRIPTION
Enable2 0x1E	5	$\overline{\text{VSEN}}$	**Volume Adjustment Slewing** Volume changes are smoothed by stepping through intermediate steps. $\overline{\text{VSEN}}$ also ensures that the volume automatically ramps from the minimum setting to the programmed value at turn-on and back to the minimum value at turn-off. 0 = Enabled. 1 = Disabled.
	4	$\overline{\text{ZDEN}}$	**Zero-Crossing Detection** $\overline{\text{ZDEN}}$ holds volume changes until there is a zero-crossing in the audio signal. This reduces clicks during volume changes (zipper noise). If no zero-crossing is detected within 100ms, the volume change is forced. 0 = Enabled. 1 = Disabled.
	3	FAST	**Jack Insertion Polling Speed** A fast polling speed tests for a jack insertion 3 times per second, while a slow polling speed tests for jack insertion every 2 seconds. Setting the polling speed to slow mode saves shutdown power consumption while the mechanical JACKSW switch is operational. 0 = Slow polling mode, 2s delay between polls. 1 = Fast polling mode, 333ms delay between polls.
	2	THRH	**Class H Threshold Select** THRH selects the threshold at which the power supplies switch from ±0.9V to ±1.8V. A higher threshold allows the IC's output stage to be powered from ±0.9V for a higher percentage of the audio waveform, decreasing power dissipation at the expense of dynamic distortion. 0 = Low threshold. 1 = High threshold.
	1	AUTO	**Automatic Mode Select** Set AUTO to allow the IC to enable functional blocks depending on the load. In auto mode, the user merely reads the status of registers 0x1D and 0x1E to find out what blocks are enabled. Setting AUTO makes bits register 0x1D and 0x01E read-only (except $\overline{\text{SHDN}}$ and SLEEP). Clear AUTO to give the system control of what functional blocks are active. The user needs to allow the jack configuration detect algorithm to complete before enabling functional blocks. 00 = User controls which functional blocks are on. Registers 0x1D and 0x1E are R/W. 01 = The IC enables functional blocks automatically depending on the results of the jack configuration detect algorithm after $\overline{\text{SHDN}}$ is set. 10 = The IC enables functional blocks automatically depending on the results of the jack configuration detect algorithm regardless of whether $\overline{\text{SHDN}}$ is set. $\overline{\text{SHDN}}$ must go to high to enable audio playback.
	0		

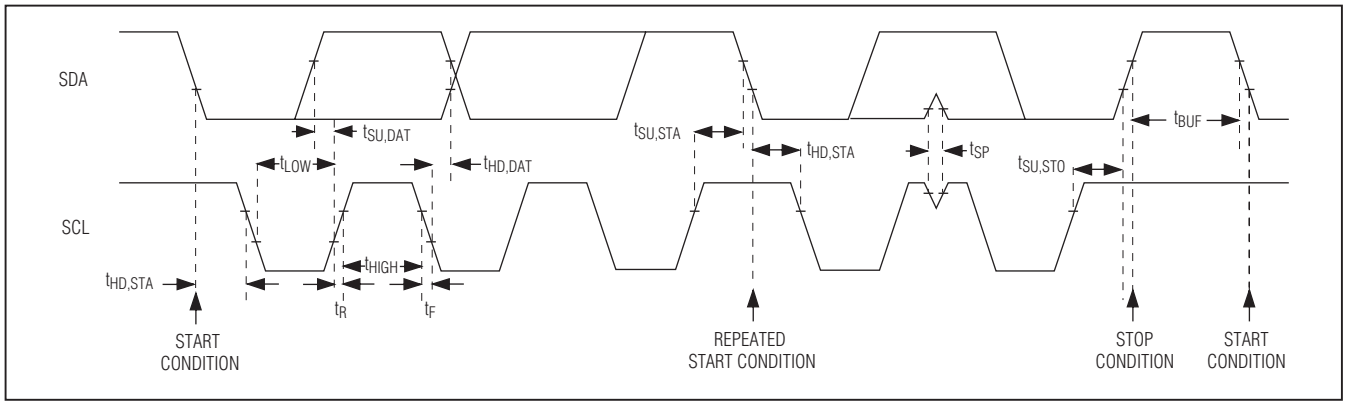


Figure 10. I²C Interface Timing Diagram

I²C Serial Interface

The IC features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. Figure 10 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 11). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

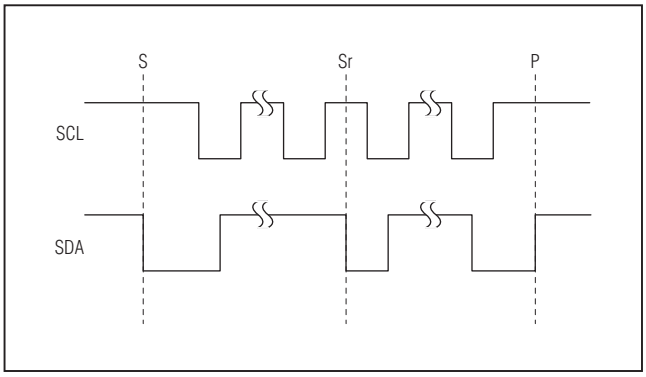


Figure 11. START, STOP, and REPEATED START Conditions

SMBus is a trademark of Intel Corp.

Audio Amplifier with Jack Detection

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. The IC has an address of 0x80. The 7 most significant bits are 100000. Setting the read/write bit to 1 (slave address = 0x81) configures the IC for read mode. Setting the read/write bit to 0 (slave address = 0x80) configures the IC for write mode. The address is the first byte of information sent to the IC after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the IC uses to handshake receipt each byte of data when in write mode (Figure 12). The IC pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

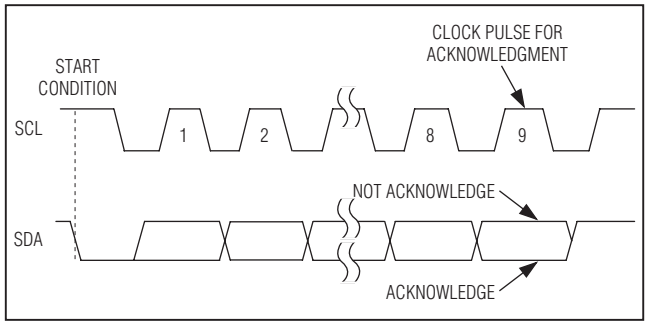


Figure 12. Acknowledge

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 13 illustrates the proper frame format for writing one byte of data to the IC. Figure 14 illustrates the frame format for writing n bytes of data to the IC.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

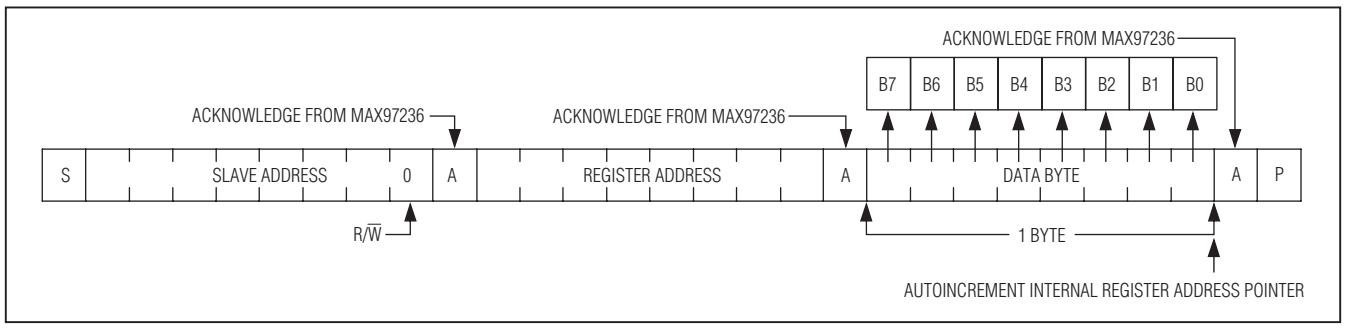


Figure 13. Writing One Byte of Data to the IC

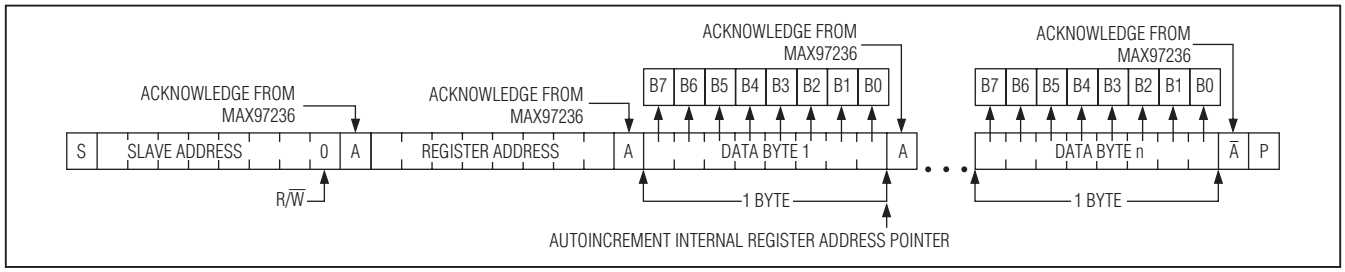


Figure 14. Writing n Bytes of Data to the IC

The third byte sent to the IC contains the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x0C are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the IC is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the IC's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The IC then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 15 illustrates the frame format for reading one byte from the IC. Figure 16 illustrates the frame format for reading multiple bytes from the IC.

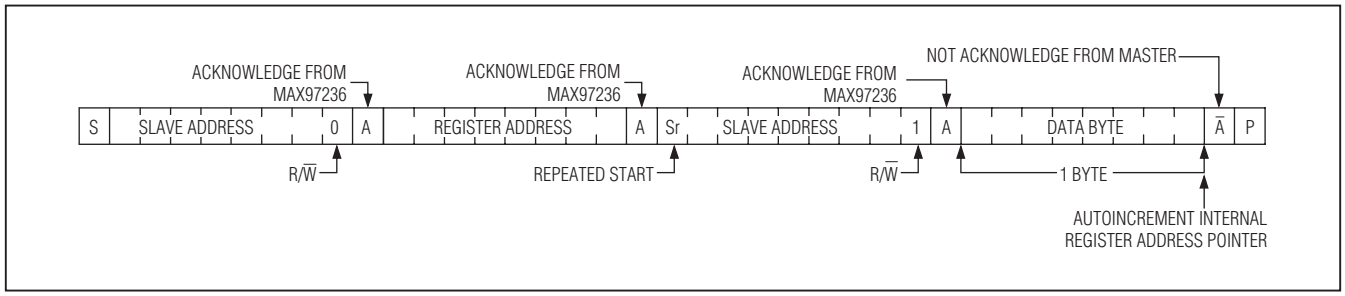


Figure 15. Reading One Byte of Data from the IC

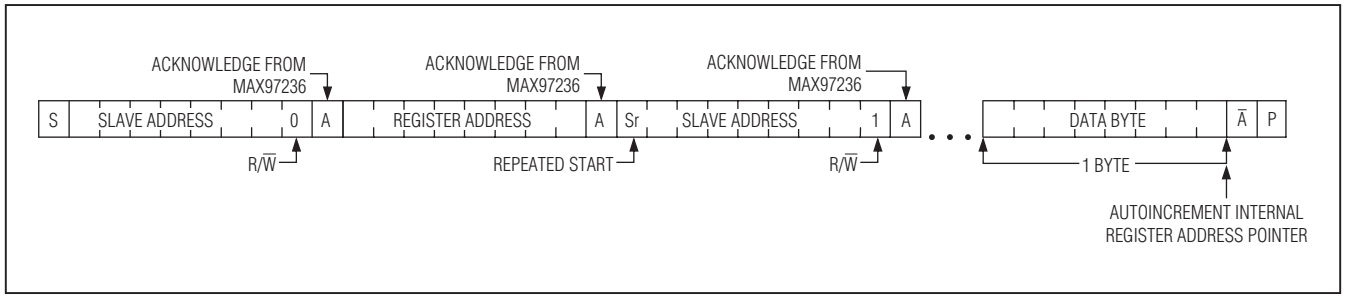


Figure 16. Reading n Bytes of Data from the IC

Audio Amplifier with Jack Detection

Applications Information

Power Modes

The power modes of the IC are controlled by the $\overline{SHDN}$ bit. The three power modes include detection, normal operating, and standby.

Detection mode occurs when no jack has been plugged in, $\overline{SHDN}$ = RESET = 0. Once a jack is plugged in and detected, the IC enters normal operating mode after $\overline{SHDN}$ transitions from 0 to 1. While in normal operating mode, pull $\overline{SHDN}$ low to put the device in standby mode. Pull RESET high then low to reset the jack detection and configuration.

Standby mode leaves the key encoder active to pick up a keypress event if the IC has completed jack detection prior to standby mode. A weak pullup voltage is put across the microphone to look for a hook switch press. Once a keypress event occurs, an interrupt flags, and the IC enters detection mode after $\overline{SHDN}$ transitions high.

Power Domains

MVDD power domain:

Microphone bias, switches, ESD, and jack detection tests 2 to 9.

V_{DD} power domain:

Charge pump, digital block, ADC, mic amp, and jack detection test 1.

Power-Up/-Down Sequence

The IC needs V_{DD} and MVDD to operate correctly.

Turning off one supply voltage during a mode might prevent proper operation of the IC.

The power-up sequence is:

- Apply V_{DD}
- Apply MVDD
- Set AUTO to 01 (register 0x1E, bit 0)

There are a few different ways to power-up/-down depending on how autonomous you want the IC to operate and whether the jack is plugged in or not. The AUTO bits are in register 0x1E, bits 0 and 1. The three methods for getting the IC running are:

- AUTO = 0x00: The IC detects a jack plug-in and set JKIN, but does not run the configuration detect until $\overline{SHDN}$ is pulled high. After the configuration is detected, the IC waits for the system to turn on the appropriate enable bits.
- AUTO = 0x01: The IC detects a jack plug-in and set JKIN, but does not run the configuration detect until $\overline{SHDN}$ is pulled high. After the configuration detect is run, the IC automatically sets the appropriate enable bits to be able to drive all loads for the found cable.
- AUTO = 0x02: The IC detects a jack plug-in, sets JKIN, and automatically runs the configuration detect. After the configuration detect is run, the IC automatically sets the appropriate enable bits to be able to drive all loads for the found cable. However, the amplifiers do not actually turn on until $\overline{SHDN}$ is pulled high. The IC completes detection and waits in standby mode until $\overline{SHDN}$ is pulled high.

Ensure that RESET = 0 to enable the jack detect plug-in test signal.

Power-Up, AUTO = 0x00 or 0x01:

1) Set IDDONE and IJACKSW and IJKIN so that an interrupt flags when something is plugged in and the detection is done.
2) Wait for $\overline{IRQ}$.
3) Wait for JACKSW to set.
4) Pull $\overline{SHDN}$ high.
5) Detection is done when DDONE sets.

If AUTO = 0x00:

1) Read the Status registers to find out what was detected.
2) System makes a decision about what to enable.
3) System sets the appropriate enable bits.
4) Set the volume register to the appropriate setting if audio is present.

If AUTO = 0x01:

1) Read the Status registers to find out what was detected.
2) The appropriate enable bits automatically set.
3) Read the Enable1 and Enable2 registers to see what was turned on.
4) Set the volume register to the appropriate setting if audio is present.

Power-Up, AUTO = 0x02:

1) Wait for JKIN to set.
2) Detection runs automatically, so wait for DDONE to set.
3) Read the Status registers to find out what was detected.
4) The IC is automatically placed in standby mode after detection is done.
5) Pull $\overline{SHDN}$ high to turn on the IC.
6) The appropriate enable bits were automatically set because AUTO = 0x02.
7) Read the Enable1 and Enable2 registers to see what was turned on.

When AUTO = 0x01 or 0x02, the IC automatically enables the required blocks according to what has been detected. In case AUTO = 0x00, it is required that all the correct blocks are enabled for unplug detection to work properly. Table 18 correlates the status bits with the enable bits for the blocks that are (need to be) enabled for proper operation.

Power-Down, All AUTO Settings:

If audio is playing and VSEN = 0:

1) Set the headphone volume register mute bits or set code 0x00 as the volume.
2) The VOL bit is set when the volume slew is done. Make sure IVOL is set so that an interrupt is flagged.
3) Pull $\overline{SHDN}$ low to go into standby mode; the current jack case is remembered. Cycle RESET (low → high → low) to run jack detection and configuration again.

If audio is not playing:

1) Set $\overline{VSEN}$ = 1 to disable volume slewing. If this is not done, the volume slew down at a rate of 1ms per volume step.
2) Set the headphone volume register mute bits or set code 0x00 as the volume, and the amplifiers mute immediately.
3) Pull $\overline{SHDN}$ to 0 to go to standby mode; the current jack case is remembered. Cycle RESET (low → high → low) to run jack detection and configuration again.

Table 18. Status Bits Relation to Enable Bits

STATUS BIT	ENABLE BIT
MIC_IN	MIC_BIAS MIC_AMP KS
LINE_L	LFTEN
LINE_R	RGHEN
HP_L	LFTEN
HP_R	RGHEN

PCB Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance, as well as route heat away from the device. Good grounding improves audio performance, minimizes crosstalk between channels, and prevents switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PCB. Route PGND and all traces that carry switching transients away from GND, and the traces and components in the audio signal path.

Place the charge-pump capacitors as close as possible to the device. Bypass PVDD and PVSS with a 1µF capacitor to PGND. Place the bypass capacitors as close as possible to the device.

Route the pins that connect to the jack on wide, low-impedance traces whenever possible. RING2 or SLEEVE ends up being the load's ground connection; ground impedance causes excess crosstalk and noise pickup.

Route the EXTCLK traces away from low-level audio input nodes and the microphone bias bypass connection to keep the audio as noise free as possible.

PGND and GND pins need to have as low an impedance connection to the ground plane. This means liberal use of vias and a solid ground plane.

The maximum resistance between the pins TIP and RING1 to the headphone jack should not exceed 3Ω.

The maximum resistance between RING2 and SLEEVE to the headphone jack should be 0.5Ω or better. RING2 or SLEEVE is used as the common connector in a headset or headphone. Any impedance on this path decreases crosstalk performance.

Power-Supply Bypassing

A bulk 10µF capacitor is required for proper charge-pump operation. The capacitors are readily available in 0603 packages in the necessary voltage rating. Bypass V_{DD} to PGND with 10µF.

Audio Amplifier with Jack Detection

Component Selection and Layout

Charge-Pump Capacitors

The charge pump requires three capacitors: PVDD, PVSS, and the flying capacitor between C1N and C1P. It is recommended that these all remain the same value. Capacitance values of 1µF are recommended. Larger value capacitors can be used to lower power-supply ripple. Do not use charge-pump caps greater than 3.3µF. See Table 19 for a detailed description for each component value.

Table 19. Recommended Component Values

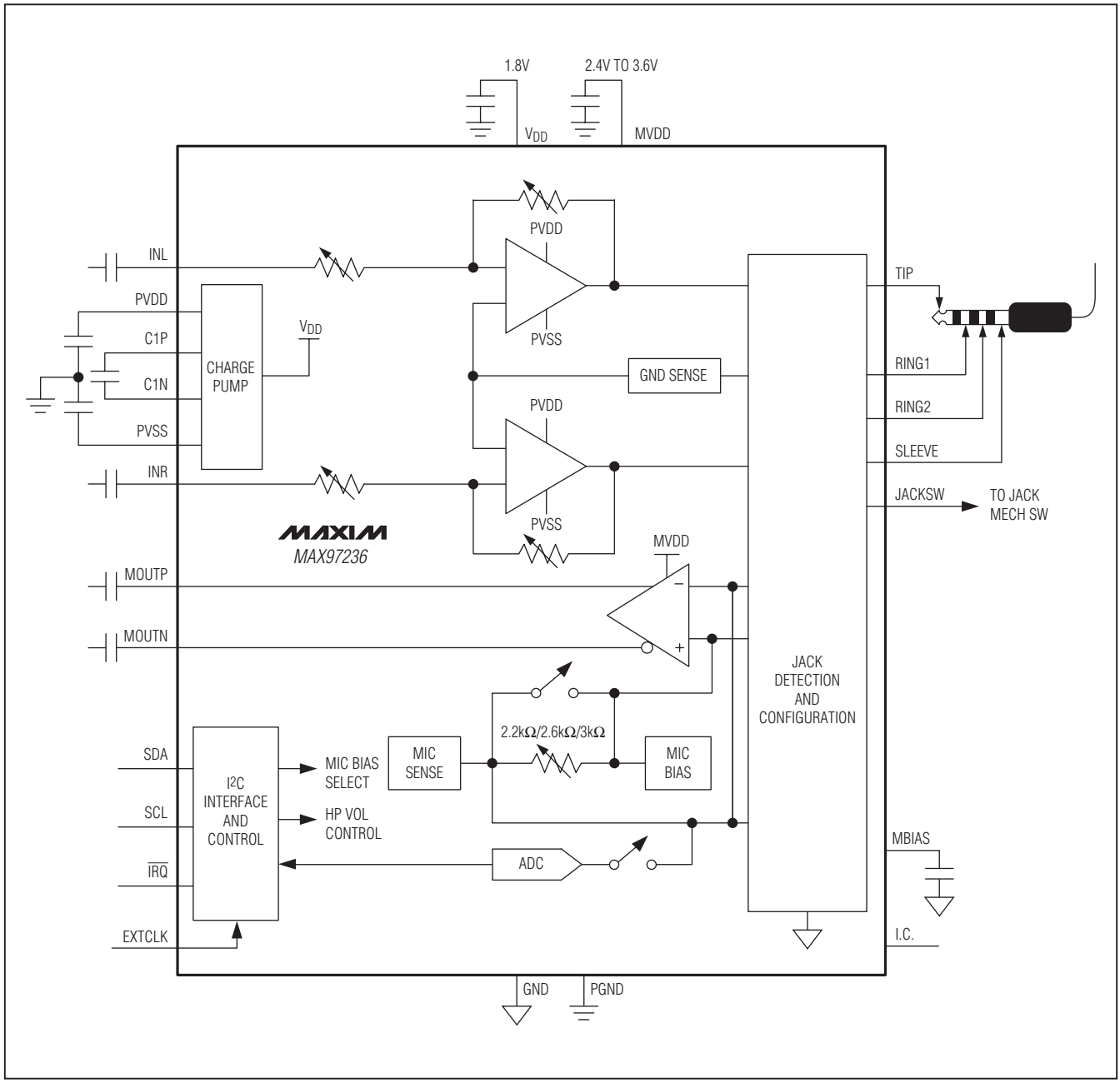
COMPONENT	RECOMMENDED VALUE	DETAILS
Charge-pump capacitors	1µF, X5R, 6.3V or greater voltage rating or better	The capacitor needs low ESR to achieve the required charge-pump output impedance. If the charge-pump output impedance is too high, the headphone amplifier cannot deliver the stated output power. A larger capacitor does not completely charge in one switching cycle. A smaller capacitor does not hold enough charge. Thus, it is highly recommended to use the suggested value.
V_{DD} capacitor	C1: 1µF to 10µF, X5R, 6.3V or better C2: 0.01nF to 0.1µF, X5R, 6.3V minimum	C1: A smaller values helps on the ESD robustness. C2: Is not a must-have capacitor, but still recommended. This capacitor helps improve the RF immunity of the IC.
Audio input capacitors	1µF, 6.3V, X5R or better	Lower capacitance creates a highpass filter due to the input impedance of the IC.
Microphone input capacitors	1µF, 6.3V, X5R or better	—
EMI filter capacitors	33pF	—
EMI filter ferrite bead	Murata BLM15BB220	—

Chip Information

PROCESS: BiCMOS

Audio Amplifier with Jack Detection

Functional Diagram/Typical Application Circuit

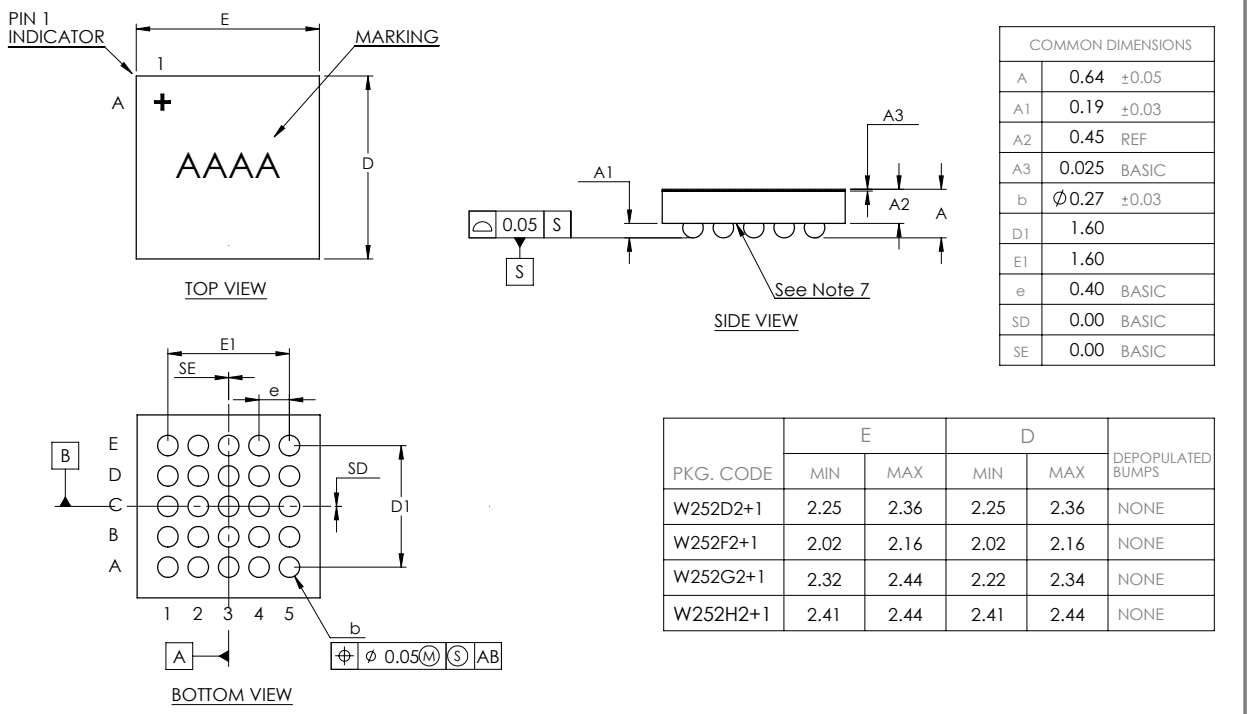


Audio Amplifier with Jack Detection

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25-Bump WLP	W252G2+1	21-0453	Refer to Application Note 1891



COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.19	±0.03
A2	0.45	REF
A3	0.025	BASIC
b	Ø0.27	±0.03
D1	1.60	
E1	1.60	
e	0.40	BASIC
SD	0.00	BASIC
SE	0.00	BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W252D2+1	2.25	2.36	2.25	2.36	NONE
W252F2+1	2.02	2.16	2.02	2.16	NONE
W252G2+1	2.32	2.44	2.22	2.34	NONE
W252H2+1	2.41	2.44	2.41	2.44	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

MAXIM

TITLE: PACKAGE OUTLINE
25 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0453 | REV. D | 1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—