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ATTENTION

SIEMENS

ICs for Communications

4 Channel ISDN Echocancellation Digital Front End
Quad IEC DFE-T

PEB 24901

Version 1.1

Preliminary Data Sheet 2.95 T2490-111-P1-7600

PEB 24901 Revision History: 2.95	
Previous Releases:	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.
For detailed technical information about “Processing Guidelines” and “Quality Assurance” for ICs, see our “Product Overview”.

Edition 2.95
This edition was realized using the software system FrameMaker®.

Published by Siemens AG, Bereich Halbleiter
P. O. Box 80 17 09, D-81617 München

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4 Channel ISDN Echocancellation Digital Front End (Quad IEC DFE-T) PEB 24901

Preliminary Data Sheet **CMOS IC**

1 Introduction

The PEB 24901 4 Channel ISDN Echocancellation Digital Front End (Quad IEC DFE-T) is the digital part of an optimized ISDN 4B3T-U-Interface Line card chip set. It features 4 independent digital signal processors providing, in conjunction with the PEB 24902 ISDN Quad Analog Front End (Quad IEC AFE) , full duplex data transmission at the U_{k0} reference point according to FTZ Guideline 1TR 220, ETSI ETR80 and CCITT I.430 standards.

The PEB 24901/24902 chip set is based on the PEB 20901/20902 IEC-T ISDN U-transceiver chip set.

1.1 Basic system Functions

- Full duplex transmission and reception of the U_{k0} interface signals according to the FTZ Guideline 1 TR 220 of the Deutsche Bundespost Telekom (DBPT).
  - 144 kbit/s user bit rate over standard local telephone loops
  - 1 kbit/s maintenance channel for transmission of data loop back commands and detected transmission errors
  - 4B3T ternary block code (subscriber line symbol rate 120 kbaud)
  - Monitoring of transmission errors
  - Subscriber loop length without repeater:

    up to 4.2 km on 0.4 mm wire

    up to 8.0 km on 0.6 mm wire
- Adaptive echo cancellation.
- Adaptive equalization.
- Automatic polarity adaption.
- Clock recovery (frame and bit synchronization).
- Transposition of ternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaption).
- Built in wake-up unit for activation from power-down state.
- Activation and deactivation procedure according to CCITT I.430 and to FTZ Guideline 1 TR 210 of the DBPT.
- Optimized for working in conjunction with telecom ICs as the IDEC® (PEB 2075), EPIC® (PEB 2055) and ELIC® (PEB 20550) via IOM-2 interface.

- Data speed conversion between the U_{k0} frames and the IOM-2 frames. Absorption of received phase-wander of up to 18 µs peak to peak (CCITT Rec. Q.512).
- Handling of commands and indications contained in the IOM-2 C/I-channel for activation, deactivation, supervision of power supply unit and equipment for wire testing.
- IOM-2 system interface
- Data availability via the MONITOR channel:
- accumulated RDS transmission errors for the whole U_{k0} link
- Echo canceller coefficients and status values, which can be used to indicate the state of the U_{k0} interface
- Switching of an analog test loop at the U_{k0} interface for testing (loop 1 in LT).
- Remote control of test loop switching via maintenance channel.
- 4 relay driver pins per port addressable by Monitor command
- 2 status pins per port reporting to the Monitor channel
- JTAG boundary scan path
- The PEB 24901 comes in a M-QFP 64 package.

1.2 Pinning and Outline

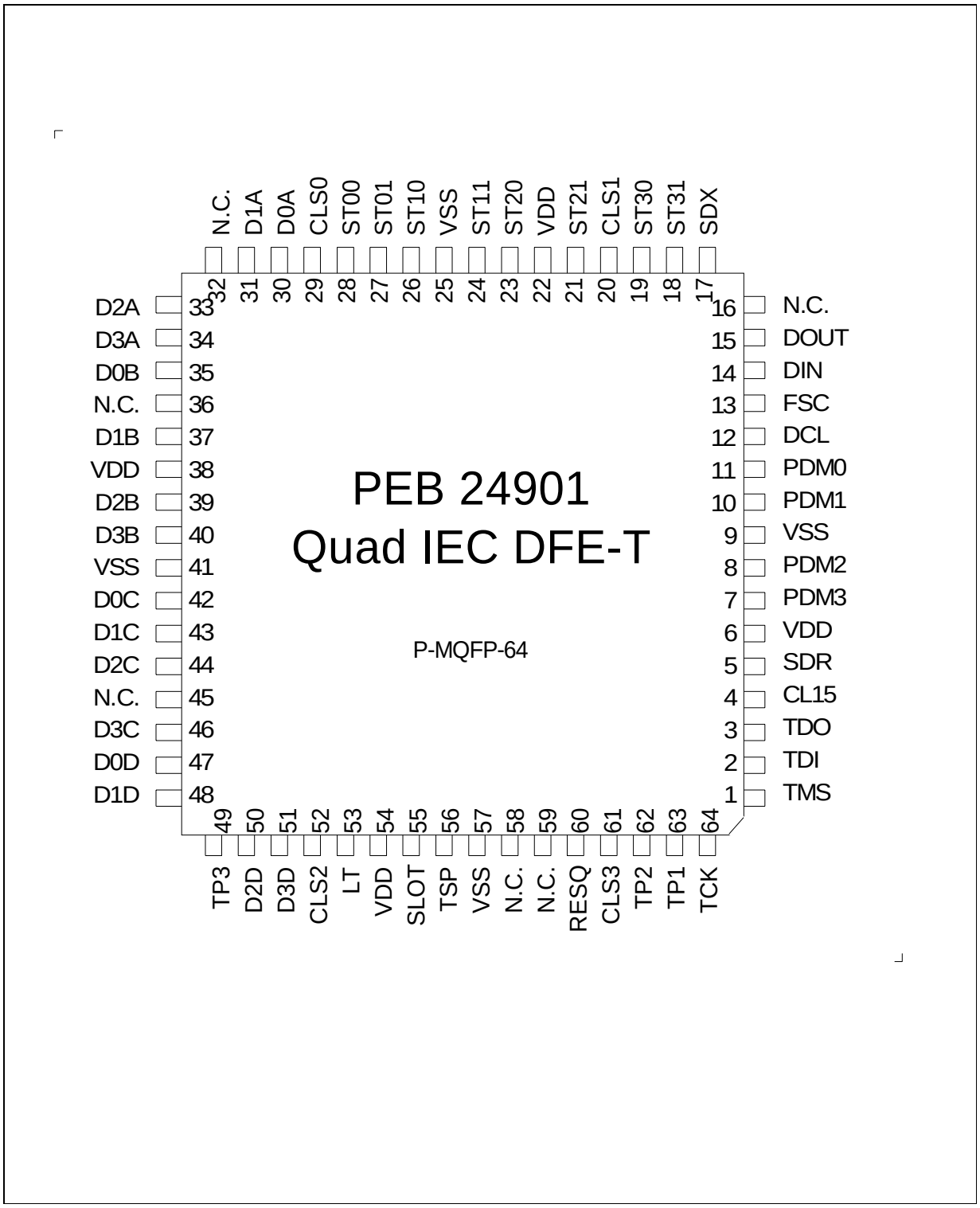


Figure 1: Pin configuration and Outline (t.b.d), top view

1.3 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

Table 1
Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Description	Reference
Power Supply Pins				
6, 22, 38, 54	VDD		5V +/-5% supply voltage	
9, 25, 41, 57	GND		0V	
JTAG Boundary Scan				
64	TCK	I	Test Clock	3.2.3
1	TMS	I	Test Mode Select	3.2.3
2	TDI	I	Test Data Input	3.2.3
3	TDO	O	Test Data Output	3.2.3
IOM-2 Interface				
14	DIN	I	Data in. Input of IOM-2 data synchronous to DCL clock	3.2.1
15	DOUT	O	Data out. Output of IOM-2 data synchronous to DCL clock.	3.2.1
13	FSC	I	Frame synchronisation clock. The start of the B1 channel in time slot 0 is marked.	3.2.1
12	DCL	I	Data clock. Clock range 512 to 4096 kHz. Note that 4 channels only can be driven with DCL >= 2048 kHz.	3.2.1

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference
Miscellaneous Function Pins				
29	CLS0	O	120 KHz transmit clock of channel 0	
20	CLS1	O	120 KHz transmit clock of channel 1	
52	CLS2	O	120 KHz transmit clock of channel 2	
61	CLS3	O	120 KHz transmit clock of channel 3	
30	D0A	O	Driver pin of line port 0, can be set with Monitor command, bit A. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
35	D0B	O	Driver pin of line port 0, can be set with Monitor command, bit B. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
42	D0C	O	Driver pin of line port 0, can be set with Monitor command, bit C. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
47	D0D	O	Driver pin of line port 0, can be set with Monitor command, bit D. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
31	D1A	O	Driver pin of line port 1, can be set with Monitor command, bit A. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
37	D1B	O	Driver pin of line port 1, can be set with Monitor command, bit B. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference
43	D1C	O	Driver pin of line port 1, can be set with Monitor command, bit C. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
48	D1D	O	Driver pin of line port 1, can be set with Monitor command, bit D. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
33	D2A	O	Driver pin of line port 2, can be set with Monitor command, bit A. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
39	D2B	O	Driver pin of line port 2, can be set with Monitor command, bit B. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
44	D2C	O	Driver pin of line port 2, can be set with Monitor command, bit C. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
50	D2D	O	Driver pin of line port 2, can be set with Monitor command, bit D. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
34	D3A	O	Driver pin of line port 3, can be set with Monitor command, bit A. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
40	D3B	O	Driver pin of line port 3, can be set with Monitor command, bit B. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference
46	D3C	O	Driver pin of line port 3, can be set with Monitor command, bit C. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
51	D3D	O	Driver pin of line port 3, can be set with Monitor command, bit D. Default after Pin-reset is low. C/I-code reset does not affect the state	3.2.1.2.3
53	LT	I	Mode pin reserved for further use. Connect to VDD	
60	RESQ	I	Reset of all four line ports, asynchronous signal, low active	
55	SLOT	I	IOM-2 slot selection. SLOT = 0 assigns slots 0 to 3 to ports 0 to 3; SLOT = 1 assigns slots 4 to 7to ports 0 to 3	3.2.1
28	ST00	I	Status pin 0 of line port 0, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
27	ST01	I	Status pin 1 of line port 0, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
26	ST10	I	Status pin 0 of line port 1, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
24	ST11	I	Status pin 1 of line port 1, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
23	ST20	I	Status pin 0 of line port 2, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference
21	ST21	I	Status pin 1 of line port 2, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
19	ST30	I	Status pin 0 of line port 3, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
18	ST31	I	Status pin 1 of line port 3, status is passed to IOM-2 via Monitor message. Connect to either VDD or GND, if not used.	3.2.1.2.4
63	TP1	I	Test pin 1. Not available to user. Connect to GND.	3.2.1.2.4
62	TP2	I	Test pin 2. Not available to user. Connect to GND.	
49	TP3	I	Test pin 3. Not available to user. Connect to GND.	
56	TSP	I	Single pulse test mode. For activation refer to table "T.B.D". When active, "+1" pulses are issued in 1 ms intervals. Connect to GND when not used.	
Interface to Analog Front End				
4	CL15	I	Master Clock 15.36 MHz. All operations and the data exchange on the digital interface are based on this clock.	3.2.2
11	PDM0	I	Input of second-order sigma-delta ADC pulse density modulated bit stream from the PEB 24902 Quad AFE, line port 0	3.2.2

Table 1
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description	Reference
10	PDM1	I	Input of second-order sigma-delta ADC pulse density modulated bit stream from the PEB 24902 Quad AFE, line port 1	3.2.2
8	PDM2	I	Input of second-order sigma-delta ADC pulse density modulated bit stream from the PEB 24902 Quad AFE, line port 2	3.2.2
7	PDM3	I	Input of second-order sigma-delta ADC pulse density modulated bit stream from the PEB 24902 Quad AFE, line port 3	3.2.2
5	SDR	I	Interface to the PEB24902 Quad AFE containing level information for the detection of the awake tone. The four lines are multiplexed on SDR.	3.2.2
17	SDX	O	Interface to the PEB24902 Quad AFE for the transmit and control data. Transmission is based on clock CL15 (15,36 Mbit/sec). For each line port the following bits are exchanged: TD0, TD1: Transmit data RANGE: Range select LOOP: Analogue loop back switch PDOW: Power down/power up Synchronisation information	3.2.2

2 System Integration

The PEB 24901 Quad IEC DFE-T is optimized to work in conjunction with the PEB 24902 Quad IEC AFE on line modules in the central office or in the LT function of the access network . It supports the 4B3T line code. A PLL internal to the PEB 24902 Quad IEC AFE synchronises the 15.36 MHz master clock onto a PTT reference clock of either 8 kHz, 512 kHz or 2048 kHz. The Quad IEC DFE-T receives this clock from the Quad IEC AFE.

The Quad IEC DFE-T is connected to four time slots of the IOM-2 interface. The selection is done with the SLOT pin. The SLOT pin assigns either the IOM-slots 0 to 3 to the four channels 0 to 3 (SLOT pin low), or it assigns the IOM-slots 4 to 7 to the channels 0 to 3 (SLOT pin high).

Figure 2 illustrates the application in a 4 channel line card together with one PEB 24902 Quad IEC AFE.

Figure 3 shows an 8 channel application. One PLL generates the synchronised clock for all 4 devices. Note that the second PEB 24902 Quad IEC AFE receives the 15.36 MHz clock in this application. It's PLL is deactivated.

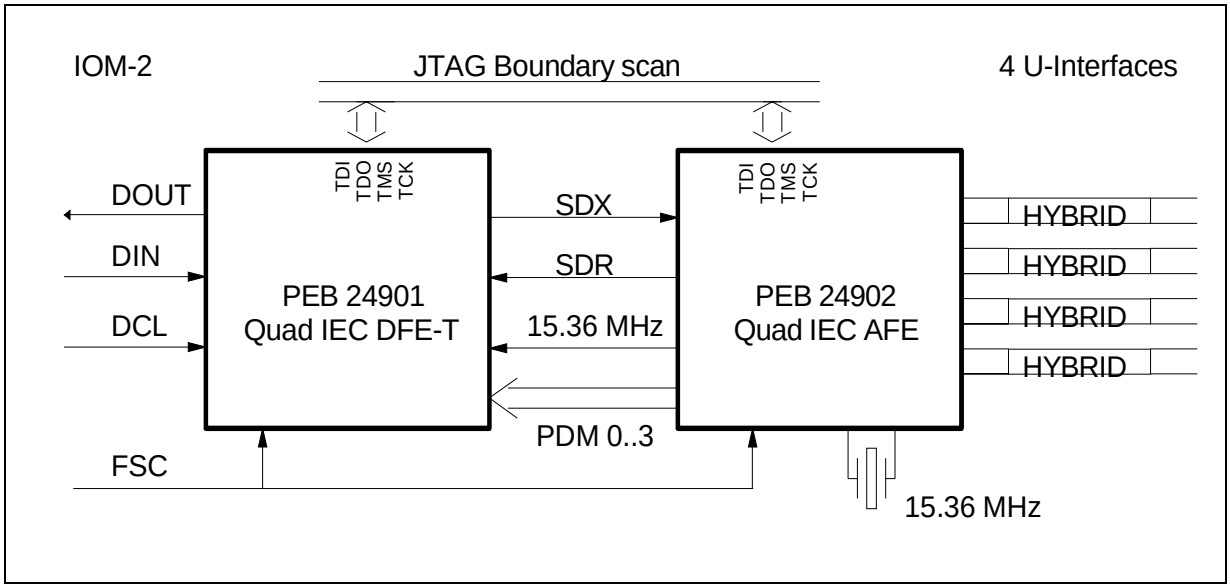


Figure 2: 4 channel LT application

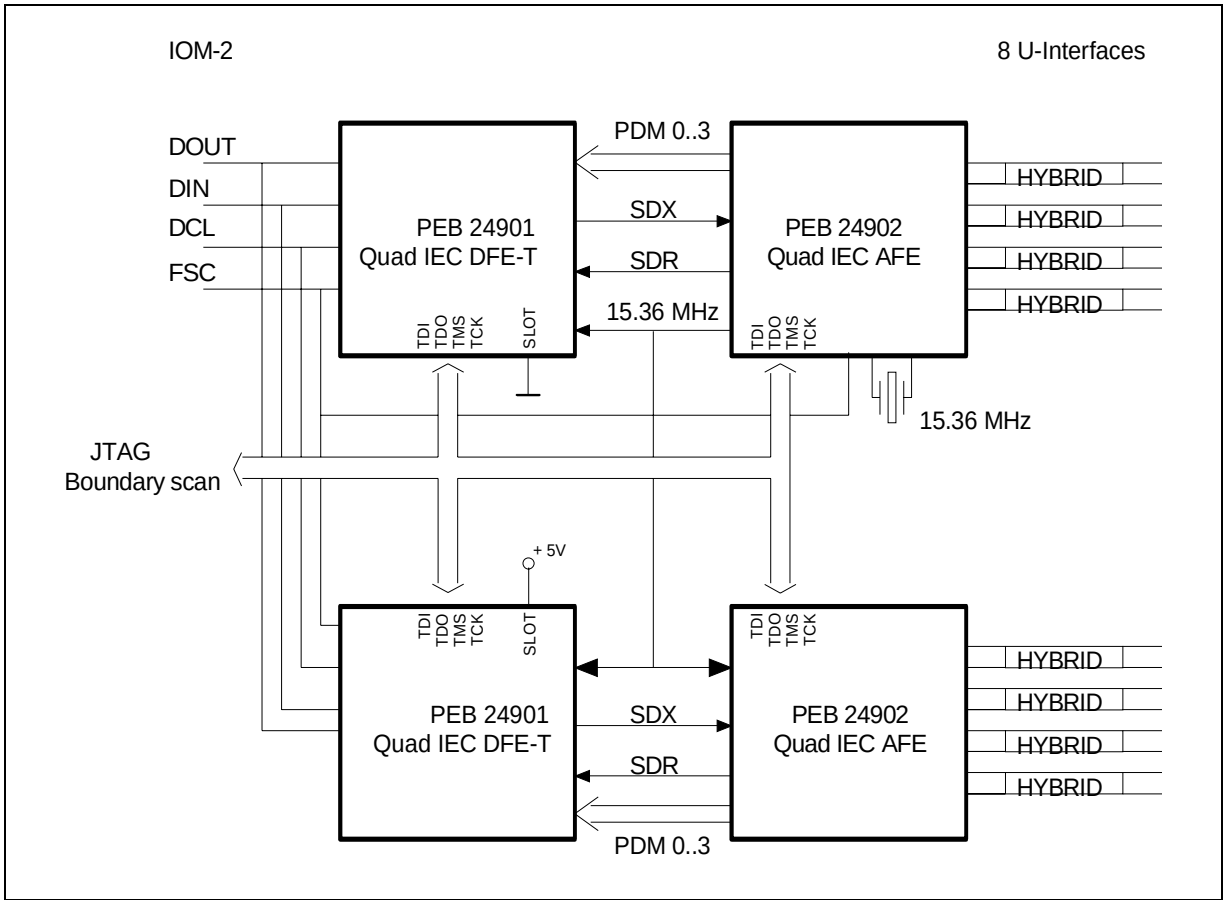


Figure 3: 8 channel LT application

3 Application Guide

3.1 Clock Generation

In the exchange (LT mode) , all timing signals are derived from a system clock via the PLL internal to the PEB 24902 Quad IEC AFE.

The master clock is generated with a crystal oscillator connected to the Quad IEC AFE. It is synchronised to the system clock (8 kHz, 512 kHz or 2048 kHz) with the PLL of the Quad IEC AFE.

Master clock nominal frequency:	15.36 MHz
Max. Difference of phase deviations of Master clock and FSC:	± 18 µs
Max. low freq. phase wander within 1 period:	± 0.85 ps
Jitter (peak-to-peak):	see **figure 4**

The jitter on the 15.36 MHz master clock is passed to the U-interface without change. Hence, fig. 4 reflects the jitter as given in FTZ 1 TR 220.

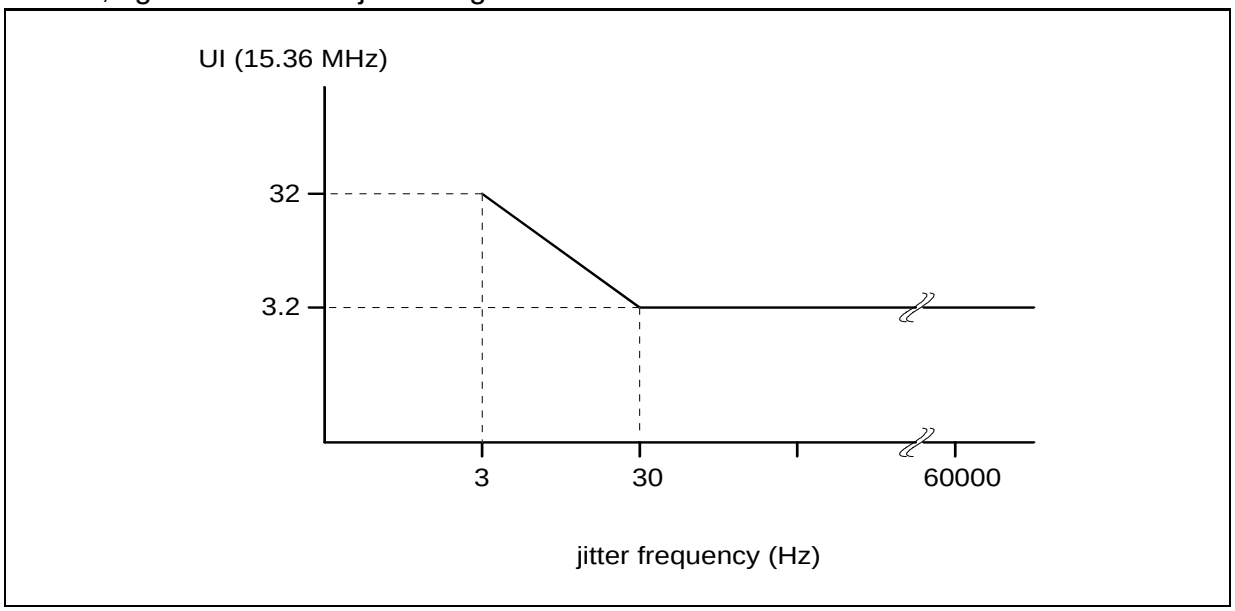


Figure 4: Maximum Clock Jitter

3.2 Interfaces

3.2.1 IOM-2 System Interface

The PEB 24901 Quad IEC DFE-T is equipped with a second generation digital ISDN Oriented Modular (IOM-2) interface, for communication with upper layer functions, such as IDEC® (PEB 2075), EPIC® (PEB 2055) and ELIC® (PEB 20550). EPIC and ELIC represent the first switching stage towards the exchange system.

The IOM-2 interface is a four-wire serial interface with a data clock (DCL), an 8 kHz frame synchronization clock (FSC), and one data line per direction: data downstream (DD) and data upstream (DU).

The basic channel consists of a total of 32 bits, or four octets: 18 bits for B1 + B2 + D plus 14 overhead bits for monitor and control information (activation/deactivation of OSI layer 1 and maintenance functions).

The ISDN user data rate is 144 kbit/s (B1 + B2 + D). Within one FSC period, 32 bit up to 256 bit are transmitted, corresponding to DCL frequencies ranging from 512 kHz up to 4096 kHz. The data is transmitted transparently synchronous and in phase in both directions over the IOM-2 interface using time division multiplexing within the 125 µs IOM-2 interface frame. As the IEC Quad DFT-T occupies four IOM-slots, the following data rates apply:

Nominal bit rate of data (DD and DU):	1024 kbit/s … 2048 kbit/s
Nominal frequency of DCL:	2048 kHz … 4096 kHz
Nominal frequency of FSC:	8 kHz

Figure 5 illustrates the multiplexed frame strucure of the IOM-2 interface.

The data is latched with the odd numbered rising edges of DCL as given in fig. 5 lower part.

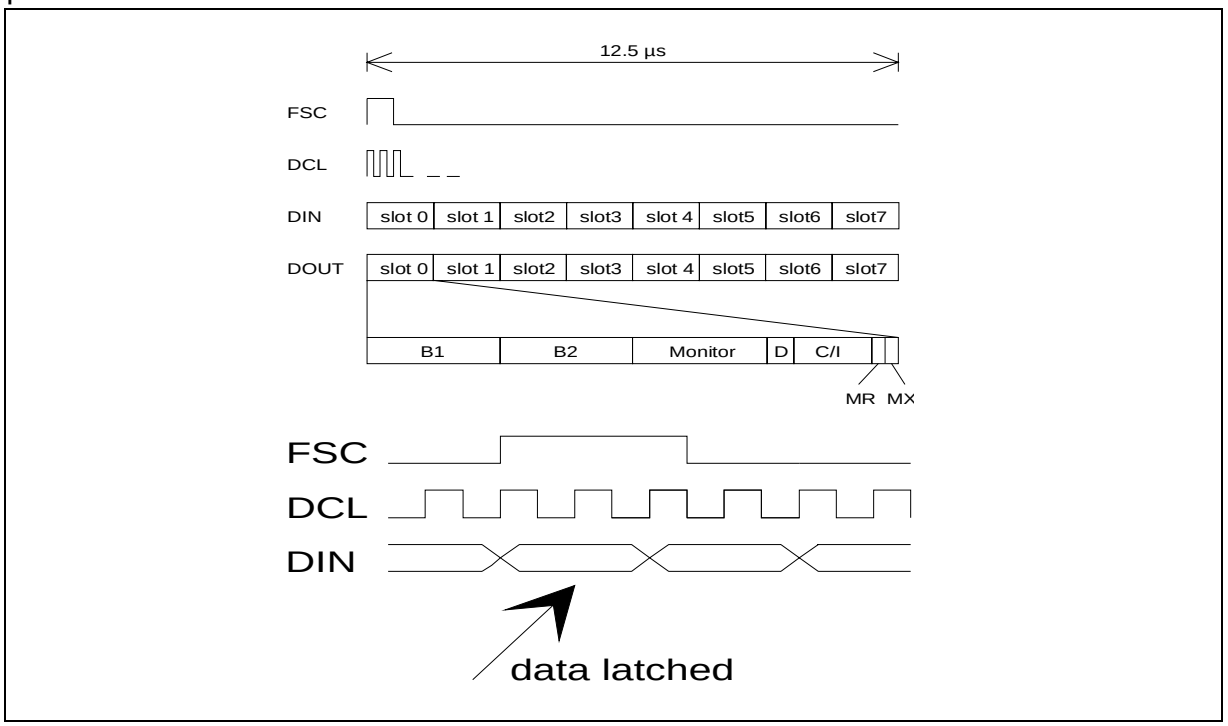


Figure 5: IOM-2 Interface and bit timing

As the PEB 24901 Quad IEC DFE-T occupies four IOM-slots, the DCL frequency should be at least 2048 KHz. The SLOT pin assigns either the IOM-slots 0 to 3 to the four channels 0 to 3 (SLOT pin low), or it assigns the IOM-slots 4 to 7 to the channels 0 to 3 (SLOT pin high).

3.2.1.1 Command/Indicate Channel

The Commandl/Indicate channel (C/I-channel) is used to control the operational status of the Quad IEC DFE-T and to issue corresponding indications. C/I-channel codes serve as the main link between the Quad IEC DFE-T and external intelligence. In **chapter 3.4.4** status diagrams give information on the commands by which the current operational status may be left, and on indications issued in all states.

Commands have to be applied continuously on DIN until the command is validated by the Quad IEC DFE-T and the desired action has been initiated. Afterwards the command may be changed.

An indication is issued permanently by the Quad IEC DFE-T on DOUT until a new indication needs to be forwarded. Because a number of states issue identical indications it is not possible to identify every state individually.

The following example illustrates the use of the C/I-channel in combination with the PEB 2055 (EPIC). It is assumed that the device has been initialized correctly prior to starting the C/I-code transfer.

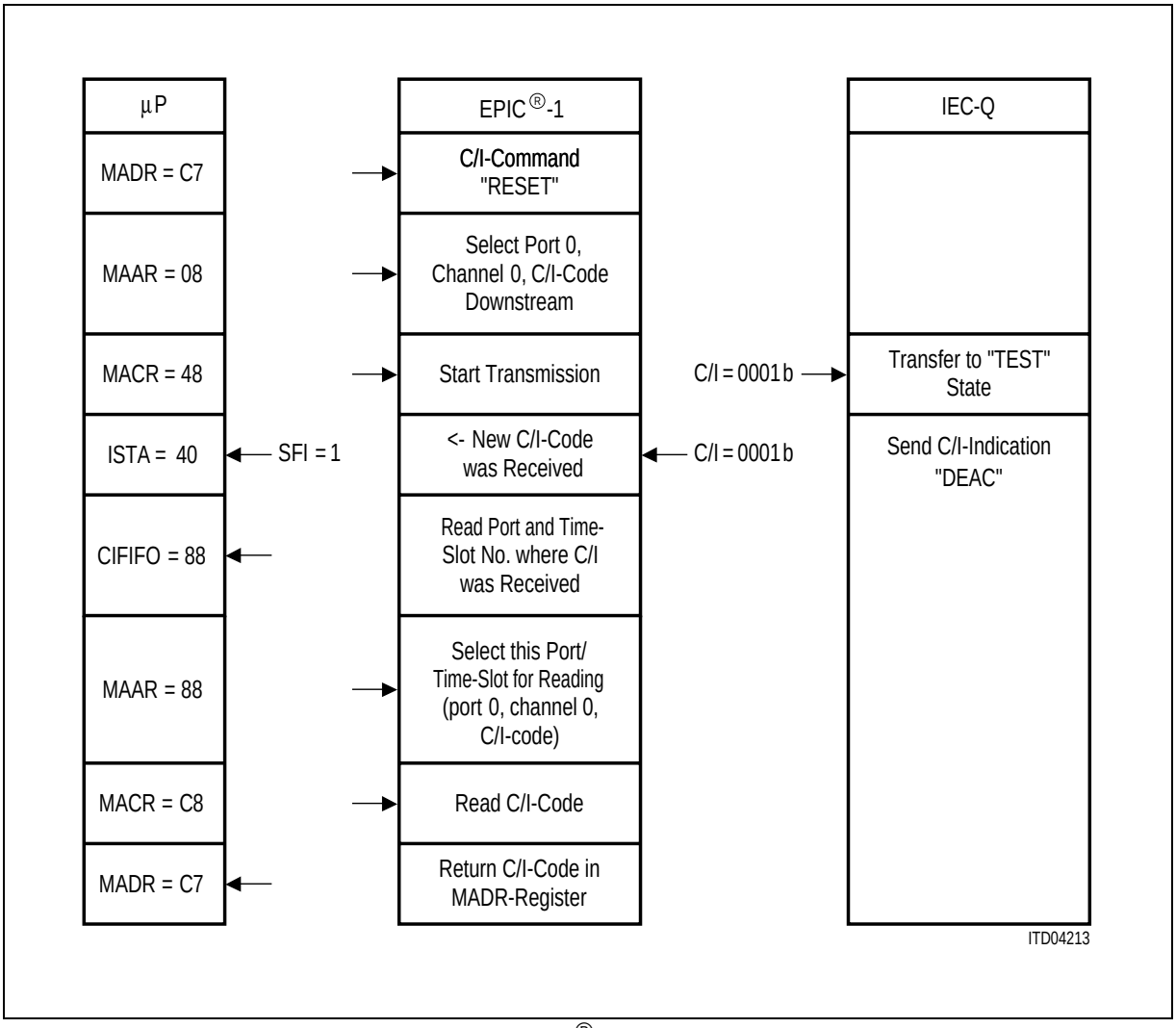


Figure 6: C/I-Channel Use with the EPIC® (all data values hexadecimal)

After the correct initialization of the EPIC, the C/I-code which is to be transmitted to the IEC-T is written into the MADR-register (structure: 1 1 C/I C/I C/I C/I 1 1). With the MAAR-register the EPIC is informed where to send this C/I-code (transmission direction, port number and time-slot number). For a description of this register please refer to the EPIC-manual. The example above sends the C/I-command to port 0, time-slot 0. MACR = 48_H starts the transmission of the command.

If a change in one of the C/I-channels was observed, an ISTA-interrupt (bit SFI) is generated. Because the user does not know in which channel the change occurred, the location needs to be read from the CIFIFO-register. This address is copied via software into address register MAAR. After having started the read operation with MACR = $C8_H$ the C/I-message can be read from MADR (structure as described earlier).

3.2.1.2 Monitor Channel

The monitor channel represents a second method of initiating and reading Quad IEC DFE-T specific information. Features of the monitor channel are supplementary to the command/indicate channel. Unlike the command/indicate channel with an emphasis on status control, the monitor channel provides access to internal bits (maintenance, overhead) and test functions as local loop-backs and block error counter.

The following chapters describe the principle of monitor handshake in IOM-2, internal safe guards against blocking of the monitor channel, and features.

3.2.1.2.1 Handshake Procedure

IOM-2 provides a sophisticated handshake procedure for the transfer of monitor messages. For handshake control two bits are assigned to each IOM-frame (on DIN and DOUT).

The monitor transmit bit (MX) indicates when a new byte has been issued in the monitor channel (active low). The transmitter postpones transmitting the next information until the correct reception has been confirmed. A correct reception will be confirmed by setting the monitor read bit (MR) to low.

In order to send a monitor message from the control unit to the Quad IEC DFE-T, the MX-bit on DIN and the MR-bit on DOUT are used. In the opposite direction the Quad IEC DFE-T handles the MX-bit of the DOUT-pin and watches the MR-bit of the DIN-signal.

Figure 7 demonstrates monitor channel handling with the PEB 2055 (EPIC-1). A two-byte message is sent from the control unit to the Quad IEC DFE-T which acknowledges the receipt by returning a two-byte long message in the monitor channel.

The EPIC-1/2 supports different types of monitor transfer. For communication with the Quad IEC DFE-T, three are of special interest.

Transmit Only. This mode is required when the EPIC sends monitor messages but no confirmation is returned by the Quad IEC DFE-T.

Transmit and Receive. The EPIC transmits first and receives afterwards. Confirmations sent by the Quad IEC DFE-T can be read.

Searching for Active Monitor Channels. Listens to the IOM-monitor channel and reads information issued by the Quad IEC DFE-T autonomously. Nothing is transmitted by the EPIC.

The EPIC uses a FIFO for transmission and reception. The user therefore does not have to provide routines for the handshake protocol.

PEB 2055 and Monitor Channel Programming:

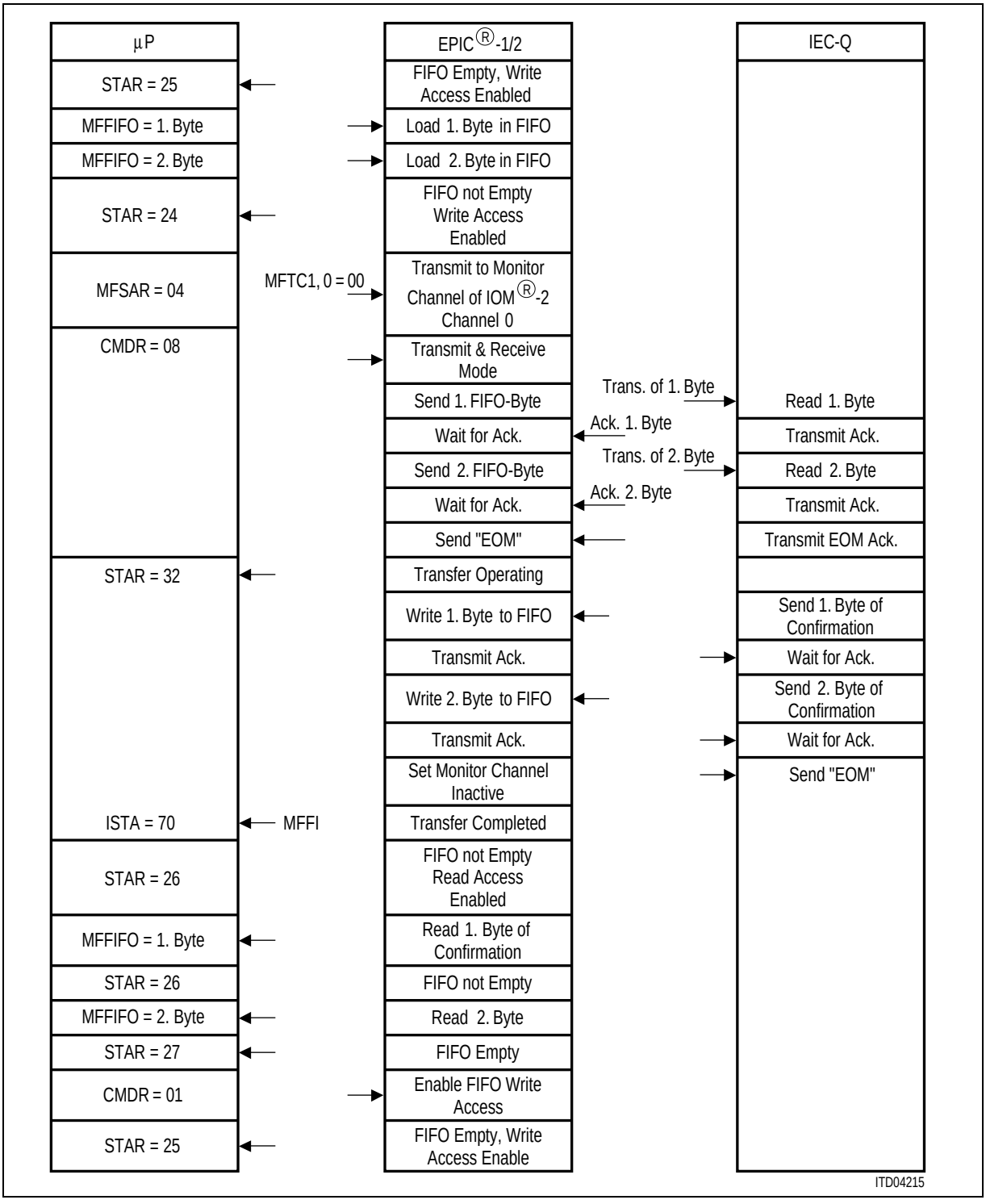


Figure 7:
Monitor Channel Handling with EPIC®-1/2 (all data values hexadecimal)

The example of **figure 7** demonstrates the use of EPIC-1 or EPIC-2 in the transmit-and-receive mode. It is assumed that the transferred monitor message will be followed by a two byte confirmation issued by the Quad IEC DFE-T.

Before programming the FIFO, it is verified that the FIFO is empty and write access is possible. All monitor data is loaded into the FIFO (two bytes), the transmission channel and mode are selected. Writing “CMDR = 08” starts transmission of the FIFO contents and enables monitor data reception. After both bytes have been transmitted, the confirmation from the Quad IEC DFE-T is read into the FIFO. After completion of the transfer an interrupt is generated. If the operation was successful, “STAR = 26” will indicate that data is loaded and the read access is enabled (in addition it is indicated that the PCM-synchronization status is correct). Following the readout of the confirmation bytes, the FIFO is cleared and the write access is selected again with the CMDR-register (“CMDR = 01”).

The handshake timing for byte transfer is handled automatically by EPIC and Quad IEC DFE-T.

3.2.1.2.2 Readout of specific Information

Chip identification, Echocanceller Coefficients and RDS counter can be read-out with two-byte MONITOR commands as given in table 2. Each command is executed after having been transferred by the proper handshake procedure.

The answers given by the Quad IEC DFE-T are summarized in table 3. The messages

Table 2
Coding of MONITOR Commands (Hexadecimal)

Identification	80 00	Quad IEC DFE-T responds with 80 07_H, distinguishing it from other layer 1 devices
RDS	80 EF	read and reset RDS counter
Coefficients	80 04 ... 80 62	read coefficients of echo canceller

"Answer Identification" and "RDS-counter" are two-byte messages. The coefficient values are given in a four-byte message. The IEC contains an adaptive FIR filter with 48

Table 3
Coding of MONITOR Messages (Hexadecimal)

Identification	80 07	Quad IEC DFE-T responds with 80 07_H,
RDS	80 " data byte"	RDS counter value "data byte"
Coefficients	88 04 .. 88 62 (even) 8C 05 ... 8C 63 (odd)	1. byte of coefficients of echo canceller 2. byte of coefficients of echo canceller

coefficients. This filter emulates the line characteristics in order to cancel the echoed data from the received signal and to regain the data from the far end. Because these coefficients characterize the line, being a time discrete pulse response, it is of great interest to read them out of the IEC and evaluate them to localize possible faults in the two wire loop.

The 16 most significant bits of the echocanceller coefficients can be read out via the MONITOR-channel. To reduce internal circuitry, these coefficients have a rather complicated format.

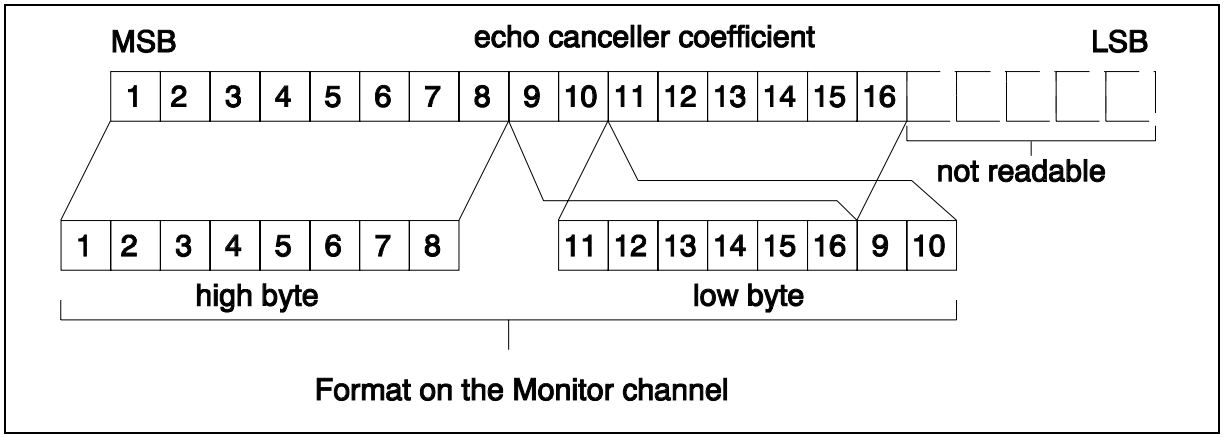


Figure 8
Transposition of EC Coefficient to MONITOR-Channel

The low byte of a coefficient is to be accessed with an even numbered address in the MONITOR-channel, the high byte with an odd numbered address. The coefficient to cancel the first echo is therefore accessible under addresses 04_H and 05_H; the last coefficient is found in addresses 62_H and 63_H. Both bytes are requested via the Monitor command addressing the high byte of one coefficient. For instance if the second coefficient is requested with the Monitor command "80 06", the Quad IEC DFE-T will answer with a four byte message giving the high byte (adress 06) and the the low byte (adress 07): 88 06 "data byte" 8C 07 "data byte".

To avoid a carry from low to high, caused by continuous adaption between the readouts of the low and the high byte, the coefficients are stored after a monitor command "Coefficients" and read out while the echocanceller allready may compute new coefficients.

3.2.1.2.3 Setting the Driver Pins

Each channels owns four data pins Dij, where i = 0, 1, 2, 3 denotes the channel and j = A, B, C, D specifies the pin. They are set with a two-byte Monitor command 81 $7x_H$, where x is the hexadecimal notation of the binary value of the pins: x_H = D C B A_{bin}.

The setting of the driver pins is not affected by a C/I reset.

Table 4
MONITOR Command to set the Driver pins (Hexadecimal Addresses)

Hexadecimal	Binary	Command
81 7x	1000 0001 0111 D C B A	set Pins DiA, DiB, DiC, DiD

3.2.1.2.4 Reading the Status Pins

Each channel owns two status pins ST_{ij}, where i = 0,1, 2, 3 denotes the channel and j = 0, 1 specifies the pin. Their logical values are reported to the Monitor channel. Any change at one of the two pins causes a two-byte Monitor message to be issued automatically giving the state of both status pins. Additionally, the Quad IEC DFE-T will issue the state of the two pins upon request . The request is given by a two-byte Monitor command .

The ST_{ij} pins have to be tied to either VDD or GND, if not used.

Table 5
MONITOR Commands to read Status pins

Hexadecimal	Binary	Command
81 00	1000 0001 0000 0000	Request Status
88 0x	1000 1000 0000 00 ST_1 ST_0	Report Status of ST_{i1} ST_{i0}

3.2.2 Interface to the Analog Front End

The interface to the PEB 24902 Quad IEC AFE is a serial interface at the pins SDX and SDR. On SDX and SDR transmit and receive data is exchanged as well as control information for the start-up procedure. The ADC output from the Quad IEC AFE is transferred to the Quad IEC DFE-T on the signals PDM0..PDM3. The timing of all signals is based on the 15.36 MHz clock which is provided by the Quad IEC AFE.

The transmit data, powerup/down, range function and analog loopback are transferred on SDX, and the level status on SDR for all line ports. Eight time slots contain the data for up to eight line ports. The Quad IEC DFE-T uses four of them. The allocation of these time slots is done by the nineth time slot, a 24 bit synch. word on SDX, that consists of all ZEROs. The other time slots with transmission data start with a ONE. Therefore the first ONE after 24 subsequent ZEROs is the first bit of time slot no. 0. This information is also used to determine the status of synchronisation of the digital interface after reset.

The transmit pulses have to be disclosed to the Quad IEC AFE with a period of 120 kHz. This defines the period of the SDX-frame. The 128 available bits during a 120 kHz period (related to the 15.36 MHz clock) are divided into the 9 slots of which 8 slots are

13 bits long used for data transmission. The status on SDR is synchronised to SDX. Each time slot on SDR carries the corresponding LD bit during the last 12 bits of the slot.

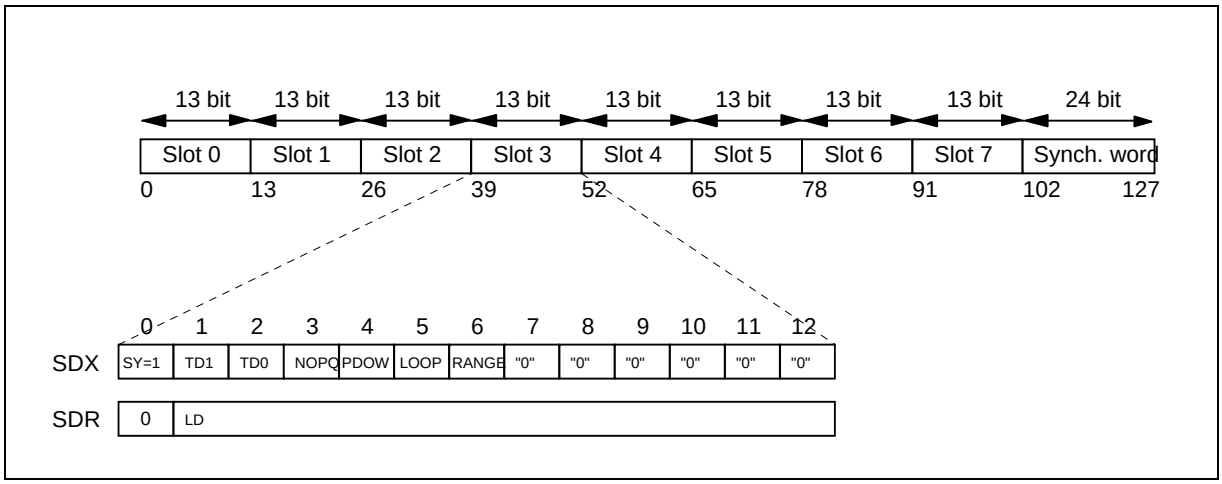


Figure 9
Frame Structure on SDX and SDR

The following data is transmitted on SDX from the DFE-T to the AFE :

NOPQ: The no-operation-bit is set to ZERO if none of the control bits (PDOW, RANGE and LOOP) shall be changed. The control bits on SDX then are set to ZERO to reduce digital cross-talk to the analog signals. The values of the control bits of the assigned line port are latched by the Quad IEC AFE.

The NOPQ bit is set to ONE if at least one of the control bits shall be changed. In this case all control bits are transmitted with their current values.

PDOW: If the PDOW bit is set to ONE, the assigned line port is switched to power down. Otherwise it is switched to power up.

RANGE: RANGE = ONE activates the range function of the Quad IEC AFE, otherwise the range function is deactivated. "Range function activated" refers to high input levels as they occur at short loop lengths.

LOOP: LOOP = ONE activates the loop function of the Quad IEC AFE, i.e. the analog loop is closed. Otherwise the line port of the Quad IEC AFE is in normal operation.

SY: First bit of the time slots with transmission data. For synchronisation and bit allocation on SDX,SY is set to ONE on SDX and set to ZERO on SDR.

"0": reserved bit. Reserved bits are currently not defined and set to ZERO. Some of these bits may be used for test purposes or can be assigned a function in later versions.

The following data is transmitted on SDR from the AFE to the DFE-T:

SY: First bit of the time slots with transmission data. For synchronisation and bit allocation on SDX,SY is set to ONE on SDX and set to ZERO on SDR.

LD: The Level-Detect bit indicates an analog signal being recognized at the line inputs of the AFE. The DFE-T will evaluate whether this signal is the wake-up signal "TN". LD being constantly tied to either ONE or ZERO indicates "no signal on U". LD changes from ONE to ZERO with the period of the signal detected by the AFE.

Table 6
Assignments of Time-Slots on SDX/SDR to Line Ports

Time-Slot No.	Line Port No.
1	0
3	1
5	2
7	3

The assignment of the channels 0 to 3 to the time slots on SDX is given in table 5.The 4B3T data is coded with the bits TD1 and TD0. The Quad IEC AFE will transmit the ternary pulses according to table 6.

Table 7
Coding of the 4B3T transmit pulse

4B3T Data Pulse	TD1	TD0
0	0	0
+ 1	1	0
– 1	1	1

3.2.3 Boundary Scan Test Controller

The Quad IEC DFE-T provides a boundary scan support for a cost effective board testing. It consists of:

- Complete boundary scan for 46 signals (pins) according to IEEE Std. 1149.1 specification
- Test access port controller (TAP)
- Four dedicated pins (TCK, TMS, TDI, TDO)
- One 32-bit IDCODE register
- additional test command performing "send single pulses" mode

Boundary Scan

All pins except the power supply pins, the "not connected" pins and pins TDI, TDO, TCK, TMS are included in the boundary scan.

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

Depending on the pin functionality one, two or three boundary scan cells are provided. Note, that there are several pins, which for chip test are used as I/O pins. Please refer to section 1.2 whether these pins are inputs or outputs. However, they are included to the boundary scan as I/O pins with three scan cells.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	input
Output	2	output, enable
I/O	3	input, output, enable

The pins are included in the following sequence in the boundary scan:

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
1	63	TP1	I	1
2	62	TP2	I	1
3	61	CLS3	O	2
4	60	RESQ	I	1
5	56	TSP	I	1
6	55	SLOT	I	1
7	53	LT	I	1
8	52	CLS2	O	2
9	51	D3D	I/O	3
10	50	D2D	O	2
11	49	TP3	I	1
12	48	D1D	I/O	3
13	47	D0D	I/O	3
14	46	D3C	I/O	3

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
15	44	D2C	I/O	3
16	43	D1C	I/O	3
17	42	D0C	I/O	3
18	40	D3B	I/O	3
19	39	D2B	O	2
20	37	D1B	O	2
21	35	D0B	O	2
22	34	D3A	O	2
23	33	D2A	O	2
24	31	D1A	O	2
25	30	D0A	O	2
26	29	CLS0	O	2
27	28	ST00	I	1
28	27	ST01	I	1
29	26	ST10	I	1
30	24	ST11	I	1
31	23	ST20	I	1
32	21	ST21	I	1
33	20	CLS1	O	2
34	19	ST30	I	1
35	18	ST31	I/O	3
36	17	SDX	O	2
37	15	DOUT	O	2
38	14	DIN	I	1
39	13	FSC	I/O	3
40	12	DCL	I/O	3
41	11	PDM0	I	1
42	10	PDM1	I/O	3
43	8	PDM2	I	1
44	7	PDM3	I	1

Boundary Scan Number TDI –––>	Pin Number	Pin Name	Type	Number of Scan Cells
45	5	SDR	I/O	3
46	4	CL15	I	1

Note: I/O pins are bidirectional only for device test purpose. For the function of these pins refer to section 1.2.

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

Following the standard definition 5 instructions are executable. Additionally, there is one specific test instruction.

TAP controller instructions:

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code
01xx	reserved	
1000	reserved	
1001	reserved	
1010	SSP	Send single pulses
1011	reserved	
11XX	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 0001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code		Output
0001	0000 0000 0010 1010	0000 1000 001	1	--> TDO

Note: In the state "test logic reset" the code "0011" is loaded into the instruction code register.

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

SSP does the same as setting the pins TSP and RESQ in SSP-mode. Single alternating pulses are issued to the Quad IEC AFE on all ports via the SDX pin.

3.3 Maintenance Functions

3.3.1 Loops

For test of the line cards, several test loops are provided which can be controlled from the exchange. When a test loop is closed, all channels (B + B + D) are looped back and data from the other end of the line is ignored. There are no separate loops for single channels.

All test loops are transparent loops. During test loops, the line signal is still transmitted. Nevertheless, the NT receives this signal and synchronizes on it. It can not distinguish between line signals sent from LT during loop 1 or loop 4, and signals sent during normal operation.

3.3.1.1 Switching an Analog Loop

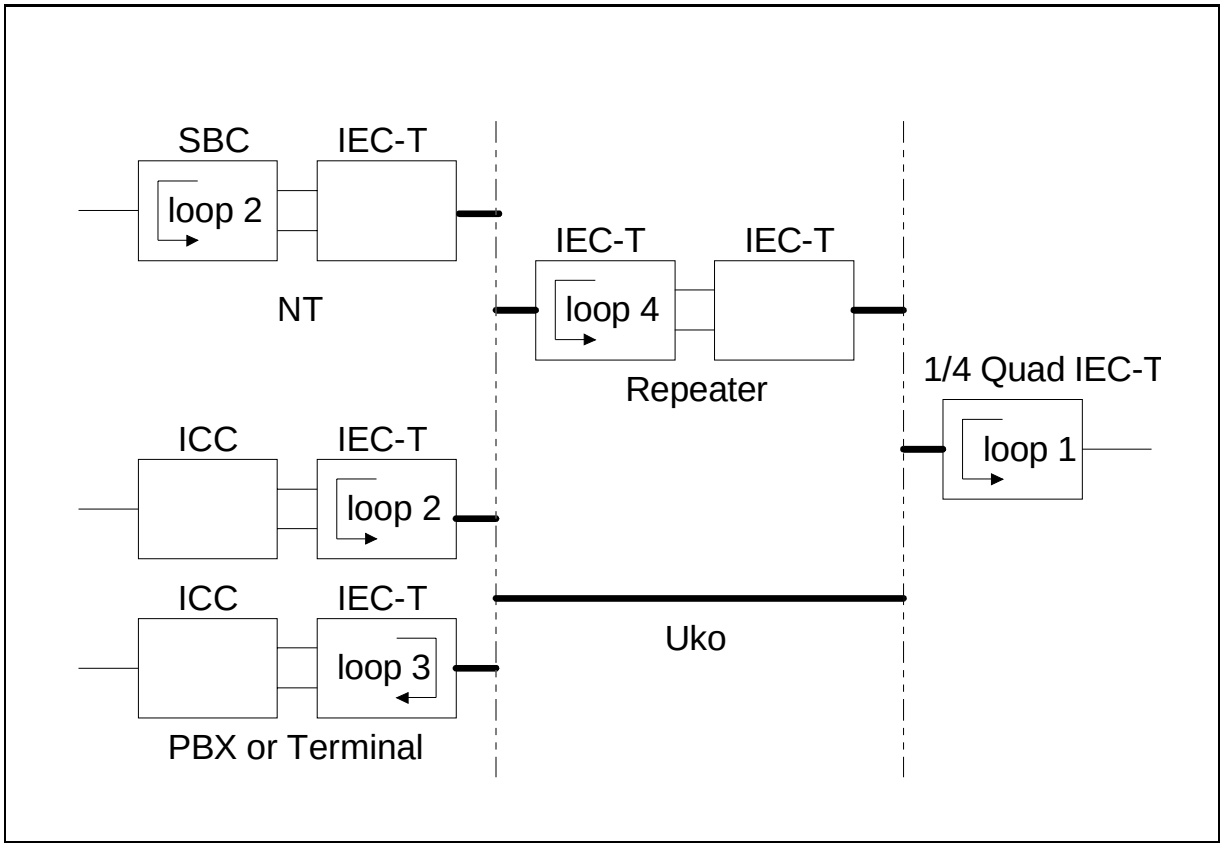


Figure 10
Test Loops Closed by the Quad IEC or under its Remote Control

Loops 1 and 4 are closed in the IEC as near to the Uk0 interface as possible. Using internal switches in the Quad IEC AFE, the signal from the line driver is fed back directly to the input. It is like a short-circuit between the pins AOUT and AIN as well as between

BOUT and BIN. The input signal from the hybrid is ignored in this mode. These loops also are referred to as "analog loops".

The analog loop mode is controlled via the IOM-2 C/I-channel. In an analog loop, the transmit path is set to LT mode and the receive path is set to the NT mode.

3.3.1.2 Switching Loop 2 in the NT

The loop 2 can be closed in the NT by command from the LT side. With an internal switch, the user data on DOUT (B + B + D) is directly fed back into DIN.

3.3.1.3 Remote Control of Loop 4 and Loop 2 by the Quad IEC DFE-T

These remote loops are controlled by the exchange via C/I-channel of the Quad IEC DFE-T . The command for closing loop 4 or loop 2 is transmitted from the exchange on the Uk0 interface in the 1 kBaud M-channel (position 85 downstream in the Uk0 frame from LT to NT/NT-Repeater).

To command the IEC LT-repeater to close loop 4, the NT-repeater has to find alternating plus and zero polarity within 8 subsequent frames in the M-channel (+ 0 + 0 + 0 + 0 ...).

To command the SBC in the NT to close loop 2, the IEC in the NT has to find continuous plus polarity within 8 subsequent frames in the M-channel (+ + + + + + + + ...). The same code has to be found by the IEC NT-PBX or NT-TE to close loop 2 itself.

To open closed loops, the NT has to find continuous zero polarity within 8 subsequent frames in the M-channel (0 0 0 0 0 0 0 0 ...) or at deactivation. During normal transmission without loops, the M symbol is set to zero (or minus **see section 3.4**).

The NT-RP, when detecting positive M symbols, does not close loop 2, but hands them over to a PEB 20901/20902 LT-RP via it's IOM-1 interface with a low in the E bit of 8 subsequent IOM frames. Negative or zero M symbols cause 8 high E bits.

3.3.2 Monitoring of Code Violations

The NT transmitts a postive M symbol upstream if any code error has been detected within a frame (position 25 upstream in the Uk0 frame from NT to LT).

The Quad IEC DFE-T contains an error counter for each channel which counts Uk0 frames with at least one detected code violation. Additionally, the frames with a received positive M symbol are counted. The error counter can be read and simultaneously reset from a certain state of activation via the IOM-2 interface. The counter is always stopped after reaching 255 which is the maximum value passed to the MONITOR-channel.

The counter is automatically reset during deactivation of the Uk0 line. It is enabled again to count code violations from the moment the RDS code is written into the IOM-2 C/I-channel, indicating that the line is sychronized.

Each counted frame with a detected code violation leads to 10 to 20 binary bit errors on average. So a bit error rate of 10^{-7} in both directions leads to about 2 detected frame

errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M symbol).

3.4 Control Procedures

A "Call-by-Call" activation or deactivation of the transmission link is provided for ISDN basic access. In a deactivated state, the line and the terminal equipment (if it is not a remote power fed device) are powered down. The entire transmission link, consisting of one or more individual lines, has to be activated to enable the connection between terminal equipment (TE) and exchange (LT).

The activation procedure is always initiated by one of the two end points and is handled between them. The deactivation procedure can be initiated only by the exchange.

Seven states of activation of transmission lines can be distinguished.

1. Activation of the link is initiated by one of the two ends.
   - Line awake: Each individual line is being awoken, but is not yet synchronized, data transmission is not yet possible
   - Synchronization downstream: synchronization is always done downstream first, the whole line has to synchronize on the exchange
   - Synchronization upstream: Because the delay differs from line to line, bit synchronization is necessary in the LT
   - Synchronized: All layer 1 units of the link are told by the exchange that synchronization has been finished
2. Transparent: In the activated state, the user data is transmitted from exchange to TE and vice versa.
3. Deactivation is done in two steps on each individual line separately.
   - Deactivation request downstream
   - Deactivation acknowledge upstream

The transmission link is totally deactivated thereafter.

To save time, each section of line does not have to wait for the transition of the entire line before it is able to proceed to the next state. Therefore the individual line sections may be at different states of activation.

To control the procedures, some control information has to be transmitted over the lines (Uk0 interface, S-bus). Therefore, special signal elements on the Uk0 interface have been specified. In the IOM-2 interface, the 32 kbit/s C/I-channel is provided to exchange the necessary control information.

The IOM-2 interface and the Uk0 interfaces are defined to prohibit states which cannot be left with normal commands and infos. Deactivation of the line leads all devices to defined states. Nevertheless, it is recommended to implement a power-on reset at pin $\overline{\text{RES}}$ to start in a defined manner, and to shorten the first deactivation and activation.

The usage of the two input pins, $\overline{\text{RES}}$ and TSP has the same effect as inputs RES and SSP in the C/I-channel. They always overwrite the IOM-2 C/I-channel input.

3.4.1 Activation and Deactivation of Uk0 Transmission Lines

On Uk0, the exchange of control information is partially state oriented. Some signal elements are given as long as no other information has to be transferred, other signal elements have distinct durations.

3.4.1.1 Awake Protocol

To awake the Uk0 interface and the idle modules, an awake and an acknowledge signal have been defined (**see section 4.10**)

Procedure for awaking one port of the Quad IEC DFE-T

After sending the awake signal, the awaking device waits for the acknowledge. After 12 ms, the awake signal is repeated, if no acknowledge has been recognized.

If an acknowledge signal has been recognized, the Quad IEC DFE-T waits for its possible repetition (in case of previous coincidence of two awake signals). If no repetition was detected, the IEC starts transmitting INFO U2 with a delay of 7 ms.

If such a repetition is detected, the Quad IEC DFE-T interprets it as an awake signal and behaves like a device awoken by the far end.

Procedure in the Quad IEC DFE-T to be awoken

If a deactivated device detects an awake signal on Uk0, an acknowledge signal is sent out. After that, the Quad IEC DFE-T waits for a possible repetition of the awake signal (in case the acknowledge hasn't been recognized). If no repetition is found, the awoken IEC starts sending INFO U2 after 7 ms from detecting the awake signal. If a repeated awake signal is found, the procedure in the awoken IEC starts again.

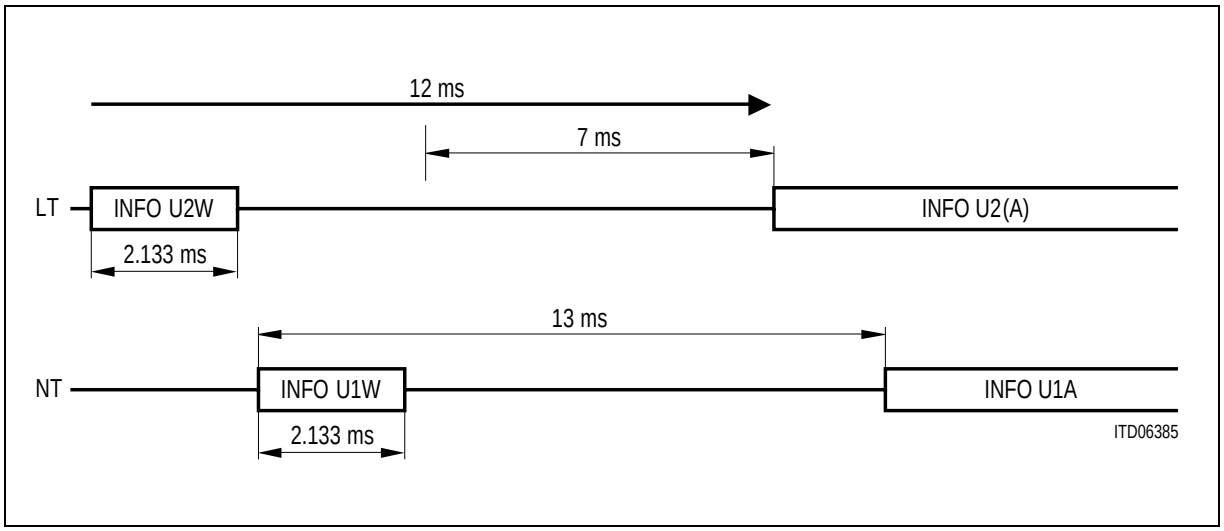


Figure 11
Procedure for Awake Downstream

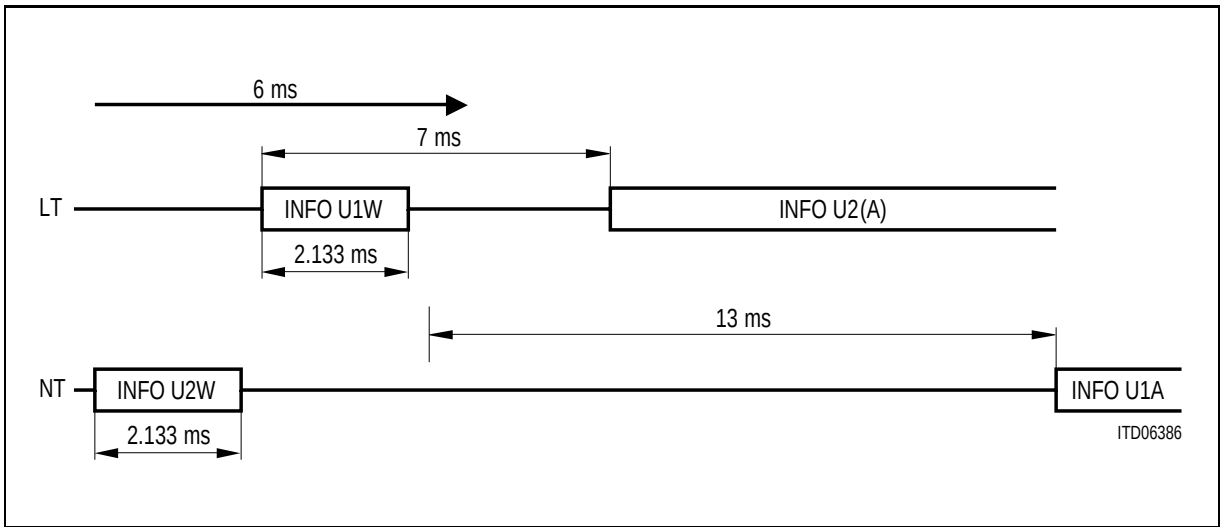


Figure 12
Procedure for Awake Upstream

3.4.1.2 Procedures for Normal Activation with NT

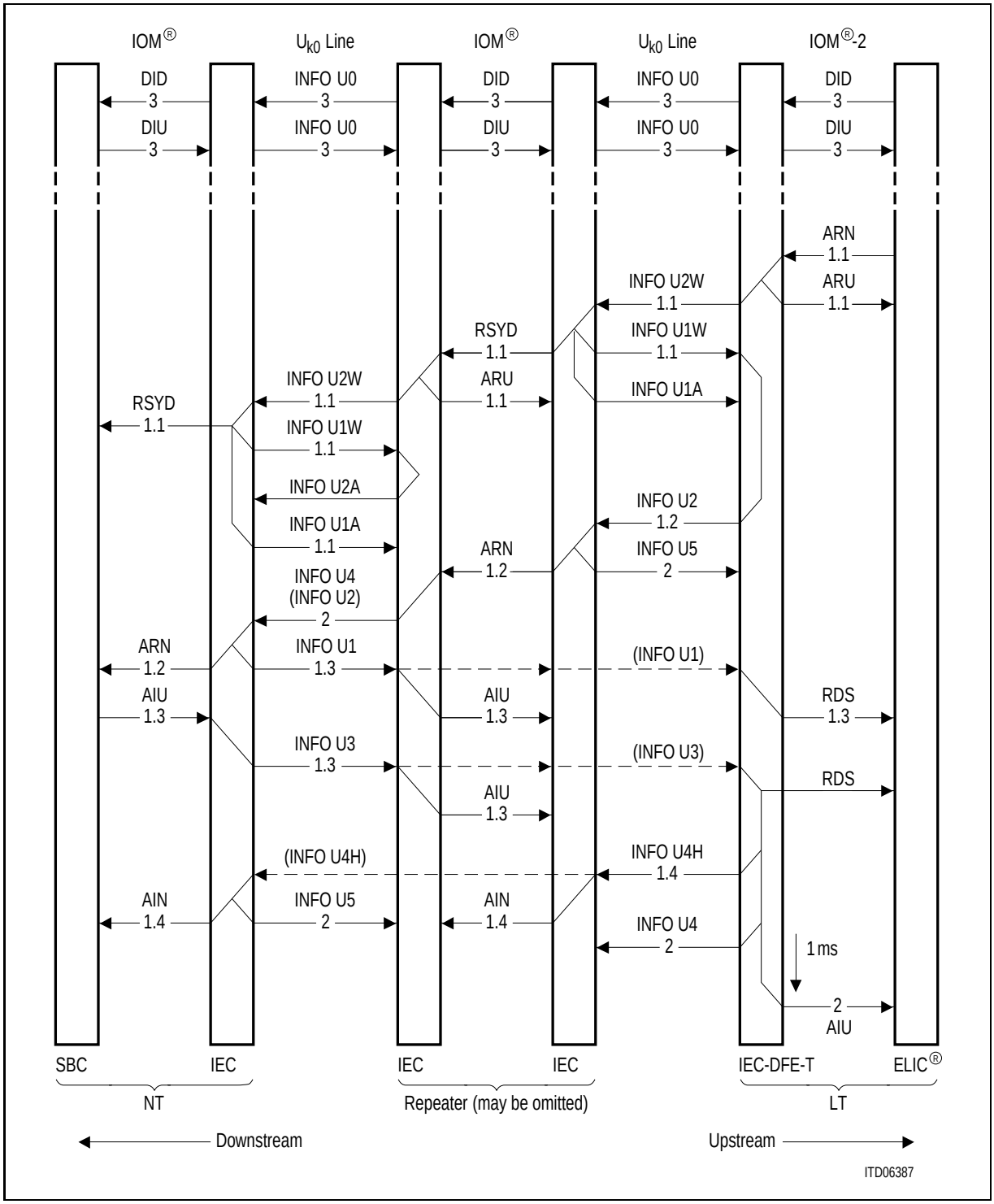


Figure 13
Activation of Uk0 Link Initiated by LT

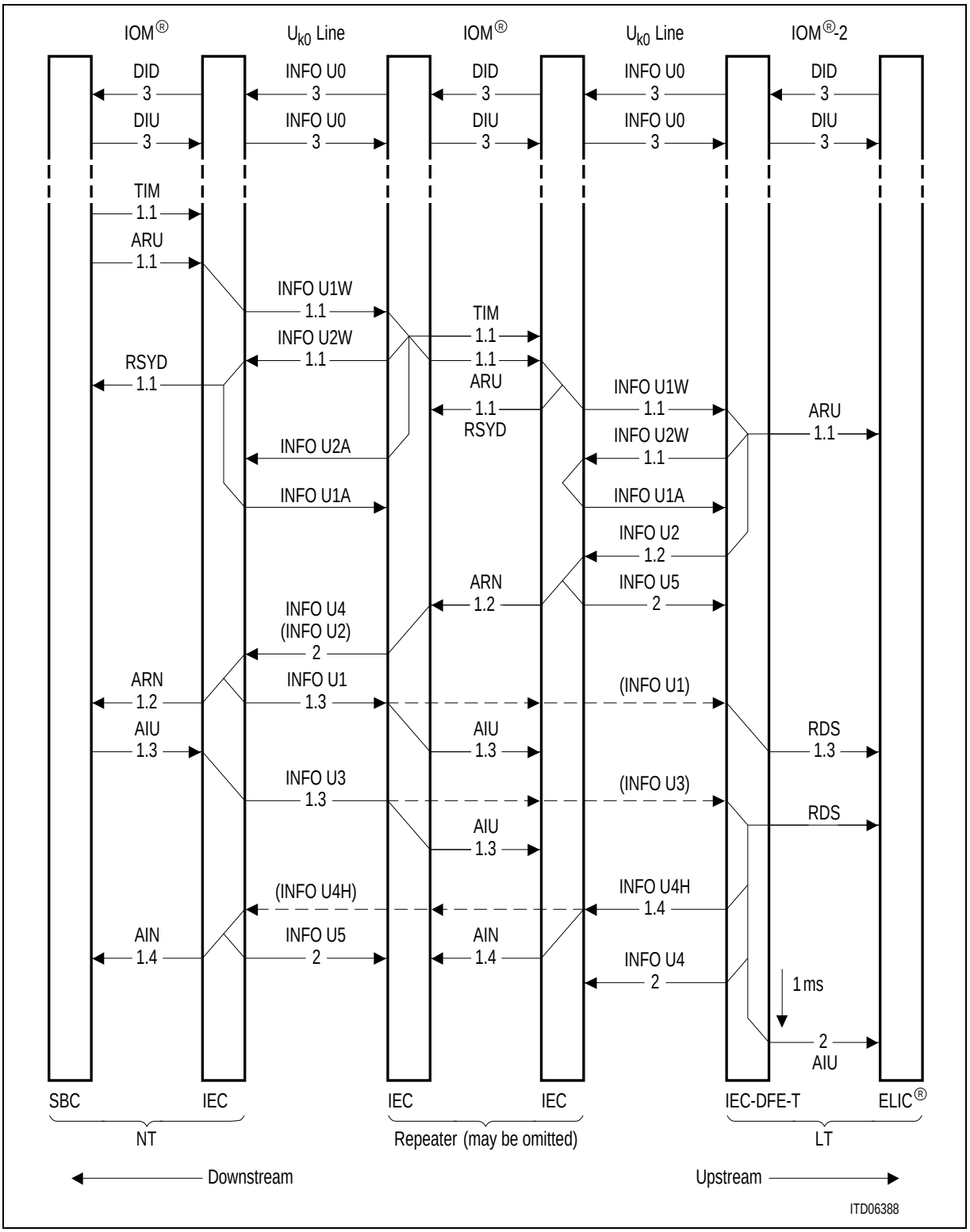


Figure 14
Activation of Uk0 Link Initiated by NT

3.4.1.3 Procedures for Normal Activation with NT-PBX or NT-TE

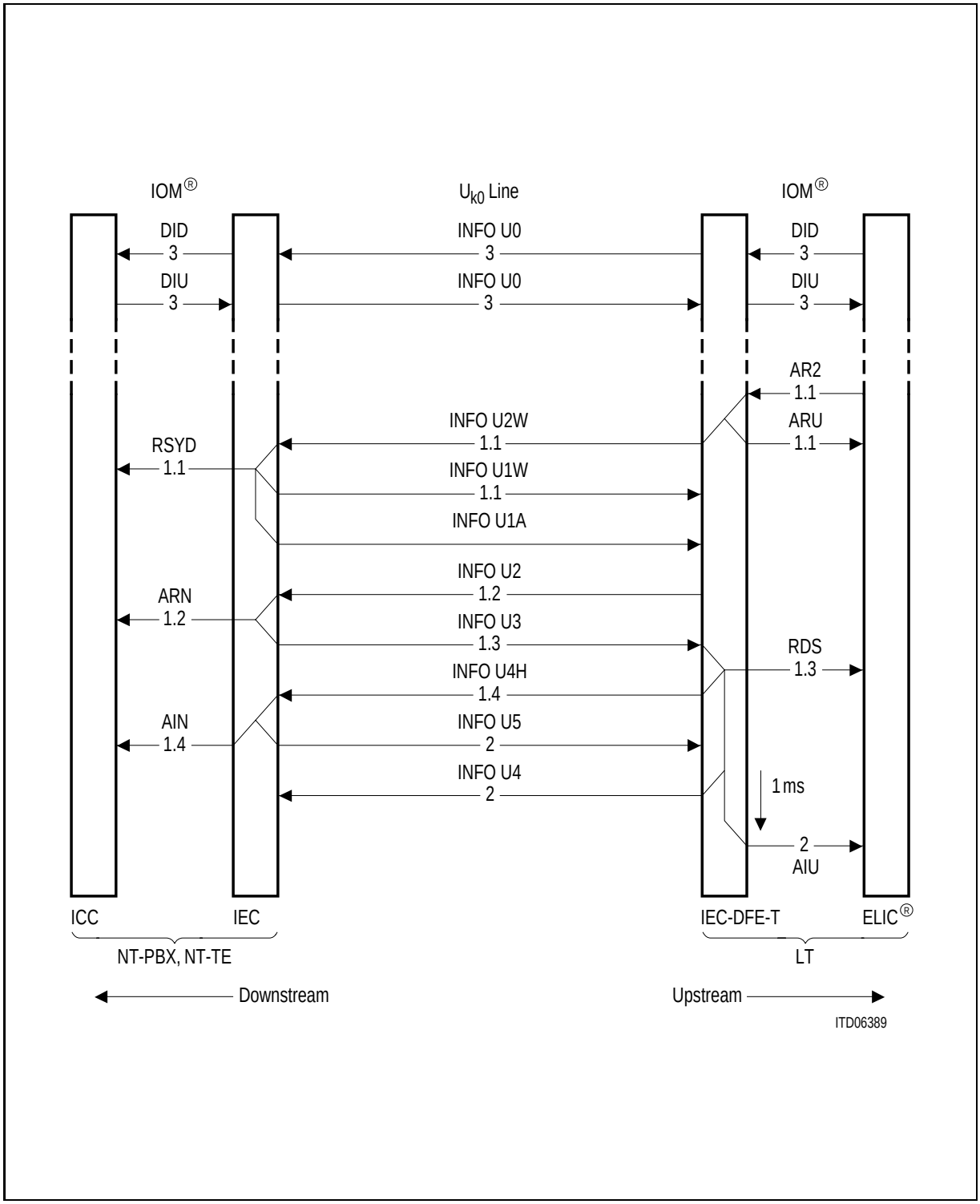


Figure 15
Activation of Uk0 Link with NT-PBX or TE Initiated by LT

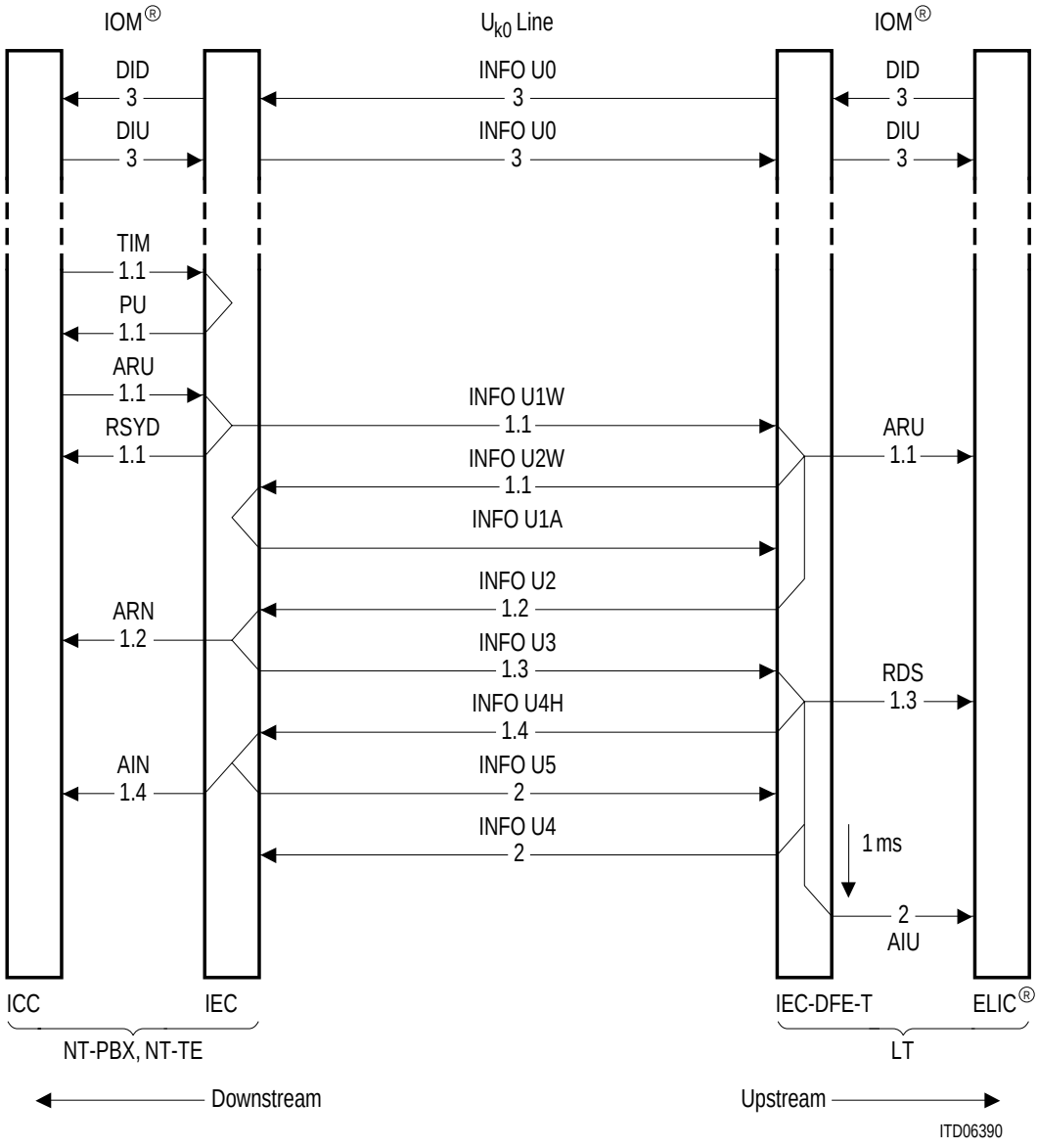


Figure 16
Activation of Uk0 Link with NT-PBX or TE Initiated by NT

3.4.1.4 Procedures for Activation of Loops

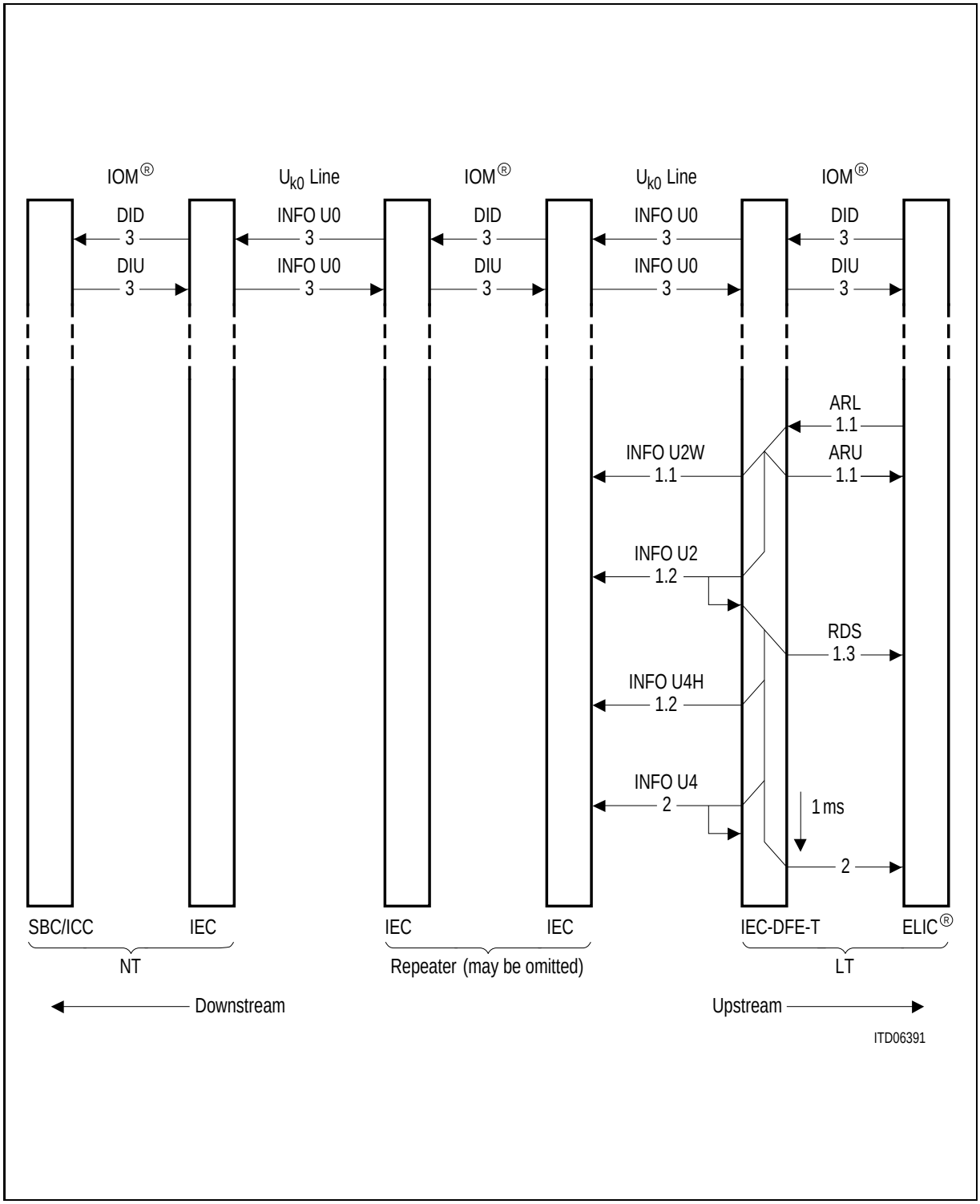


Figure 17
Activation of Loop1

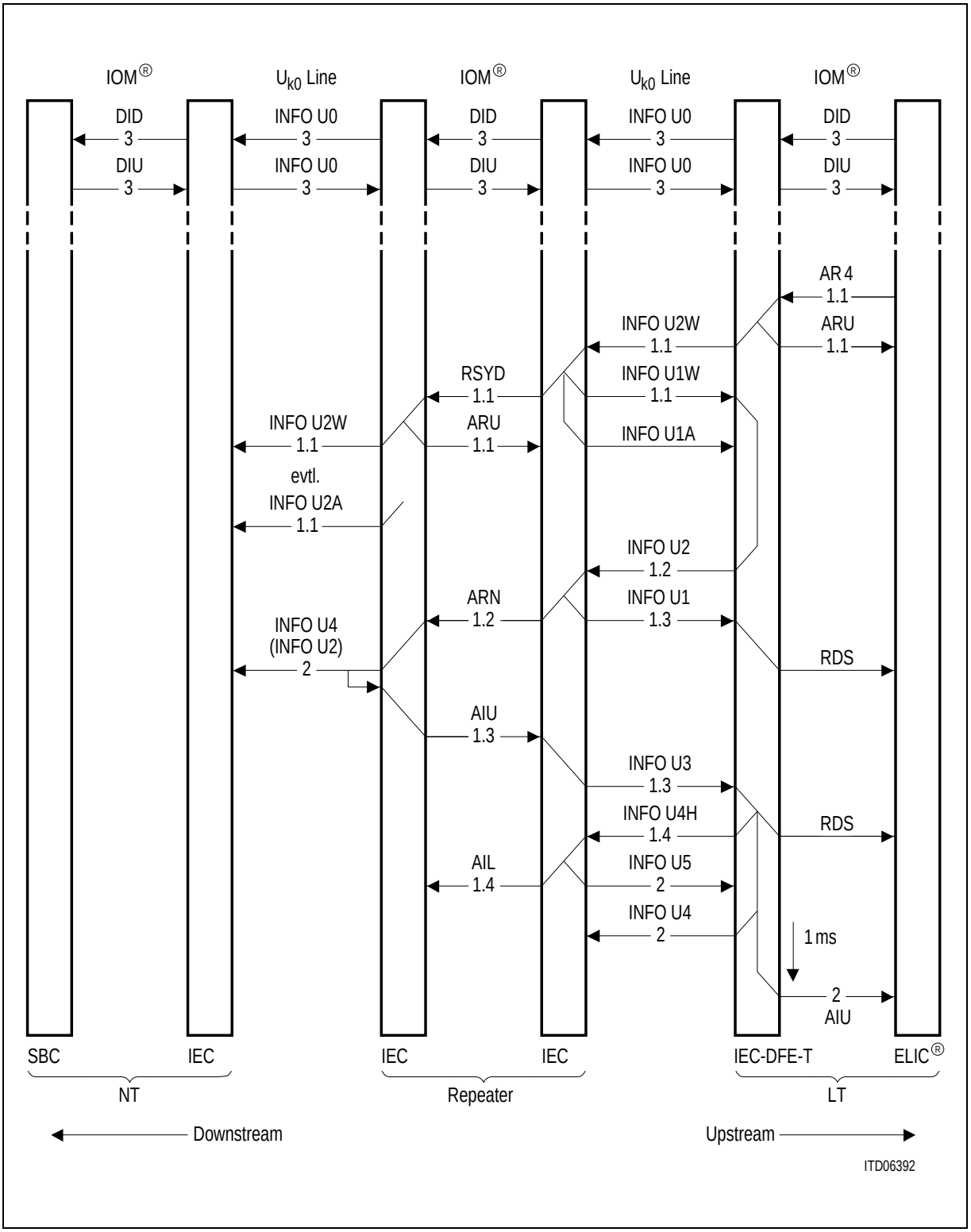


Figure 18
Activation of Loop 4

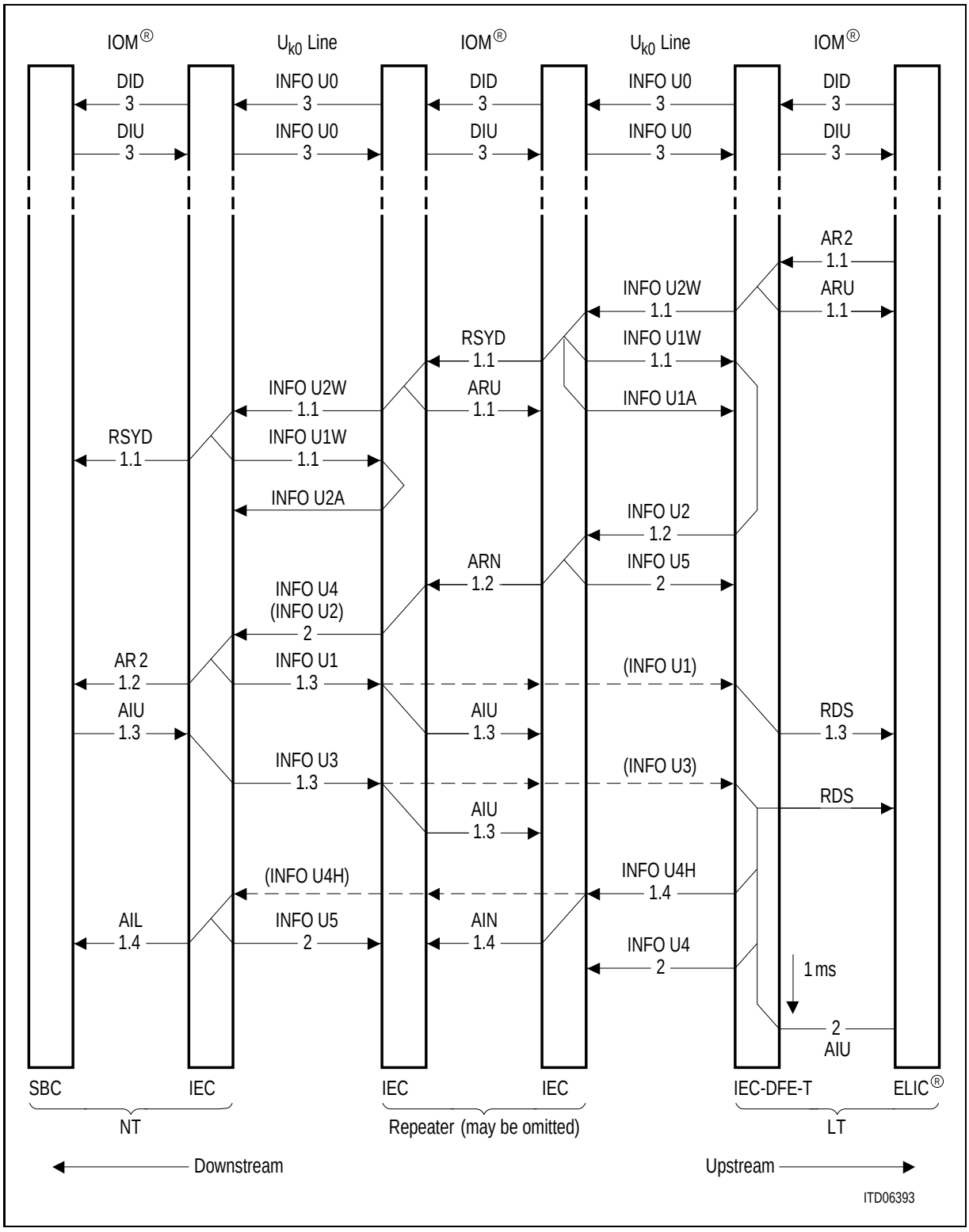


Figure 19
Activation of Loop 2 with NT

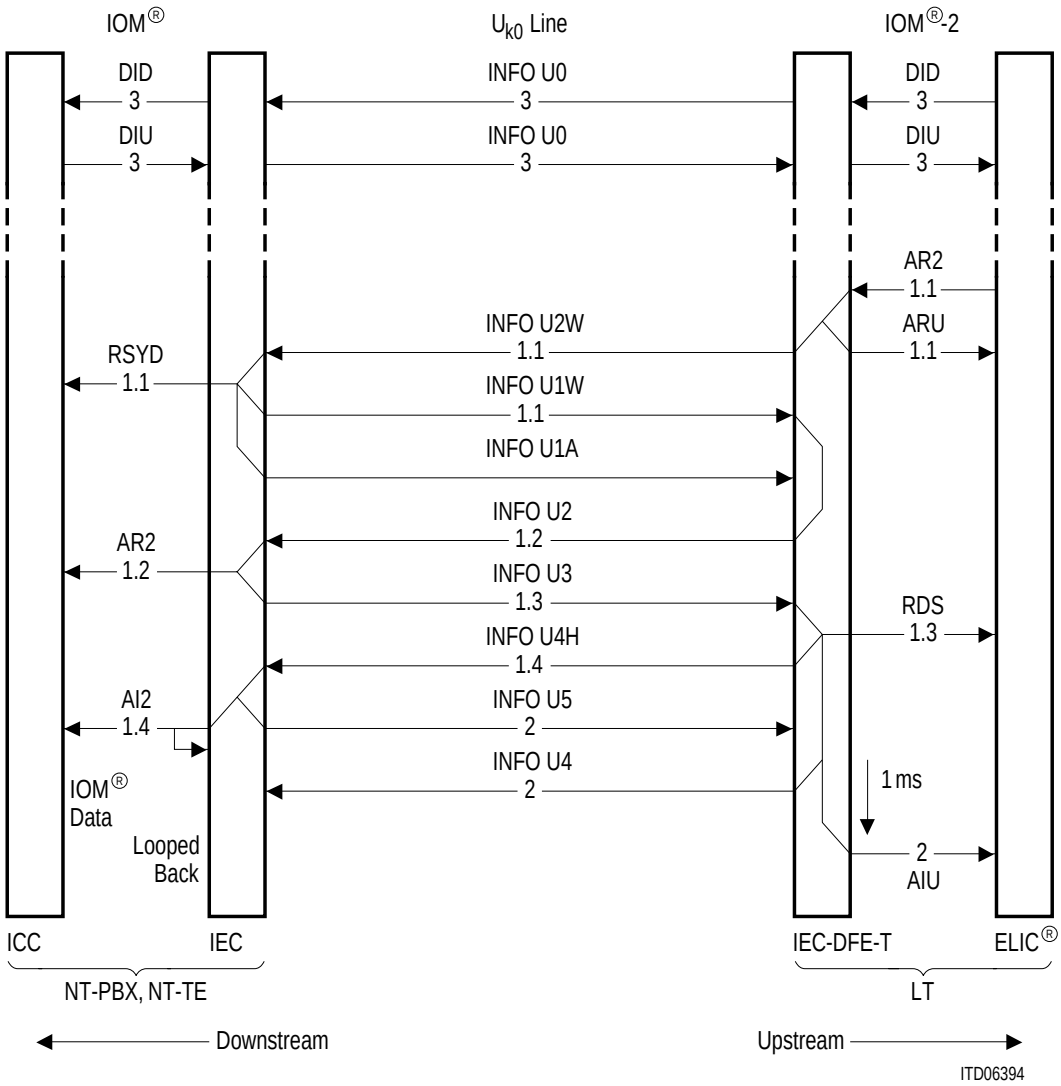


Figure 20
Activation of Loop 2 within NT-PBX or TE

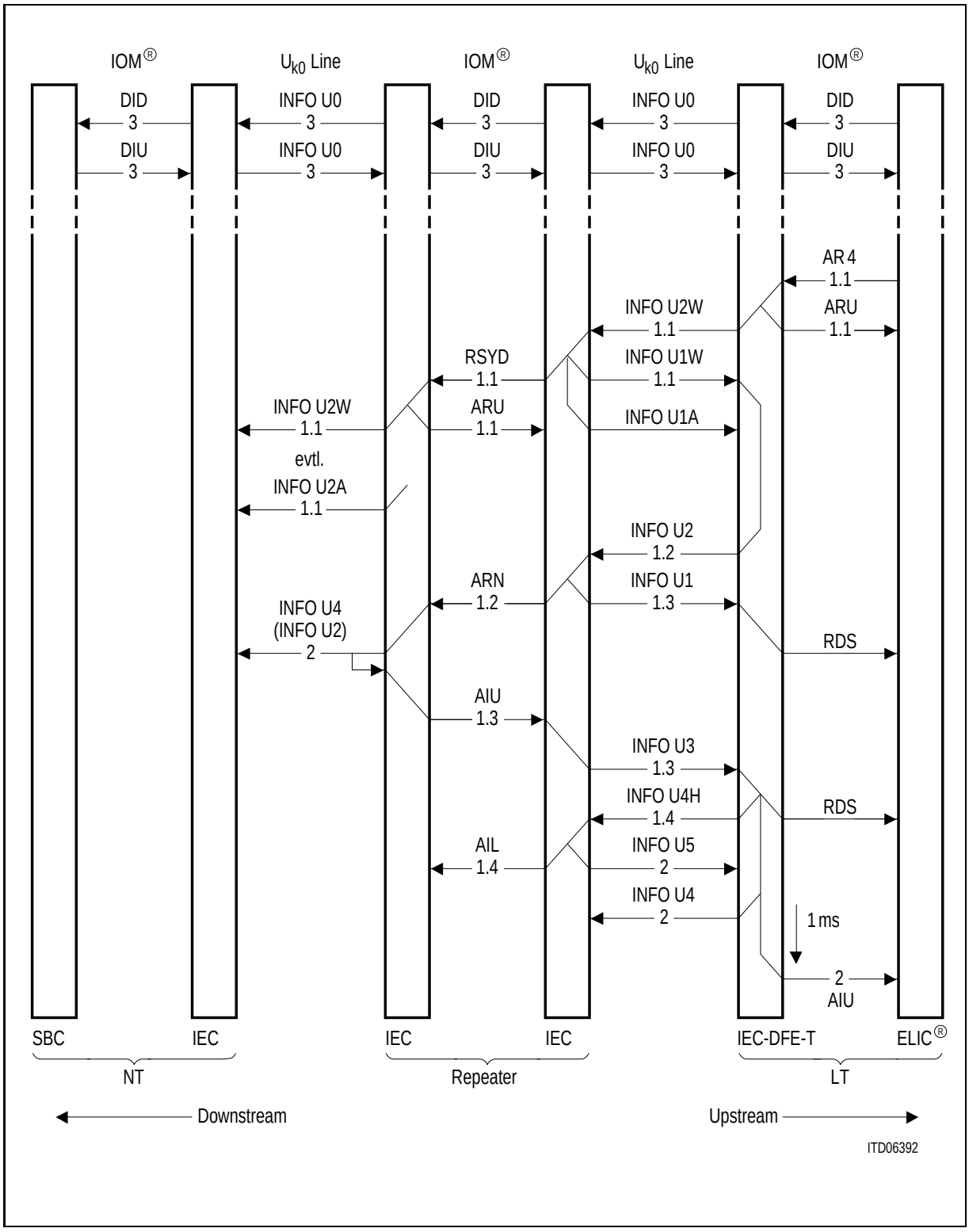


Figure 21
Activation of Loop 3 within NT-PBX or TE

3.4.1.5 Procedure for Deactivation

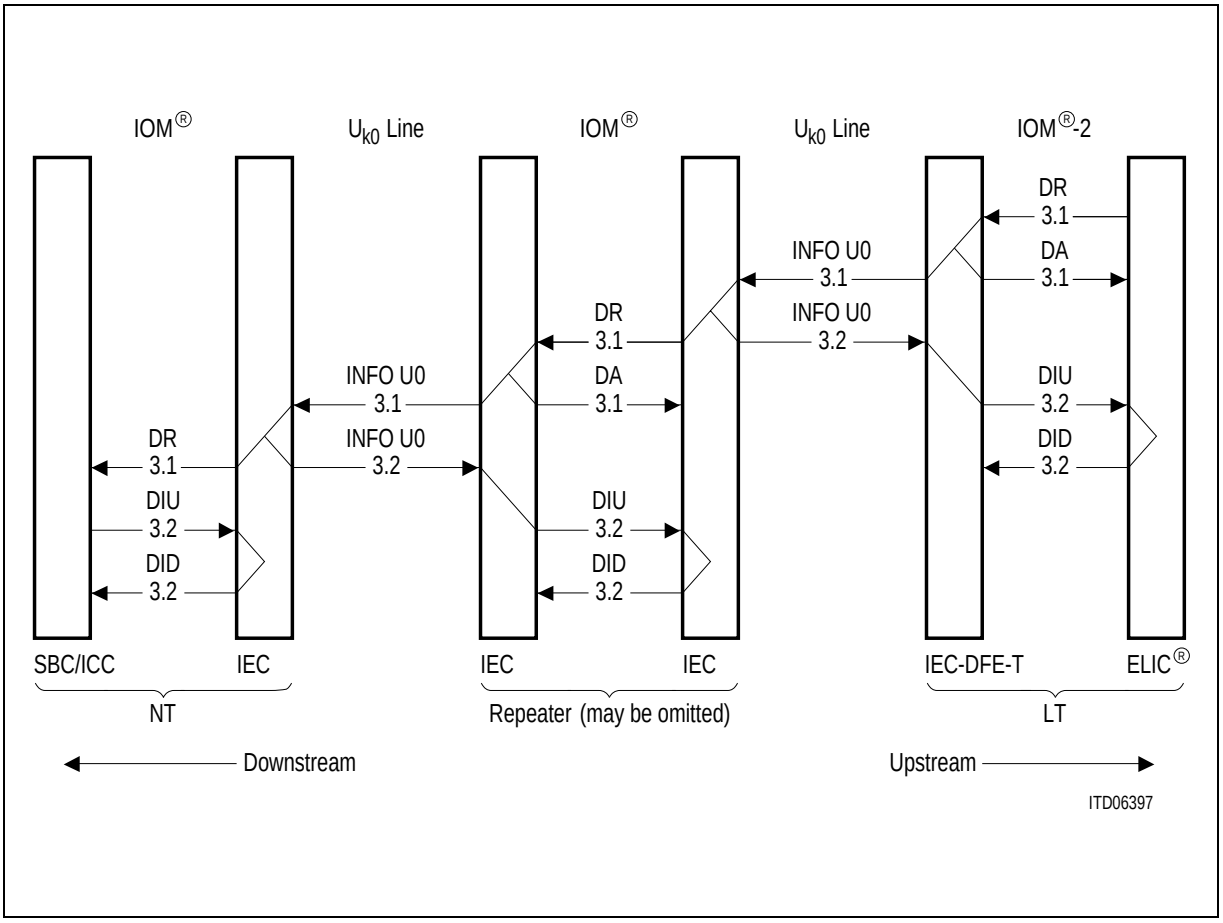


Figure 22
Deactivation of Uk0 Link, always Initiated by LT

3.4.2 IOM-2 Control Information in the C/I-Channel

The control information in the C/I-channel depends on the state of activation. Each code in the C/I-channel is repeated in each IOM frame until a change is necessary. In the layer 2 device (PEB 20550 ELIC), the code is changed by the controlling processor which overwrites a special register with a new code. In the layer 1 transceiver, like the PEB 24901/24902 Quad IEC-T, a change of C/I-channel code is the result of a detected signal element on the line or a time-out during (de-)activation.

To detect a change in the C/I-channel, the new code must be found in two successive IOM frames to be considered valid (double last look criterion). If the receiving device accepts the new code, it results in a new line signal or in closing a loop directly in the device. A layer 2 device then gives an interrupt request to the processor to hand over the new control information.

Based on these protocols, control information is given downstream (directed from the exchange to the terminal equipment) or upstream (directed from the terminal equipment to the exchange) from one end point to the other via one or more parts of the whole transmission line.

3.4.2.1 IOM-2 C/I codes for (De-)Activation Downstream

ARD	10– –	**Activation Request Downstream**. The upstream unit of the IOM-2 interface is a layer 1 device which has just finished synchronizing. Or, it is a layer 2 device (which does not synchronize) initiating activation. Receiving this, the Quad IEC DFE-T in the exchange starts by sending awake signal INFO U2W. After a successful awake procedure, the IECQuad DFE-T sends INFO U2. ARD represents the following group of activation requests: ARN 1000 Activation Request no loop. ARL 1001 Activation Request local loop only in the exchange. AR2 1010 Activation Request loop 2 in the NT. AR4 1011 Activation Request loop 4 only in the repeater. For the description of the loops **see section 3.3**.
DR	0000	**Deactivation Request**. The upstream unit of the IOM-2 interface requests deactivation. This command must be applied at least 0.5 ms to ensure that the downstream unit has reached the requested state, after the information on the C/I-channel has been evaluated.
DID	1111	**Deactivation Indication downstream**. DID informs the downstream unit that the upstream unit is also deactivated. The layer 1 devices are now ready to receive awake signals; the IOM-2 interface may be powered down after 4 IOM frames.

3.4.2.2 IOM-2 C/I codes for (DE-)Activation Upstream

ARU	1000	**Activation Request Upstream**. The downstream unit of the IOM-2 interface has detected an awake signal on the line or requests activation, if it is a layer 2 device.
RDS	0111	**Running digital sum is readable**. The downstream unit of the IOM-2 interface (usually a layer 1 device) has detected the line signal which informs that the whole Uk0 interface is synchronized (INFO U1 or U3 detected on Uk0). At this point, the counter of frames with detected code violations is enabled.
AIU	1100	**Activation Indication Upstream**. The downstream unit of the IOM-2 interface (usually a layer 1 device) has detected the line signal which informs that the whole transmission line to the TE is synchronized (INFO U3 on Uk0). In the exchange, the IEC switches itself to the transparent state and controls the transition to the transparent state of the other layer 1 devices. It informs layer 2 that the whole line is now transparent.
DA	0001	**Deactivation Acknowledge**. DA informs the upstream unit that the IEC is deactivating the transmission line downstream. This indication is given out to overwrite a possible DIU code in the C/I-channel upstream to enable the ICC to detect the change to DIU which follows afterwards.
DIU	1111	**Deactivation upstream**. DIU informs the upstream unit that the transmission line downstream is deactivated. The downstream unit is in the power-down state. The transmitter is disabled, but awake signals may be detected.
RSYU	0100	**Resynchronizing Indication upstream**. RSYU informs the upstream unit that the downstream unit isn't synchronous. RSYU is given, if the IEC (LT or LT-RP) was in the fully activated state and has lost synchronization afterwards (but transmission of INFO U4 will not be interrupted).

3.4.2.3 IOM-2 C/I codes to the Quad IEC DFE-T for Test and Maintenance

LTD	0011	**Line Termination Disable**. In the LT, the Quad IEC DFE-T stops transmitting signals (INFO U0) on the correwsponding channel, ignoring awake signals. The channel is set to power-down. This command is used to keep the Uk0 interface deactivated (e.g. due to a continuous fault).
RES	1101	**Reset**. Any stored settings except the driver pins are erased. The corresponding channel goes to the power-up state, but no line signal will be sent out. An applied low on $\overline{\text{RES}}$ pin, while TSP is low, has the same effect for all four channels together.
SSP	0101	**Send Single Pulses**. Thechannel goes to the power-up state and sends single pulses with a period of 1 ms. An applied high on the TSP pin, while $\overline{\text{RES}}$ is high, has the same effect on all four channels together.
TEST	0110	**Test mode**. The channel goes from any mode and at any state of activation to the transparent state (sends INFO U4/U5). An applied low on $\overline{\text{RES}}$ pin, while TSP is high, has the same effect on all four channels together.

3.4.2.4 Summary of IOM-2 Control Informations

Table 8
Summary of Codes in C/I-Channel

Code	Command	Indication
A1...A4	**DIN**	**DOUT**
0 0 0 0	DR	
0 0 0 1		DA
0 0 1 0		
0 0 1 1	LTD	
0 1 0 0		RSYU
0 1 0 1	SSP	
0 1 1 0	TEST	
0 1 1 1		RDS
1 0 0 0	ARN	ARU
1 0 0 1	ARL	
1 0 1 0	AR2	
1 0 1 1	AR4	
1 1 0 0		AIU
1 1 0 1	RES	
1 1 1 0		
1 1 1 1	DID	DIU

3.4.3 Meaning of Uk0 INFOs

INFO U0	Deactivation signal of both directions. Downstream, it is the command to deactivate the NT. Upstream, it is the acknowledge of deactivation of the NT.
INFO U1W	Awake or acknowledge signal upstream used in the awake procedure of the Uk0 interface.
INFO U2W	Awake or acknowledge signal downstream used in the awake procedure of the Uk0 interface.

INFO U2	The LT (and LT-RP, if the NT-RP is synchronized) sends INFO U2 to enable the own echo canceller to adapt the coefficients, and with the Barker code the NT at the other end is enabled to synchronize. The M-channel on Uk0 may be used to transfer loop commands. Recognizing INFO U2 is used as a criterion for synchronization.
INFO U2A	While the IEC NT-RP is synchronizing on the received signal, the IEC LT-RP sends out INFO U2A to enable its echo canceller to adapt the coefficients, but sending no Barker code it inhibits the NT (-TE, -PBX) to synchronize on the still asynchronous signal. Due to proceeding synchronization, the Uk0 frame may jump from time to time. INFO U2A can not be detected in the IEC NT at the far end.
INFO U1A	While the IEC (in all NT modes) is synchronizing on the received Signal, it sends out INFO U1A to enable its echo canceller to adapt the coefficients, but sending no Barker code it inhibits the LT (-RP) to synchronize on the still asynchronous signal. Due to proceeding synchronization, the Uk0 frame may jump from time to time. INFO U1A can’t be detected in the IEC LT at the far end.
INFO U1	When synchronized, the IEC (in all NT modes) sends the Barker code and the LT (-RP) may synchronize itself. INFO U1 indicates additionally that a terminal equipment hasn’t yet activated. When receiving INFO U1, the IEC indicates the synchronized state with RDS to layer 2. Usually during activation, no INFO U1 is detected in the LT because the TE is activated first and INFO U1 changes to INFO U3 before being detected. The M-channel on Uk0 may be used to transfer code error indications and 1 kbit/s transparent data.
INFO U3	When detecting INFO U3, the IEC LT in the exchange is allowed to command the transition to the fully transparent state, because it indicates that the whole link to the TE is synchronous in both directions. The M-channel on Uk0 may be used to transfer code error indications and 1 kbit/s transparent data.
SI	The IEC sends periodically single pulses spaced 1 ms to the Uk0 interface to ensure that it is within the specified pulse mask.
INFO U4H	With INFO U4H, each unit is commanded to go to the transparent state. When detecting this, the IEC NT stops sending INFO U3 and indicates This to the SBC or layer 2 device, ICC, via the IOM-2 interface. The M-channel on Uk0 may be used to transfer loop commands and 1 kbit/s transparent data.

INFO U4	INFO U4 means fully transparent data, the M-channel on Uk0 may be used to transfer loop commands and 1 kbit/s transparent data.
INFO U5	INFO U5 means fully transparent data, the M-channel on Uk0 may be used to transfer code error indications and 1 kbit/s transparent data.

3.4.4 State Diagrams

The following state diagrams describe all the action/reaction resulting from any command or detected signal and resulting from the various operating modes.

The states, inputs and outputs are characterized as shown in the following example:

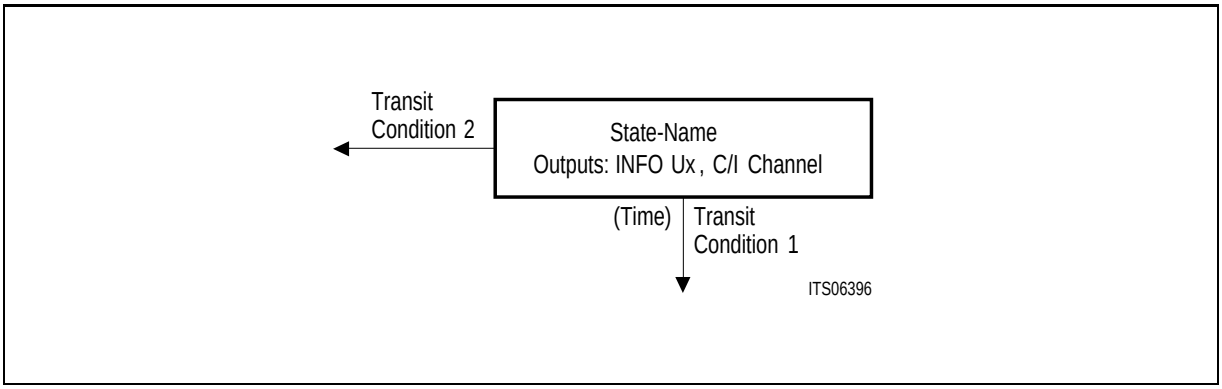


Figure 23
Example of a State with Outputs and Inputs

Each state has one or more exits to other states. These transitions depend on certain conditions which are noted next to the transition lines. These conditions are the only possibility to leave a state. If more conditions have to be fulfilled together, they are put into parentheses with an AND operator (&). If more than one condition leads to the same transition, they are put into parentheses with an OR operator (|). The meaning of a condition may be inverted by the NOT operator (/). Only the described states and transitions can exist.

Some conditions lead from each state to the same target state. To reduce the number of lines and the complexity of the figures, a state named “ANY STATE” exists standing for each state.

At some transitions, an internal timer is started. The time until the timer runs out, is noted in curly brackets { } next to the transition line. If the end of the started time leads to a transition from one state to another, this condition is indicated by TE (timer ended).

These actions are chosen to cope with all ISDN devices with IOM-2 standard interfaces. The states and transitions have been prepared to prevent undefined situations. In any case, the involved devices will enter defined conditions when the line is deactivated.

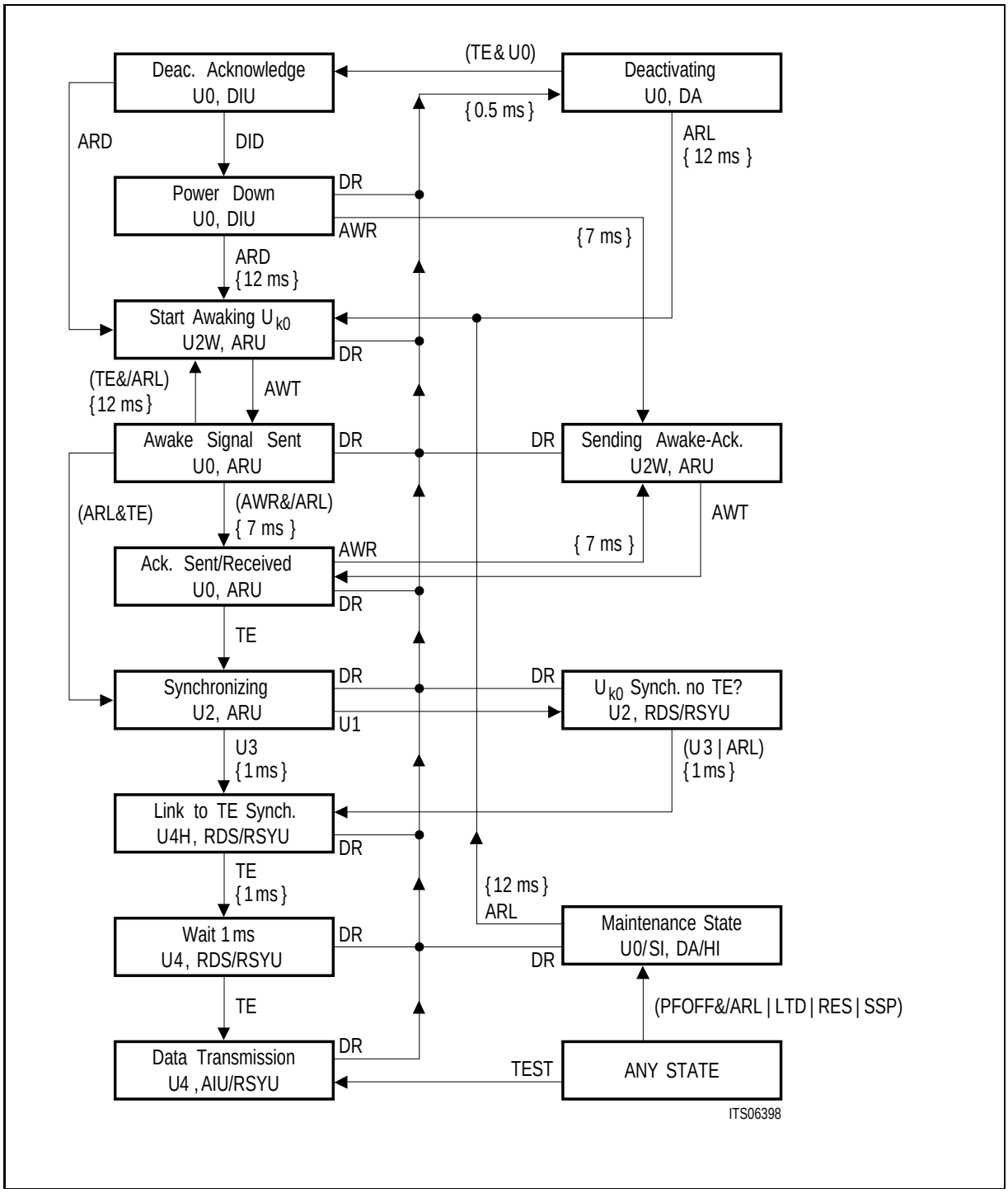


Figure 24
State Diagram of the LT

3.4.4.1 Transit Conditions and their Appreviations

In the following list, C/I-channel infos are omitted.

AWR	Awake signal (INFO U1W or U2W) detected
AWT	INFO U1W of U2W has been sent out
FRJ	Frame jump, detected by receive or transmit buffer, at least one IOM-2 frame (18 bit) is repeated or omitted caused by receive or transmit buffer over/ underflow
TE	Timer ended, the started timer has run out
U0	INFO U0 detected
U1	INFO U1 detected
U2	NFO U2 detected
U3	INFO U3 detected
U4H	INFO U4H detected

3.4.4.2 Control of the Analog Loop and Loop Commands on Uk0

The output of the Quad IEC DFE-T, e.g. infos on Uk0 or C/I-channel contents, usually depends only on the given state of the Quad IEC DFE-T control unit. In some states, several outputs are possible depending on input. If $\overline{\text{RES}}$ is not set to low or TSP isn't set to high, only the control of loops is state independent and is evaluated from the C/I-channel input.

ARL	causes the chip to be reset and the analog loop to be closed.
AR2	causes the M symbol continuously to be set to plus polarity in the LT.
AR4	causes the M symbol to be set to alternating plus and zero polarity in the LT

Any other C/I-channel input, low at $\overline{\text{RES}}$ or high at TSP, causes the analog loop to be opened and the M symbol to be set to zero.

3.4.4.3 Description of the Activation/Deactivation States of Quad IEC DFE-T

In this section, each state is described with its inputs, its outputs and its meaning. Unless described otherwise, the activation controller performs the following actions:

- No RESET of the Quad IEC DFE-T
- The adaption of receiver coefficients is disabled
- The RDS counter of frames with code violations is reset and disabled
- The received user data is given transparently to the IOM-2 interface
- The Quad IEC DFE-T is in power-up

The C/I-channel output and the transmitted Uk0 INFO are already specified by the state diagrams; below they are only referred to, if within a state there are more than one of them specified. In this case, the C/I-channel output and the transmitted Uk0 INFO depend on the given inputs.

Ack. sent/received	If awaking, the Quad IEC DFE-T has received the acknowledge signal. If being awoken the Quad IEC DFE-T has sent the acknowledged. Anyway, the Quad IEC DFE-T waits for possible repetition or time-out. The user data (B + B + D) on pin DOUT is clamped to high to avoid undesired false data in the D-channel during activation.
Awake signal sent	The Quad IEC DFE-T is awaking the Uk0 interface and waits for the acknowledge or for the time-out after sending the awake signal. The user data (B + B + D) on pin DOUT is clamped to high.
Deac. acknowledged	The Quad IEC DFE-T has received INFO U0, indicates this to the upstream unit and waits for DID, the permission to power down. The user data (B + B + D) on pin DOUT is clamped to high (except repeater modes).
Deact. request rec.	The Quad IEC DFE-T has received INFO U0 or one of the deactivating maintenance requests, RES or SSP. If it receives SSP, the Quad IEC DFE-T sends a single pulse every 1 ms on the line, otherwise INFO U0 is sent. The Quad IEC DFE-T remains at least 0.5 ms in this state before accepting DIU to be sure that it is already valid. The user date (B + B + D) on pin DOUT is clamped to high (except repeater modes).
Deactivating	The Quad IEC DFE-T deactivates Uk0 sending INFO U0; it remains at least 0.5 ms in this state to make sure that the associate device on IOM-2 has recognized a change from a possible DIU state to DA. The user data (B + B + D) on pin DOUT is clamped to high (except repeater modes).
Data transmission	The transmission of user data is enabled (INFO U4/U5). If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the Quad IEC DFE-T gives out RSYD or RSYU on the C/I-channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames. The RDS counter and the adaption of receiver coefficients are enabled even if RSYD/RSYU is given out.

Frame jump	In the transmit or in the receive data buffer a data over- or underflow has occurred. This is indicated to the associated layer 2 device with code FJ for 0.5 ms (4 IOM-2 frames). The RDS counter and the adaption of receiver coefficients are enabled.
IOM awaked	The LT in the exchange has received INFO U3 indicating that the link is synchronized from and to the TE. The LT commands, with 1 ms INFO U4H, the whole link to the TE to be switched transparent. The RDS counter and the adaption of receiver coefficients are enabled. If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the IECQuad DFE-T gives out RSYD or RSYU on the C/I-channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames.
Maintenance state	With SSP or LTD in the C/I-channel or with a low on pin $\overline{\text{RES}}$ as well as a high on pin TSP, the Quad IEC DFE-T goes to the maintenance state. The user data (B + B + D) on pin DOUT is clamped to high. If pins TSP and $\overline{\text{RES}}$ are high or code SSP is in the C/I-channel input, the Quad IEC DFE-T sends each ms a single pulse on the line to enable the test whether it fits into the specified pulse mask. IF pins $\overline{\text{RES}}$ and TSP are low or RES is in the C/I-channel input, the Quad IEC DFE-T is reset in this state erasing all stored coefficients. The Quad IEC DFE-T leaves the maintenance state only if TSP is low, $\overline{\text{RES}}$ is high and code DR or ARL is in the C/I-channel.
Power down	Entering this state, the Quad IEC DFE-T powers down within 0.5 ms stopping most parts of the Quad IEC DFE-T, so that these CMOS circuits cannot consume further energy. The IOM-2 interface units remain active as long as they are clocked via CL15 pin, and the user data (B + B + D) on pin DOUT is clamped to high .
Sending awake-ack	The Quad IEC DFE-T has received the awake signal and acknowledges this in this state. The user data (B + B + D) on pin DOUT is clamped to high.
Synchronized	The LT-RP has recognized INFO U1 or U3, so 1,152 subsequent bits have been transferred without any bit error. This indicates synchronization. Now the Quad IEC DFE-T itself is ready to go to the transparent state.

Synchronizing	After successful awake procedure, the IEC tries to recognize INFO U1, U2 or U3 (mode dependent). The user data (B + B + D) on pin DOUT is clamped to high.
Start awaking Uk0	Receiving ARU or ARD in the C/I-channel, the IEC has powered up and is sending the awake signal. The user data (B + B + D) on pin DOUT is clamped to high .
Uk0 synch. no TE?	The Quad IEC DFE-T in the exchange has recognized INFO U2, so 1,152 subsequent bits have been transferred without any bit error. This is an indication for synchronization of Uk0, but no terminal equipment has announced its presence yet. The Quad IEC DFE-T is now ready to go to the transparent state, if a TE was connected. From this state of activation, the RDS counter and the adaption of receiver coefficients are enabled until deactivation is performed. In case of an analog loop, the Quad IEC DFE-T leaves this state again at once. If no loop should be closed, the Quad IEC DFE-T waits for INFO U3 indicating that at least one TE is at the end of the link or for deactivation. If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the Quad IEC DFE-T gives out RSYD or RSYU on the C/I-channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames.
Wait 1 ms	Before indicating to the layer 2 device that the transparent state has been reached, the Quad IEC DFE-T in the exchange waits 1 ms to be sure that the whole link is already transparent upstream too. The user data (B + B + D) on pin DOUT is clamped to high . If in 64 subsequent Uk0 frames the Barker-code is not found at the expected position, the Quad IEC DFE-T gives out RSYD or RSYU on the C/I-channel until it has resynchronized finding the Barker-code on the same position in 4 subsequent frames.

4 Technical Description

4.1 General

The Uk0 interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

Separation of the transmitted and received signals is done by means of echo cancellation.

The following functions are transmitted over the twisted pair:

- Bidirectional:
  - B1, B2, D data channels
  - 120 kHz Symbol clock
  - 1 kHz Frame and 40 kHz block clock
  - Activation
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops
- From NT to LT side:
  - Indication of monitored code violations

On the Uk0 interface, transmission ranges of 4.2 km on wires of 0.4 mm diameter and 8 km on 0.6 mm wires are achieved without additional signal regeneration on the loop.

The transmission ranges can be doubled by inserting one repeater for signal regeneration.

4.2 Frame Structure of the Uk0 Interface

1 ms frames are transmitted via the Uk0 interface, each consisting of:

- 108 symbols: 144 bit scrambled and coded B + B + D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, resp. 36 bits) contains the user data of two IOM-2 frames in the same order (8B + 8B + 2D + 8B + 8B + 2D).

Different synchwords are used for each direction:

- Downstream from LT to NT+ + + – – – + – – + –
- Upstream from NT to LT– + – – + – – – +++

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

After successful synchronization, resynchronization will occur if the synchword is found to be consecutive 64 times in another position in the frame than the one expected after successful synchronization.The Quad IEC DFE-T is synchronized, if it detects the synchword four times consecutively with a period of 1 ms.

Table 9
Frame Structure for Downstream Transmission LT to NT

1 D_1	2 D_1	3 D_1	4 D_1	5 D_1	6 D_1	7 D_1	8 D_1	9 D_1	10 D_1	11 D_1	12 D_1
13 $D_{1/2}$	14 $D_{1/2}$	15 $D_{1/2}$	16 D_2	17 D_2	18 D_2	19 D_2	20 D_2	21 D_2	22 D_2	23 D_2	24 D_2
25 D_2	26 D_2	27 D_2	28 D_3	29 D_3	30 D_3	31 D_3	32 D_3	33 D_3	34 D_3	35 D_3	36 D_3
37 D_3	38 D_3	39 D_3	40 $D_{3/4}$	41 $D_{3/4}$	42 $D_{3/4}$	43 D_4	44 D_4	45 D_4	46 D_4	47 D_4	48 D_4
49 D_4	50 D_4	51 D_4	52 D_4	53 D_4	54 D_4	55 D_5	56 D_5	57 D_5	58 D_5	59 D_5	60 D_5
61 D_5	62 D_5	63 D_5	64 D_5	65 D_5	66 D_5	67 $D_{5/6}$	68 $D_{5/6}$	69 $D_{5/6}$	70 D_6	71 D_6	72 D_6
73 D_6	74 D_6	75 D_6	76 D_6	77 D_6	78 D_6	79 D_6	80 D_6	81 D_6	82 D_7	83 D_7	84 D_7
85 M	86 D_7	87 D_7	88 D_7	89 D_7	90 D_7	91 D_7	92 D_7	93 D_7	94 D_7	95 $D_{7/8}$	96 $D_{7/8}$
97 $D_{7/8}$	98 D_8	99 D_8	100 D_8	101 D_8	102 D_8	103 D_8	104 D_8	105 D_8	106 D_8	107 D_8	108 D_8
109 D_8	110 +	111 +	112 +	113 –	114 –	115 –	116 +	117 –	118 –	119 +	120 –

D_1 ... D_8 Ternary B + B + D data of IOM-2 frames 1 ... 8
M Maintenance symbol
+, – Synchword

Transparent access to the M bit is not possible via the IOM-2 interface.

U_1 ... U_8 Ternary B + B + D data of IOM-2 frames 1... 8

Table 10
Frame Structure for Upstream Transmission NT to LT

1 U_1	2 U_1	3 U_1	4 U_1	5 U_1	6 U_1	7 U_1	8 U_1	9 U_1	10 U_1	11 U_1	12 U_1
13 $U_{1/2}$	14 $U_{1/2}$	15 $U_{1/2}$	16 U_2	17 U_2	18 U_2	19 U_2	20 U_2	21 U_2	22 U_2	23 U_2	24 U_2
25 M	26 U_2	27 U_2	28 U_2	29 U_3	30 U_3	31 U_3	32 U_3	33 U_3	34 U_3	35 U_3	36 U_3
37 U_3	38 U_3	39 U_3	40 U_3	41 $U_{3/4}$	42 $U_{3/4}$	43 $U_{3/4}$	44 U_4	45 U_4	46 U_4	47 U_4	48 U_4
49 U_4	50 –	51 +	52 –	53 –	54 +	55 –	56 –	57 –	58 +	59 +	60 +
61 U_4	62 U_4	63 U_4	64 U_4	65 U_4	66 U_4	67 U_5	68 U_5	69 U_5	70 U_5	71 U_5	72 U_5
73 U_5	74 U_5	75 U_5	76 U_5	77 U_5	78 U_5	79 $U_{5/6}$	80 $U_{5/6}$	81 $U_{5/6}$	82 U_6	83 U_6	84 U_6
85 U_6	86 U_6	87 U_6	88 U_6	89 U_6	90 U_6	91 U_6	92 U_6	93 U_6	94 U_7	95 U_7	96 U_7
97 U_7	98 U_7	99 U_7	100 U_7	101 U_7	102 U_7	103 U_7	104 U_7	105 U_7	106 $U_{7/8}$	107 $U_{7/8}$	108 $U_{7/8}$
109 U_8	110 U_8	111 U_8	112 U_8	113 U_8	114 U_8	115 U_8	116 U_8	117 U_8	118 U_8	119 U_8	120 U_8

M Maintenance symbol

+, - Synchword

Transparent access to the M bit is not possible via the IOM-2 interface.

4.3 Coding from Binary to Ternary Data

Each 4 bit block of binary data is coded into 3 ternary symbols of MMS 43 block code according to **table 10**.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 11
MMS 43 Coding Table

				S1				S2				S3				S4			
t →				t →				t →				t →				t →			
0	0	0	1	0	–	+	1	0	–	+	2	0	–	+	3	0	–	+	4
0	1	1	1	–	0	+	1	–	0	+	2	–	0	+	3	–	0	+	4
0	1	0	0	–	+	0	1	–	+	0	2	–	+	0	3	–	+	0	4
0	0	1	0	+	–	0	1	+	–	0	2	+	–	0	3	+	–	0	4
1	0	1	1	+	0	–	1	+	0	–	2	+	0	–	3	+	0	–	4
1	1	1	0	0	+	–	1	0	+	–	2	0	+	–	3	0	+	–	4
1	0	0	1	+	–	+	2	+	–	+	3	+	–	+	4	–	–	–	1
0	0	1	1	0	0	+	2	0	0	+	3	0	0	+	4	–	–	0	2
1	1	0	1	0	+	0	2	0	+	0	3	0	+	0	4	–	0	–	2
1	0	0	0	+	0	0	2	+	0	0	3	+	0	0	4	0	–	–	2
0	1	1	0	–	+	+	2	–	+	+	3	–	–	+	2	–	–	+	3
1	0	1	0	+	+	–	2	+	+	–	3	+	–	–	2	+	–	–	3
1	1	1	1	+	+	0	3	0	0	–	1	0	0	–	2	0	0	–	3
0	0	0	0	+	0	+	3	0	–	0	1	0	–	0	2	0	–	0	3
0	1	0	1	0	+	+	3	–	0	0	1	–	0	0	2	–	0	0	3
1	1	0	0	+	+	+	4	–	+	–	1	–	+	–	2	–	+	–	3

4.4 Decoding from Ternary to Binary Data

Decoding is done in the reverse manner of coding. The received blocks of 3 ternary symbols are converted into blocks of 4 bits. The decoding algorithm is given in the following table.

As in the encoding table, the left hand symbol of each block (both binary and ternary) is the first bit and the right hand is the last. If a ternary block "0 0 0" is received, it is decoded to binary "0 0 0 0". This pattern usually occurs only during deactivation.

Table 12
4B3T Decoding Table

Ternary Block	Binary Block
0 0 0, + 0 +, 0 – 0	0 0 0 0
0 + –	0 0 0 1

Table 12
4B3T Decoding Table

+	–	0			0	0	1	0
0	0	+,	–	– 0	0	0	1	1
–	+	0			0	1	0	0
0	+	+,	–	0 0	0	1	0	1
–	+	+,	–	– +	0	1	1	0
–	0	+			0	1	1	1
+	0	0,	0	– –	1	0	0	0
+	–	+,	–	– –	1	0	0	1
+	+	–,	+	– –	1	0	1	0
+	0	–			1	0	1	1
+	+	+,	–	+ –	1	1	0	0
0	+	0,	–	0 –	1	1	0	1
0	+	–			1	1	1	0
+	+	0,	0	0 –	1	1	1	1

4.5 Monitoring of Code Violations

The RDS Monitor computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+ 1, 0, –1). At the end of each block, the running digital sum is the number of the next column in **table 11** which should contain the next received block. A code violation has occurred if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0, three user symbols with zero polarity, is found in the received data.

When, at the end of a ternary block, no error was found, the running digital sum is left at its current value for the next ternary block. If the counter value is greater than 4, it is set to 3 at the beginning of the next ternary block, if its value is 0 or less, it is set to one. So after a code violation has been detected, the RDS monitor synchronizes itself within a period depending on the received text.

Some transmission errors do not cause a code violation.

4.6 Scrambler

The binary transmit data from the IOM-2 interface is scrambled with a polynomial of 23 bits, before it is sent to the 4B3T coder. The scrambling algorithm ensures that no sequences of permanent binay 0s or 1s are transmitted. It is given in figure 10.

The scrambler contains supervision circuitry to avoid the case of continuous output (1 or 0). This case can occur during activation if, for example, each stored bit in the scrambler is equal to the continuous data input. In this case, at least one bit must be changed to gain the wanted pseudo random pattern.

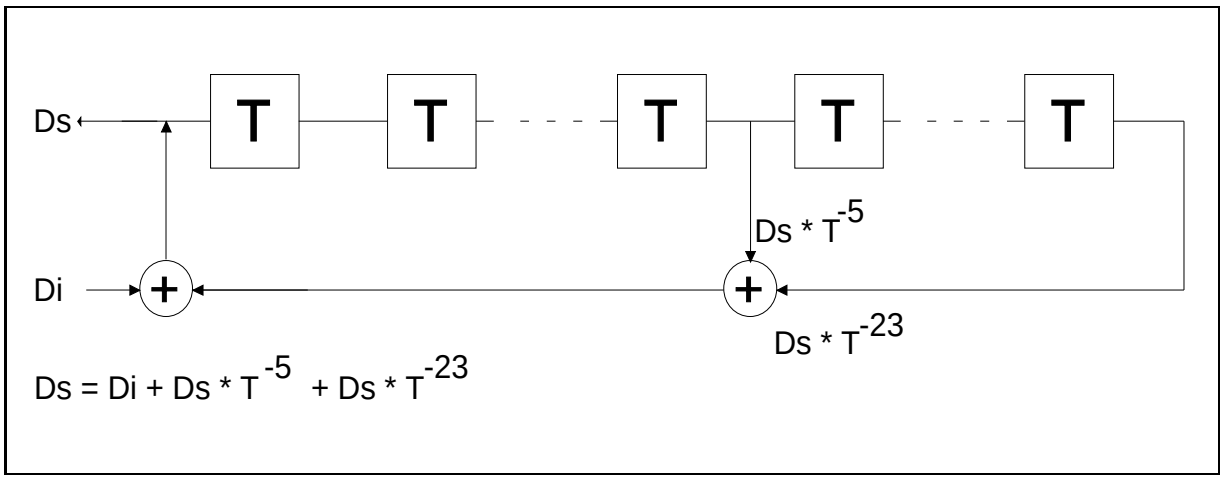


Figure 25
Scrambler

4.7 Descrambler

The received data (after decoding from ternary to binary) is multiplied with a polynomial of 23 bits in order to recover the original data before it is sent to the IOM-2 interface. The descrambler is self synchronized after 23 symbols. The descrambler polynomial is given in figure 25 and figure 28.

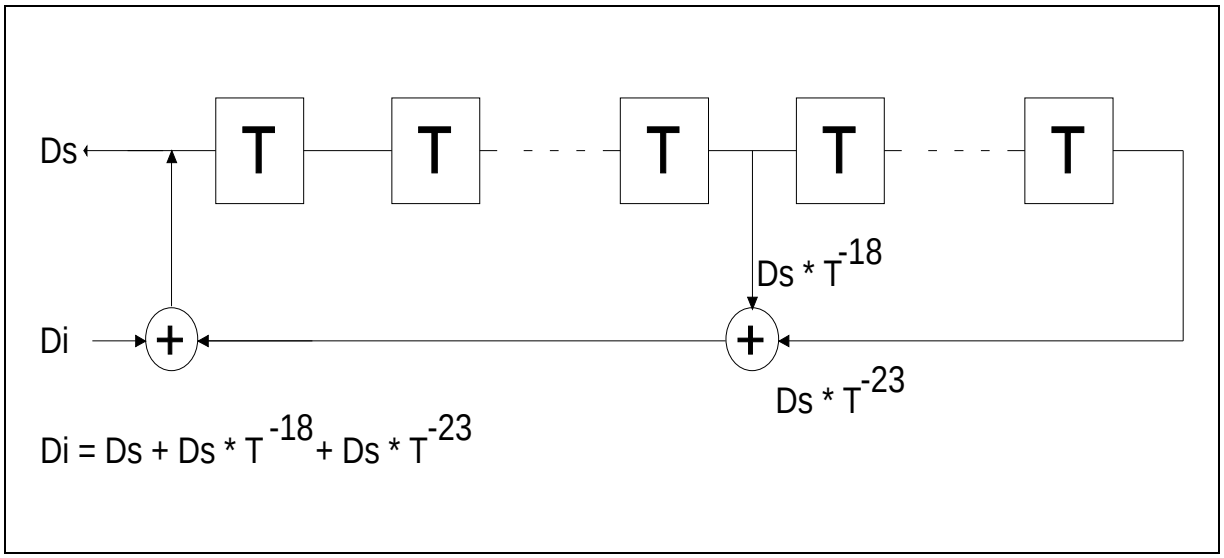


Figure 26
Descrambler in the LT without Local Loop Active

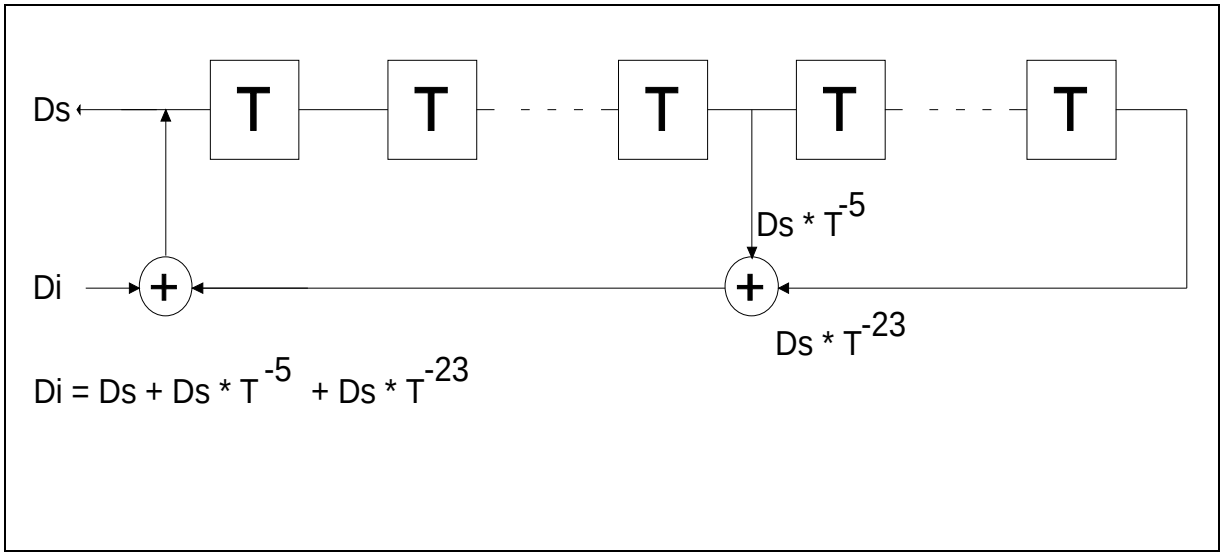


Figure 27
Descrambler with Local Loop Active

4.8 Signal Elements Used for Activation and Deactivation

Certain signal elements are used for activation and deactivation which cannot appear during normal operation. In this section, only the coding is described. For the meaning and usage of these signal elements see **section 3.4**.

Table 13
Coding of the Uk0-Signal Elements

Upstream from NT to LT	Downstream from LT to NT
INFO U1W: 16 times ternary + + + + + + + + – – – – – – – – A tone of: Frequency: 7.5 kHz Width: 2.13 ms	INFO U2W 16 times ternary + + + + + + + + – – – – – – – – A tone of: Frequency: 7.5 kHz Width: 2.13 ms
INFO U1A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code	INFO U2A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code
INFO U1: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)	INFO U2: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)
INFO U3: Binary continuous "1" before scrambling. Frame (Transmitting Barker code)	INFO U4H: Binary continuous "1" before scrambling with duration of 1 ms. Frame (Transmitting Barker code)
INFO U5: Binary data from the digital interface. Frame (Transmitting Barker code)	INFO U4: Binary data from the digital interface. Frame (Transmitting Barker code)
INFO U0: Ternary continuous "0" No frame, no signal level	INFO U0: Ternary continuous "0" No frame, no signal level

4.9 Detection of INFO U0, U1, U2, U3 and U4H

The Quad IEC DFE-T detects an INFO U1, U2 or U3 if the continuous binary data is found on the descrambler output after 8 subsequent Uk0 frames. These INFOs are detected after 8 to 9 ms.

INFO U4H is recognized if the NT finds 16 subsequent binary 1s in the data stream.

INFO U0 is recognized if the Quad IEC DFE-T finds one complete frame with continuous zero level.

4.10 Awake Signal Detection

To activate the Uk0 interface, special awake and acknowledge signals (INFO U1W and U2W) are defined. The activating Quad IEC DFE-T sends out a 7.5 kHz tone of 2.133 ms duration, which has to be detected by the IEC on the other end of the line, which then acknowledges it with the same 7.5 kHz tone of 2.133 ms duration.

The awake/acknowledge signal is generated like each signal on the U link, but neither 4B3T coded data nor frames are transmitted. The awake/acknowledge signal is a series of 16 periods. Each of them is generated by subsequent 8 plus-level and 8 minus-level ternary symbols with the usual 120 kBaud symbol rate. During normal transmission no such symbol sequence can occur.

A special awake unit is implemented in the Quad IEC DFE-T. After detecting a wake-up signal, the control procedures are started (**see section 3.4**).

The line signal is evaluated by checking for level, frequency and duration. To be recognized as valid, the wake-up signal has to exceed a threshold level of 25 - 80 mV at the line side of the transformer, and its frequency has to be between 6.15 kHz as lower limit and 8.27 - 8.89 kHz as higher limit. After detecting 14 subsequent rising edges on the line within the frequency range, the Quad IEC DFE-T waits until no two subsequent falling edges occur within a period of 0.39 ms which could belong to an awake signal. This happens usually after the 16th edge when only some attenuated oscillations may occur.

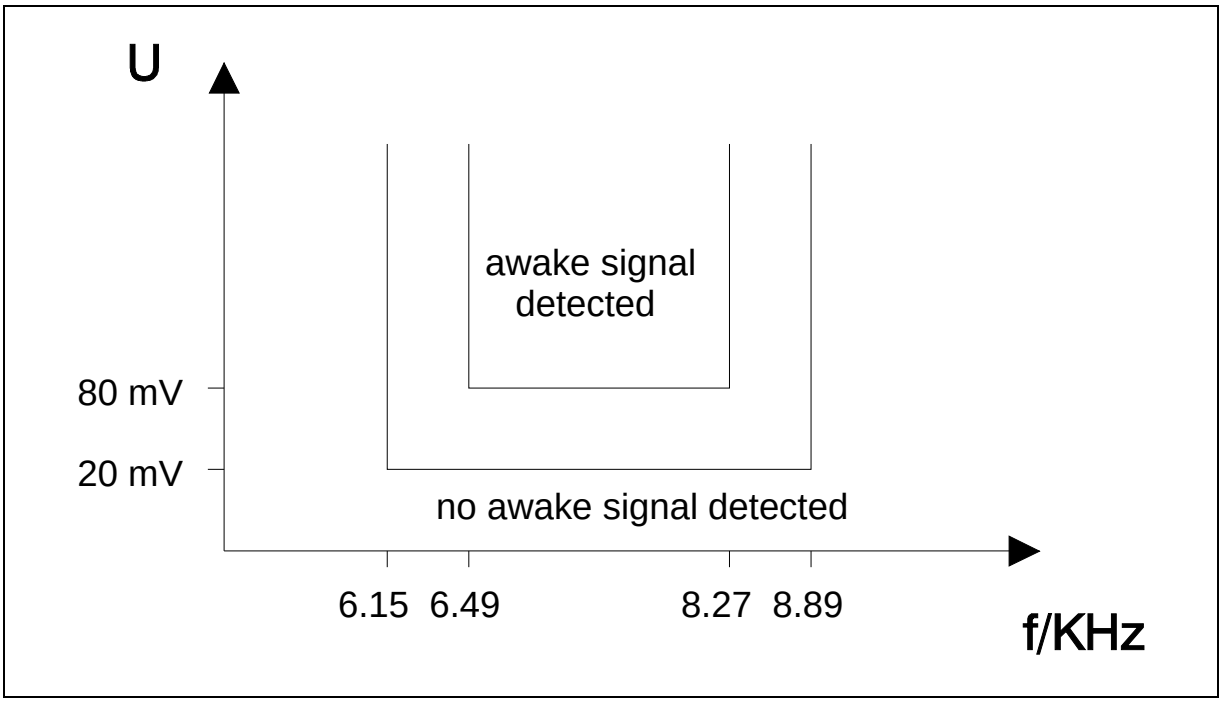


Figure 28:
Level and Frequency for Awake Signal Recognition

5 Electrical Characteristics

Unless otherwise specified, the static and dynamic limits apply over a supply voltage range from 4.75 to 5.25 V and over the temperature range as specified in **section 6.2**.

5.1 Static Requirements

Table 14
Static Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High level input voltage	V_{IH}	2.4		V_{DD} + 0.3	V	
Low level input voltage	V_{IL}	– 0.3		0.8	V	
Low level input leakage current	V_{IL}	– 1			µA	V_{IN} = GND
High level input leakage current	I_{IH}			1	µA	V_{IN} = VDD
High level output voltage	V_{OH}	4.0			V	tbd
Low level output voltage	V_{OL}			0.33	V	tbd
Input capacitance	C_{IN}			10	pF	

5.2 Dynamic Requirements

preliminary values

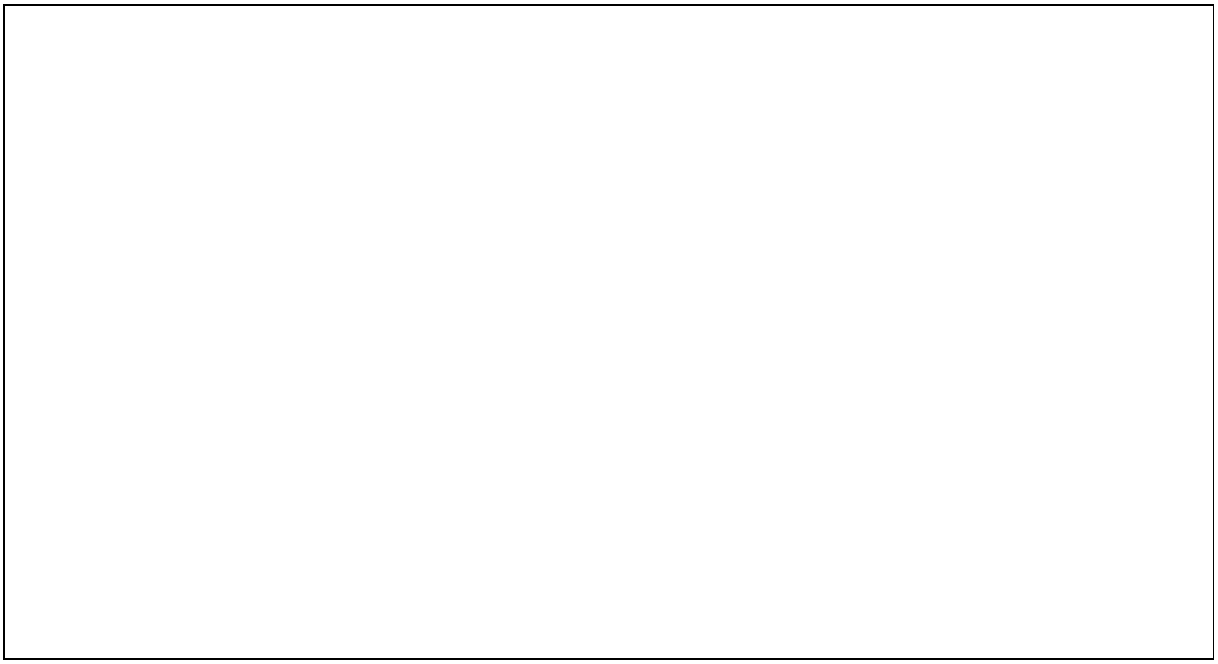


Figure 29:
Dynamic Requirements (t.b.d)

Table 15
Dynamic Input Characteristics

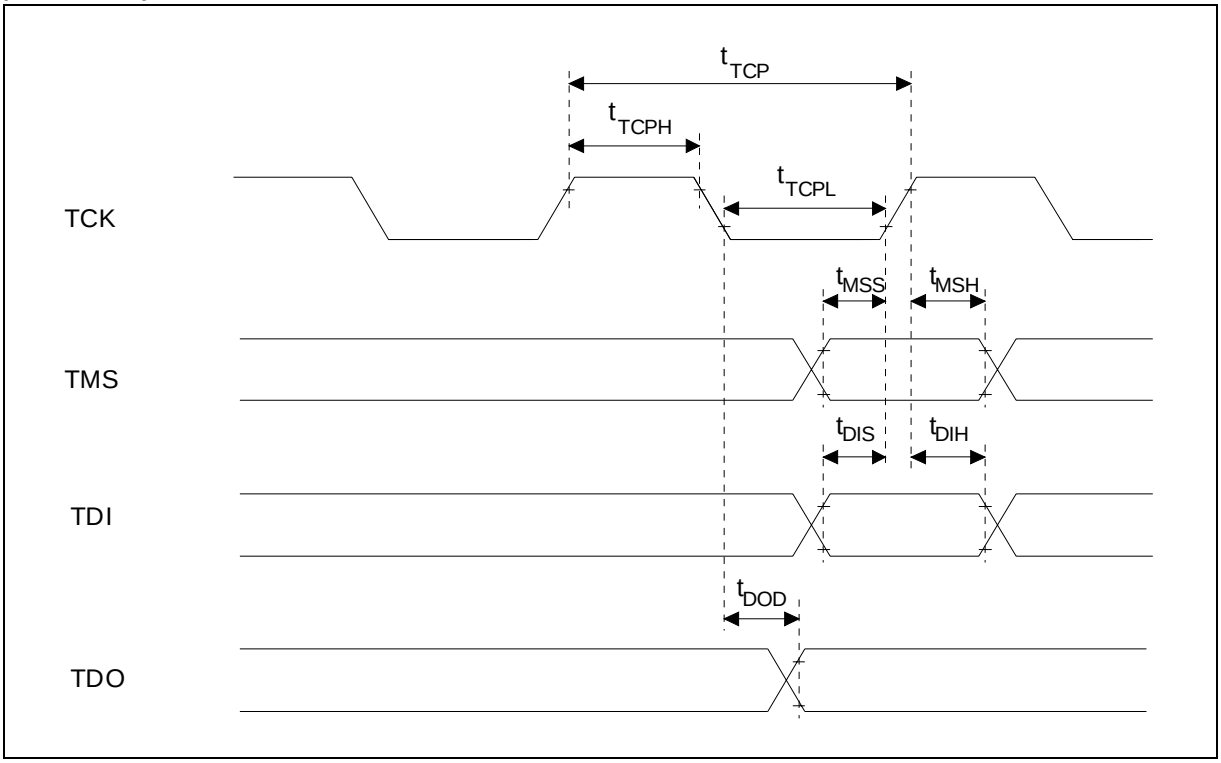
Parameter	Signal	Symbol	Limit Values			Unit
			min.	typ.	max.	
Clock rise / fall time	CL15	t_r, t_f			15	ns
Clock period	CL15	T_{cw}		65		ns
Pulse width high / low	CL15	t_h t_l	20 20			ns ns
Data rise / fall time		t_r, t_f		t.b.d		ns
Data setup		t_{ds}		t.b.d		ns
Data hold		t_{dh}		t.b.d		ns

Table 16
Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
t.b.d							

5.3 Boundary Scan Timing

preliminary values



Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns

Parameter	Symbol	Limit Values		Unit
		min.	max.	
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

5.4 Power Supply

5.4.1 Supply Voltages

VDD to GND = +5V ±0,25V

5.4.2 Power Consumption

All measurements with random 2B+D data in active states, 5V (0°C - 70°C)

Table 17
Power Consumption

Parameter	Symbol	Limit Values			Unit	Comment
		min.	typ.	max.		
			t.b.d		mW	all line ports are in power up
			t.b.d		mW	all line ports are in power-down

5.5 Maximum ratings

Stresses above those listed in **table 17** may cause permanent damage to the device. Exposure to conditions beyond those indicated in **section 5.4.1** of this specification may affect device reliability.

This is a stress rating only and functional operation of the device under these conditions or at any other condition beyond those indicated in the operational conditions of this

specification is not implied. It is not implied, that more than one of these conditions can be applied simultaneously.

Table 18
Maximum ratings

Parameter	Limit Values		Unit
	min.	max.	
positive Supply Voltage		7.0	V
Voltage applied at any input	-0.3	VDD + 0.3 max. 7.0	V
Voltage applied at any output	-0.3	VDD + 0.3 max. 7.0	V
Voltage between GNDx to any other GNDx		0.3	V
Voltage between VDDx to any other VDDx		0.3	V

6 Environmental Requirements

6.1 Storage and Transportation

The rated (limited capability) storage and transportation temperature range prior to printed board assembly shall be as follows:

- 65 to +150°C (without supply voltage)

6.2 Operating Ambient

The operating ambient temperature for standard and extended temperature versions shall be within the limits as follows:

0 °C to +70 °C (standard version)

– 40 °C to +85 °C (extended temperature range version)