ispPAC®-POWR1208P1

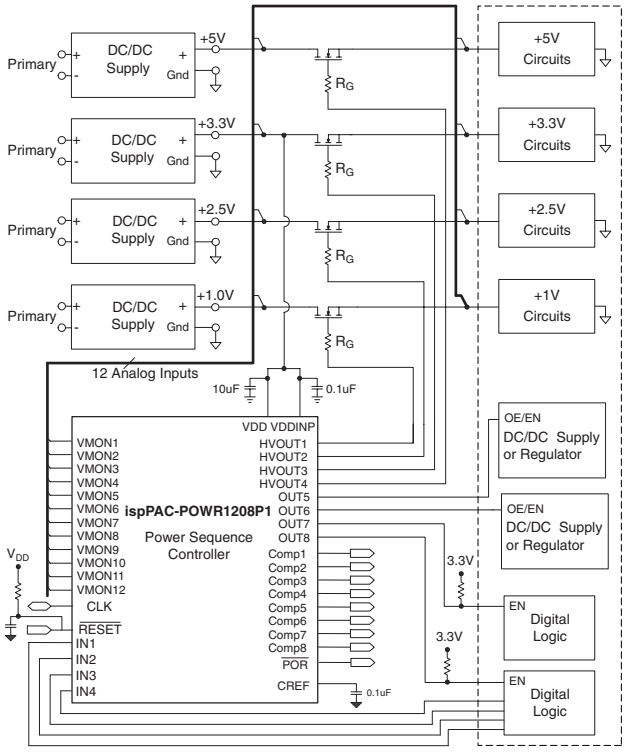
In-System Programmable Power Supply Sequencing Controller and Precision Monitor

February 2005 **Data Sheet**

Features

- **Monitor and Control Multiple Power Supplies**
  - Simultaneously monitors up to 12 power supplies
  - Sequence controller for power-up conditions
  - Provides eight output control signals
  - Programmable digital and analog circuitry
- **Precision Analog Comparators for Monitoring**
  - 12 analog comparators for monitoring
  - 384 programmable threshold levels spanning 0.68V to 5.93V
  - 0.5% precision
  - Other user-defined voltages possible
  - 80mV near-ground threshold for power-off detect
  - Each comparator independently configurable
  - Eight direct comparator outputs
  - Digital filter on comparator outputs
- **Embedded PLD for Sequence Control**
  - Implements state machine and input conditional events
  - In-System Programmable (ISP™) through JTAG and on-chip E²CMOS®
  - Input synchronizers
- **Embedded Programmable Timers**
  - 4 Programmable 8-bit timers (32µs to 524ms)
  - Programmable time delay between multiple power supply ramp-up and wait statements
- **Embedded Oscillator**
  - Built-in clock generator, 1MHz
  - Programmable clock frequency
  - Programmable timer pre-scaler
  - External clock support
- **Programmable Output Configurations**
  - Four digital outputs for logic and power supply control
  - Four fully programmable gate driver outputs for FET control, or programmable as four additional digital outputs
  - Expandable with ispMACH™ 4000 CPLD
- **2.7V to 5.5V Supply Range**
  - In-system programmable at 3.0V to 5.5V
  - Industrial temperature range: -40°C to +85°C
  - 44-pin TQFP package

Application Block Diagram



Description

The Lattice ispPAC-POWR1208P1 incorporates both in-system programmable logic and in-system programmable analog circuits to perform special functions for power supply sequencing and monitoring. The ispPAC-POWR1208P1 device has the capability to be configured through software to control up to eight outputs for power supply sequencing and 12 comparators monitoring supply voltage limits, along with four digital inputs for interfacing to other control circuits or digital logic. Once configured, the design is downloaded into the device through a standard JTAG interface. The circuit configuration and routing are stored in non-volatile E²CMOS. PAC-Designer,® an easy-to-use Windows-compatible software package gives users the ability to design and simulate logic and sequences that control the power supplies or FET driver circuits. The user has control over timing functions, programmable logic functions and comparator threshold values as well as I/O configurations.

Power Supply Sequence Controller and Monitor

The ispPAC-POWR1208P1 device is specifically designed as a fully-programmable power supply sequencing controller and monitor for managing up to eight separate power supplies, as well as monitoring up to 12 analog inputs or supplies. The ispPAC-POWR1208P1 device contains an internal PLD that is programmable by the user to implement digital logic functions and control state machines. The internal PLD connects to four programmable timers, special purpose I/O and the programmable monitoring circuit blocks. The internal PLD and timers can be clocked by either an internal programmable clock oscillator or an external clock source.

The voltage monitors are arranged as 12 independent comparators, each with 384 programmable trip-point settings ranging from 0.68V to 5.392V in roughly 0.5% steps. An additional low-voltage threshold (80mV) is also provided for sensing power-off conditions.

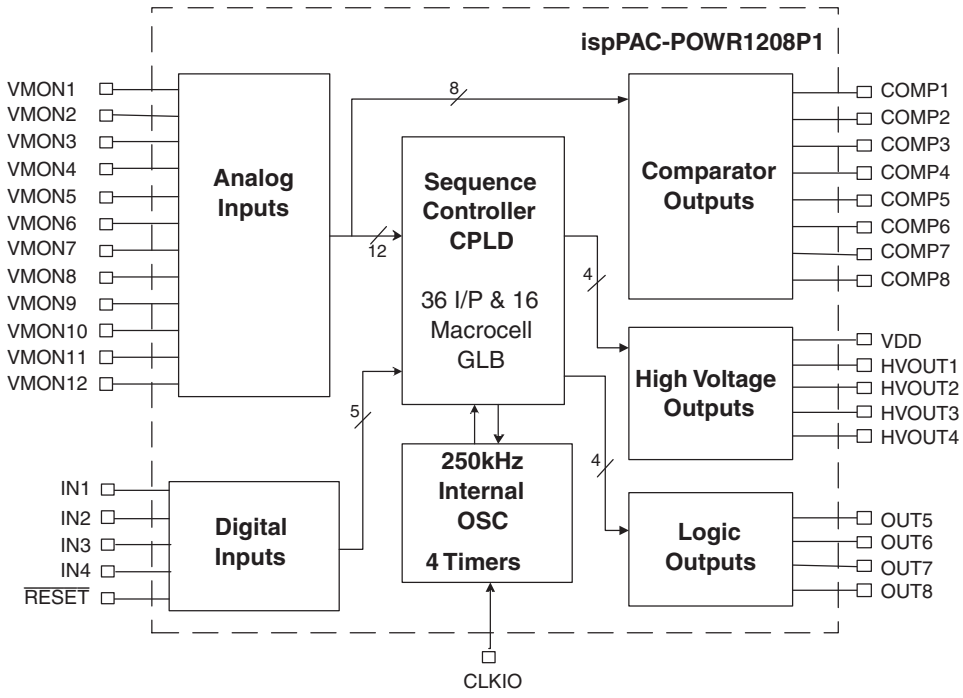
The voltage monitors incorporate two features designed to increase their robustness. The first is a small amount of hysteresis. In general, more hysteresis implies more noise immunity, but as trip-points decrease a fixed amount of hysteresis would adversely affect the trip-point accuracy. For this reason the ispPAC-POWR1208P1's voltage monitors use a scheme in which hysteresis scales with trip-point voltages remaining at a nearly constant 0.5% of the selected trip-point. Hysteresis is 30mV for a 5.932V trip-point and scales down to 4mV for a 0.68V trip-point.

The second feature that increases the voltage monitor's robustness are a synchronizer and digital filter in each monitor circuit. The filter may be optionally enabled to provide higher noise immunity at the cost of a somewhat increased response time.

The programmable logic functions consist of a block of 36 inputs with 81 product terms and 16 macrocells. The architecture supports the steering of product terms to enhance the overall usability.

Output pins are configurable in two different modes. There are eight outputs for controlling eight different power supplies. OUT5-OUT8 are open-drain outputs for interfacing to other circuits. The HVOUT1-HVOUT4 pins can be programmed individually as open-drain outputs or as high voltage FET gate drivers. As high voltage FET gate driver outputs, they can be used to drive an external N-Channel MOSFET as a switch to control the voltage ramp-up of the target board. The four HVOUT drivers have programmable current and voltage levels.

Figure 1. ispPAC-POWR1208P1 Block Diagram



Pin Descriptions

Number	Name	Pin Type	Description
1	HVOUT4	O/D Output	Open-drain Output 4
		Current Source	FET Gate Driver 4
2	HVOUT3	O/D Output	Open-drain Output 3
		Current Source	FET Gate Driver 3
3	HVOUT2	O/D Output	Open-drain Output 2
		Current Source	FET Gate Driver 2
4	HVOUT1	O/D Output	Open-drain Output 1
		Current Source	FET Gate Driver 1
5	VDD	Power	Main Power Supply
6	IN1	CMOS Input	Input 1, Schmitt-Trigger Input
7	IN2	CMOS Input	Input 2, Schmitt-Trigger Input
8	IN3	CMOS Input	Input 3, Schmitt-Trigger Input
9	IN4	CMOS Input	Input 4, Schmitt-Trigger Input
10	$\overline{\text{RESET}}$	CMOS input[1]	PLD Reset Input, Active Low, Schmitt-Trigger Input
11	VDDINP	Power[2]	Digital Inputs Power Supply
12	OUT5	O/D Output	Open-Drain Output
13	OUT6	O/D Output	Open-Drain Output
14	OUT7	O/D Output	Open-Drain Output
15	OUT8	O/D Output	Open-Drain Output
16	COMP8	O/D Output	VMON8 Comparator Output (Open-Drain)
17	COMP7	O/D Output	VMON7 Comparator Output (Open-Drain)
18	COMP6	O/D Output	VMON6 Comparator Output (Open-Drain)
19	COMP5	O/D Output	VMON5 Comparator Output (Open-Drain)
20	COMP4	O/D Output	VMON4 Comparator Output (Open-Drain)
21	COMP3	O/D Output	VMON3 Comparator Output (Open-Drain)
22	COMP2	O/D Output	VMON2 Comparator Output (Open-Drain)
23	COMP1	O/D Output	VMON1 Comparator Output (Open-Drain)
24	TCK	TTL/LVCMOS Input	Test Clock (JTAG Pin)
25	$\overline{\text{POR}}$	O/D Output	Power-On-Reset Output
26	CLK	Bi-directional I/O[3]	Clock Output (Open-Drain) or Clock Input
27	GND	Ground	Ground
28	TDO	TTL/LVCMOS Output	Test Data Out (JTAG Pin)
29	$\overline{\text{TRST}}$	TTL/LVCMOS Input	Test Reset, Active Low, 50k Ohm Internal Pull-up (JTAG Pin, Optional Use)
30	TDI	TTL/LVCMOS Input	Test Data In, 50k Ohm Internal Pull-up (JTAG Pin)
31	TMS	TTL/LVCMOS Input	Test Mode Select, 50k Ohm Internal pull-up (JTAG Pin)
32	VMON1	Analog Input	Voltage Monitor Input 1
33	VMON2	Analog Input	Voltage Monitor Input 2
34	VMON3	Analog Input	Voltage Monitor Input 3
35	VMON4	Analog Input	Voltage Monitor Input 4
36	VMON5	Analog Input	Voltage Monitor Input 5
37	VMON6	Analog Input	Voltage Monitor Input 6
38	VMON7	Analog Input	Voltage Monitor Input 7

Pin Descriptions (Continued)

Number	Name	Pin Type	Description
39	CREF	Reference[4]	Reference for Internal Use, Decoupling Capacitor (.1uf Required, CREF to GND)
40	VMON8	Analog Input	Voltage Monitor Input 8
41	VMON9	Analog Input	Voltage Monitor Input 9
42	VMON10	Analog Input	Voltage Monitor Input 10
43	VMON11	Analog Input	Voltage Monitor Input 11
44	VMON12	Analog Input	Voltage Monitor Input 12

1. $\overline{\text{RESET}}$ is an active low INPUT pin, external pull-up resistor to V_{DD} is required. When driven low it resets all internal PLD flip-flops to zero, and may turn "ON" or "OFF" the output pins, including the HVOUT pins depending on the polarity configuration of the outputs in the PLD. If a reset function is needed for the other devices on the board, the PLD inputs and outputs can be used to generate these signals. The $\overline{\text{RESET}}$ should be used if multiple ispPAC-POWR1208P1 devices are cascaded together in expansion mode.
2. V_{DDINP} can be chosen independent of V_{DD}. It is used to set the logic threshold only to the four logic inputs IN1-IN4.
3. CLK is the PLD clock output in master mode. It is re-routed as an input in slave mode. The clock mode is set in software during design time. In output mode it is an open-drain type pin and requires an external pull-up resistor. Multiple ispPAC-POWR1208P1 devices can be tied together with one acting as the master, the master can use the internal clock and the slave can be clocked by the master. The slave needs to be set up using the clock as an input.
4. The CREF pin requires a 0.1µF capacitor to ground, near the device pin. This reference is used internally by the device. No additional external circuitry should be connected to this pin.

Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below. Stresses beyond these listed values may cause permanent damage to the device. Functional operation of the device at these or any other conditions outside those indicated in the operating sections of this specification is not implied.

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{DD}	Core supply voltage at pin	—	-0.5	6.0	V
V_{DDINP}[1]	Digital input supply voltage for IN1-IN4	—	-0.5	6.0	V
HVOUTmax	HVOUT pin voltage, max = V_{DD} + 9V	—	-0.5	15	V
V_{IN}[2]	Input voltage applied, digital inputs	—	-0.5	6.0	V
VMON	Input voltage applied, V_{MON} voltage monitor inputs	—	-0.5	7.0	V
V_{TRI}	Tristated or open drain output, external voltage applied (CLK pin 26 pull-up ≤ V_{DD}).	—	-0.5	6.0	V
T_S	Storage temperature	—	-65	150	°C
T_A	Ambient temperature with power applied	—	-55	125	°C
T_{SOL}	Maximum soldering temperature (10 sec. at 1/16 in.)	—	—	260	°C

1. V_{DDINP} is the supply pin that controls logic inputs IN1-IN4 only. Place 0.1µF capacitor to ground and supply the V_{DDINP} pin with appropriate supply voltage for the given input logic range.
2. Digital inputs are tolerant up to 5.5V, independent of the V_{DDINP} voltage.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{DD}	Core supply voltage at pin		2.7	5.5	V
V_{DDPROG}	Core supply voltage at pin	During E^2 cell programming	3.0	5.5	V
V_{DDINP}[1]	Digital input supply voltage for IN1-IN4		2.25	5.5	V
V_{IN}[2]	Input voltage digital inputs		0	5.5	V
V_{MON}	Voltage monitor inputs V_{MON1} - V_{MON12}		0	6.0	V
Erase/Program Cycles		EEPROM, programmed at V_{DD} = 3.0V to 5.5V	1000	—	Cycles
T_{APROG}	Ambient temperature during programming		-40	+85	°C
T_A	Ambient temperature	Power applied	-40	+85	°C

1. V_{DDINP} is the supply pin that controls logic inputs IN1-IN4 only. Place 0.1µF capacitor to ground and supply the V_{DDINP} pin with appropriate supply voltage for the given input logic range.
2. Digital inputs are tolerant up to 5.5V, independent of the V_{DDINP} voltage.

Analog Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{DD}	V_{DD} Supply Current	Internal Clock = 1MHz	—	10	20	mA
I_{DDINP}	V_{DDINP} Supply Current		—	5	20	µA

Reference

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{REF}[1]	Reference voltage at CREF pin	T = 25°C	—	1.16	—	V

1. CREF pin requires a 0.1µF capacitor to ground.

Voltage Monitors

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{IN}	Input impedance		70	100	130	kΩ
V_{MON} Range	Programmable voltage monitor trip point (384 steps)		0.680		5.932	V
V_{MON} Accuracy	Absolute accuracy of any trip point[2]	T = 25 °C, V_{DD} = 3.3V $V_{MON} \leq$ 1.8V	-0.5		+0.5	%
		T = 25 °C, V_{DD} = 3.3V V_{MON} > 1.8V	-0.6		+0.6	%
V_{MON} Tempco[1]	Temperature drift of any trip point	-40°C to +85°C		30		ppm/ °C
V_{HYST}	Hysteresis of V_{MON} input	V_{DD} = 3.3V		0.5% of trip point setting		%
V_{MONLO}	Near-ground sense threshold	T = 25 °C, V_{DD} = 3.3V	70	80	90	mV
PSR	Trip point sensitivity to V_{DD}	V_{DD} = 3.3V		0.07		%/V

1. See Performance Graphs section.
2. Guaranteed by characterization.

High Voltage FET Drivers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP} Range	Programmable gate driver voltage (eight steps)	(Note 1)	8	—	12	V
V_{PP} Accuracy	Absolute accuracy of V_{PP} output voltage	25°C	-10	—	10	%
V_{PP} Step	Gate driver voltage step	(Note 2)	—	0.5	—	V
I_{SOURCE} Range	Programmable I_{SOURCE} current (32 steps)		0.5	—	50	µA
I_{SOURCE} Accuracy	Absolute accuracy of I_{SOURCE} current		—	10	—	%
I_{STEP}	Relative current value, from any I_{SOURCE} setting to the next		—	15	—	%
R_{SINK}	Gate driver sink/discharge resistor when setting FET driver to a LOW state	FET Driver in OFF state	—	8	—	kΩ

1. Maximum voltage of V_{PP} is not to exceed 7.5V over V_{DD}.
2. The high voltage driver outputs are set in software, HVOUT voltage range is between 8V and 12V. V_{DD} values determine the maximum V_{PP}.

Power-On-Reset

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{LPOR}[3]	V_{DD} supply threshold above which $\overline{POR}$ output is guaranteed to be driven low	V_{DD} ramping up[1]	—	—	1.15	V
V_{HPOR}[3]	V_{DD} supply threshold above which $\overline{POR}$ output is guaranteed driven high, and device initializes	V_{DD} ramping up[1]	—	—	2.1	V
t_{DPOR}	$\overline{POR}$ delay[2]	V_{DD} ramping up to 3.3V in <10µs C_{REF} = 0.1µF	—	3	—	ms
V_{RESET}	V_{DD} supply threshold below which will trigger a reset cycle from the “ON’ state.	VDD ramping down[1]	1.8	—	2.1	V

1. POR tests run with 10kΩ resistor pulled up to V_{DD}.
2. 1MHz clock must be present.
3. Hysteresis = 50mV.

AC/Transient Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
Voltage Monitors						
t_{PDMON}	Propagation Delay. Output transitions after a step input, from V_{MON} to comparator output	Glitch filter OFF.[1] Input V_{TRIP} + 100mV to V_{TRIP} - 100mV	—	4	7	µs
		Glitch filter ON.[1] Input V_{TRIP} + 100mV to V_{TRIP} - 100mV	28	32	35	µs
Oscillators						
f_{CLK}	Internal Master Clock frequency		0.8	1	1.2	MHz
PLDCLKext	Frequency range of applied external clock source	External clock applied	0.8	—	1.2	MHz
PLDCLK Range	Programmable frequency range of PLD clock (8 binary steps)	(Note 1)	1.95	—	250	kHz
Timers						
Timeout Range	Range of programmable time-out duration (15 steps)	(Note 1)	0.03	—	524	ms

1. Assumes 1MHz clock.

Digital Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}	Input or I/O leakage current, no pull-up	$0V \le V_{IN} \le V_{DDINP}$ or V_{DD} 25 °C			+/-10	µA
I_{PU}	Input pull-up current (TMS, TDI, $\overline{TRST}$)	25 °C		70		µA
V_{OL}	Output Low Voltage [OUT5-OUT8] [COMP1-COMP8] [HVOUT1-HVOUT4]	$I_{SINKOUT}$ = 4mA			0.4	V
$I_{SINKHVOUT}$	Maximum sink current for HVOUT pins in open-drain mode [HVOUT1-HVOUT4]	(Note 1)			10	mA
$I_{SINKOUT}$	Maximum sink current for logic outputs [OUT5-OUT8], [COMP1-COMP8]	(Note 1)			20	mA
$I_{SINKTOTAL}$	Total combined sink currents from all outputs [OUT, HVOUT, COMP]	(Note 1)			80	mA

1. [OUT5-OUT8] and [COMP1-COMP8] can sink up to 20mA max. per pin for LEDs, etc. However, output voltage levels may exceed V_{OL}. Total combined sink currents from all outputs (OUT, HVOUT, COMP) should not exceed $I_{SINKTOTAL}$.

DC Input Levels: IN1-IN4

Symbol	Parameter	Min.	Max.	Units
V_{IL}	Schmitt trigger input low voltage	-0.3	0.25 x V_{DDINP}	V
V_{IH}	Schmitt trigger input high voltage	0.75 x V_{DDINP}	5.5	V

Note: V_{DDINP} is the input supply pin for IN1-IN4 digital logic input pins. These pins' Schmitt-Trigger thresholds are dependent on the voltage at V_{DDINP}.

Timing Characteristics

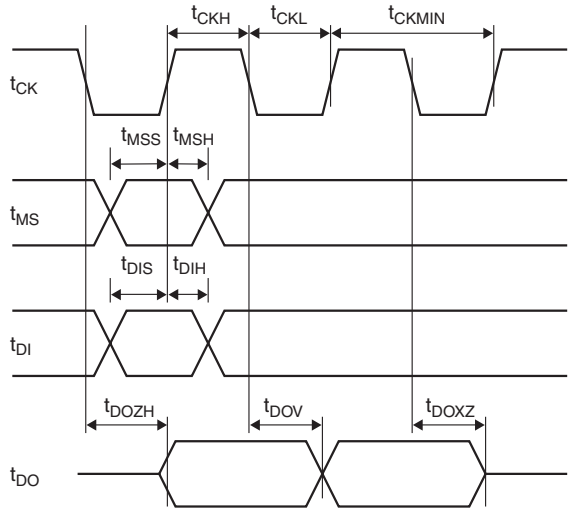
Over Recommended Operating Conditions

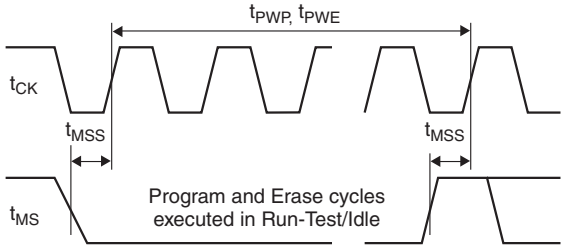
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PLD Timing						
t_{PD}	Combinatorial propagation delay from INx input to OUTx output.				150	ns
t_{RST}	$\overline{\text{RESET}}$ pulse width		25			µs

Timing for JTAG Operations

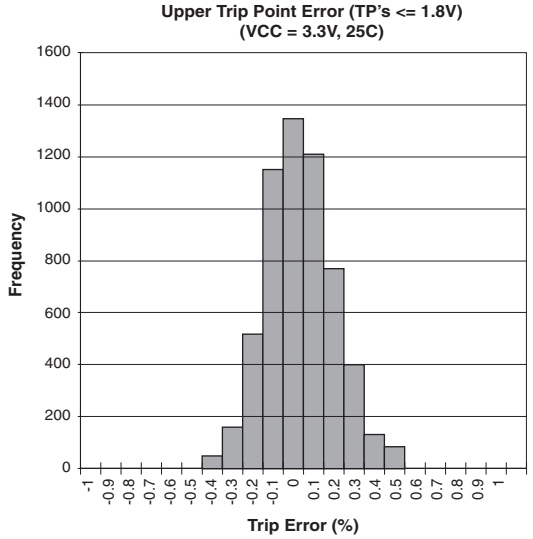
Symbol	Parameter	Conditions	Min	Typ.	Max	Units
t_{CKMIN}	Minimum clock period		1			µs
t_{CKH}	TCK high time		200			ns
t_{CKL}	TCK low time		200			ns
t_{MSS}	TMS setup time		15			ns
t_{MSH}	TMS hold time		50			ns
t_{DIS}	TDI setup time		15			ns
t_{DIH}	TDI hold time		50			ns
t_{DOZX}	TDO float to valid delay				200	ns
t_{DOV}	TDO valid delay				200	ns
t_{DOXZ}	TDO valid to float delay				200	ns
t_{RSTMIN}	Minimum reset pulse width		40			ns
t_{PWP}	Time for a programming operation[1]		40		100	ms
t_{PWE}	Time for an erase operation		40		100	ms

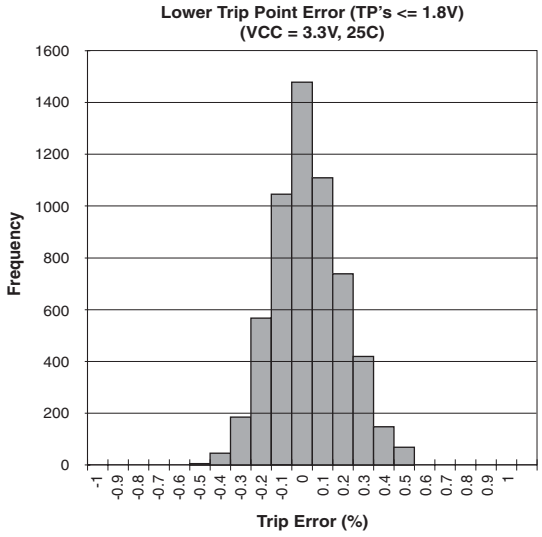
1. t_{PWP} represents programming pulse width for a single row of E^2CMOS cells.

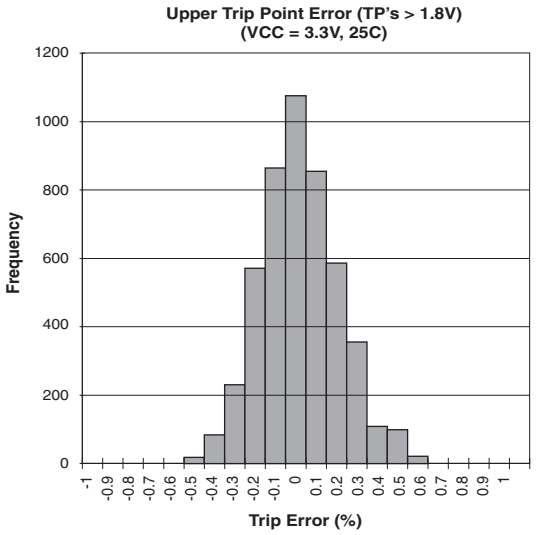


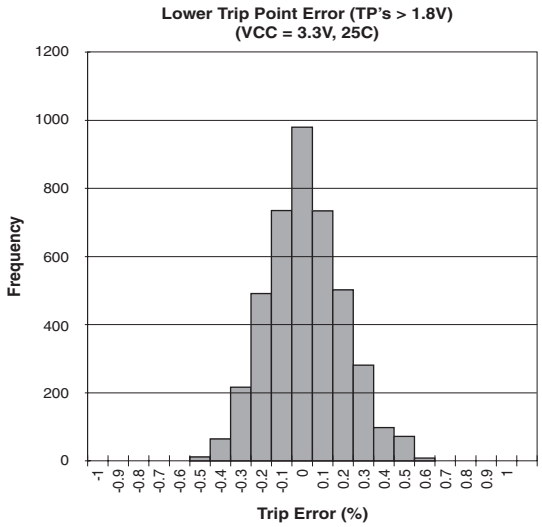


Performance Graphs









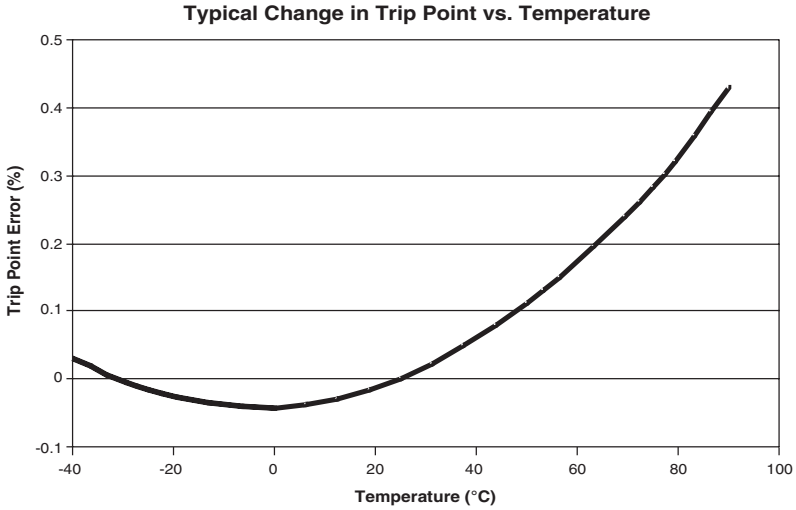


Table 1. V_{MON} Trip Points

	1	2	3	4	5	6	7	8	9	10	11	12
0	0.680	0.808	0.962	1.142	1.363	1.618	1.931	2.289	2.724	3.241	4.221	5.017
1	0.684	0.812	0.968	1.149	1.371	1.628	1.942	2.302	2.741	3.260	4.246	5.046
2	0.688	0.817	0.974	1.156	1.378	1.637	1.954	2.316	2.757	3.279	4.270	5.076
3	0.692	0.822	0.979	1.162	1.386	1.647	1.965	2.329	2.773	3.298	4.295	5.105
4	0.696	0.827	0.985	1.169	1.394	1.656	1.976	2.342	2.789	3.318	4.320	5.135
5	0.700	0.831	0.990	1.176	1.402	1.666	1.988	2.356	2.805	3.337	4.345	5.164
6	0.704	0.836	0.996	1.182	1.410	1.675	1.999	2.369	2.821	3.356	4.370	5.194
7	0.708	0.841	1.002	1.189	1.418	1.685	2.010	2.383	2.837	3.375	4.394	5.224
8	0.712	0.845	1.007	1.196	1.426	1.694	2.021	2.396	2.853	3.394	4.419	5.253
9	0.716	0.850	1.013	1.202	1.434	1.704	2.033	2.410	2.869	3.413	4.444	5.283
10	0.720	0.855	1.019	1.209	1.442	1.713	2.044	2.423	2.885	3.432	4.469	5.312
11	0.724	0.860	1.024	1.216	1.450	1.723	2.055	2.437	2.901	3.451	4.494	5.342
12	0.728	0.864	1.030	1.222	1.458	1.732	2.067	2.450	2.917	3.470	4.518	5.371
13	0.732	0.869	1.035	1.229	1.466	1.742	2.078	2.464	2.933	3.489	4.543	5.401
14	0.736	0.874	1.041	1.236	1.474	1.751	2.089	2.477	2.949	3.508	4.568	5.430
15	0.740	0.878	1.047	1.243	1.482	1.761	2.101	2.490	2.965	3.527	4.593	5.460
16	0.744	0.883	1.052	1.249	1.490	1.770	2.112	2.504	2.981	3.547	4.618	5.489
17	0.748	0.888	1.058	1.256	1.498	1.780	2.123	2.517	2.997	3.566	4.642	5.519
18	0.752	0.893	1.064	1.263	1.506	1.789	2.135	2.531	3.013	3.585	4.667	5.548
19	0.756	0.897	1.069	1.269	1.514	1.799	2.146	2.544	3.029	3.604	4.692	5.578
20	0.760	0.902	1.075	1.276	1.522	1.808	2.157	2.558	3.045	3.623	4.717	5.607
21	0.764	0.907	1.081	1.283	1.530	1.818	2.169	2.571	3.061	3.642	4.742	5.637
22	0.768	0.911	1.086	1.289	1.538	1.827	2.180	2.585	3.077	3.661	4.766	5.666
23	0.772	0.916	1.092	1.296	1.546	1.837	2.191	2.598	3.093	3.680	4.791	5.696
24	0.776	0.921	1.097	1.303	1.554	1.846	2.203	2.612	3.109	3.699	4.816	5.726
25	0.780	0.926	1.103	1.310	1.562	1.856	2.214	2.625	3.125	3.718	4.841	5.755
26	0.784	0.930	1.109	1.316	1.570	1.865	2.225	2.638	3.141	3.737	4.866	5.785
27	0.787	0.935	1.114	1.323	1.578	1.875	2.237	2.652	3.157	3.756	4.890	5.814
28	0.791	0.940	1.120	1.330	1.586	1.884	2.248	2.665	3.173	3.776	4.915	5.844
29	0.795	0.944	1.126	1.336	1.594	1.894	2.259	2.679	3.189	3.795	4.940	5.873
30	0.799	0.949	1.131	1.343	1.602	1.903	2.271	2.692	3.205	3.814	4.965	5.903
31	0.803	0.954	1.137	1.350	1.610	1.913	2.282	2.706	3.221	3.833	4.990	5.932

Table 1 shows all possible comparator trip point voltage settings. There are 384 available voltages, ranging from 0.680V to 5.932V, as well as a 'near-ground' monitor threshold of 80mV which can be used to determine if a power supply rail has completely discharged to an OFF state. In addition to these 385 voltage monitor trip points, the user can add external resistors to divide down the voltage and achieve virtually any voltage trip point. This allows the capability to monitor higher voltages such and 12V, 15V, 24V, etc. Voltage monitor trip points are set in the graphical user interface of PAC-Designer software by simple pull-down menus. The user simply selects the given range and corresponding trip point value. Attenuation and reference values are set internally using E^2CMOS configuration bits internal to the device.

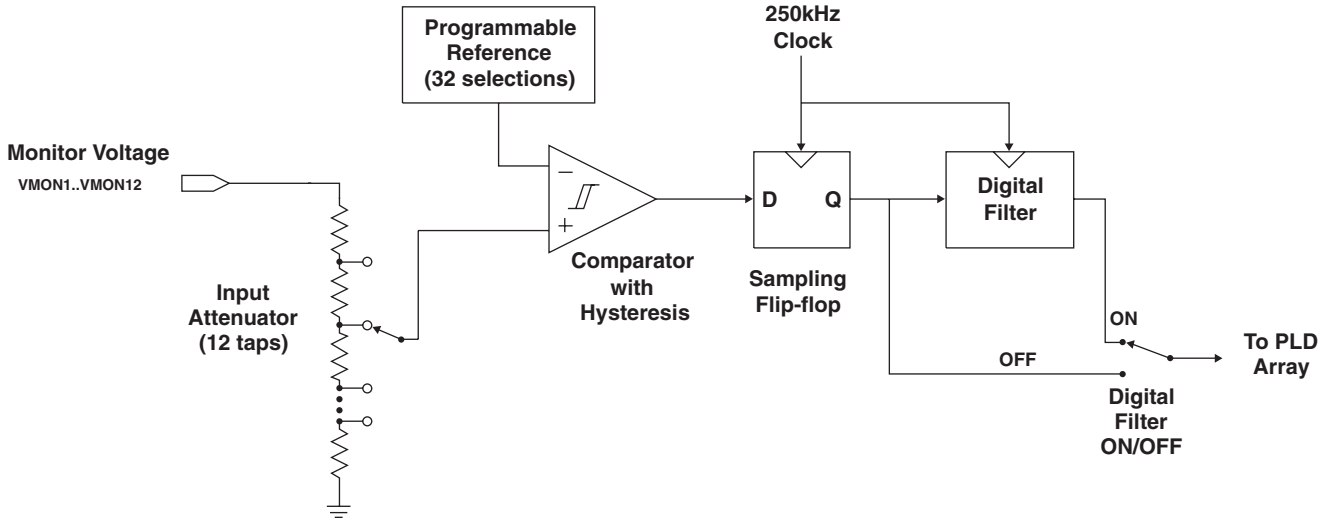
Theory Of Operation

The ispPAC-POWR1208P1 incorporates programmable voltage monitors along with digital inputs and outputs as well as high voltage FET gate drivers to control MOSFETs for ramping up power supply rails. The 16 macrocell

PLD inputs are from the 12 voltage monitors and four digital inputs. There are four embedded programmable timers that interface with the PLD, along with an internal programmable oscillator.

The 12 independently programmable voltage monitors each have 384 programmable trip points over the range of 0.680V to 5.932V. Additionally, a 80mV 'near-ground' sensing threshold is selectable which allows the voltage monitors to determine if a monitored signal has dropped to ground-level. This feature is especially useful for determining if a power supply's output has completely turned off. Figure 2 shows a simplified schematic representation of one of these monitors.

Figure 2. Voltage Monitors



Each monitor consists of four major subsystems. The core of the monitor is a precision voltage comparator. This comparator outputs a HIGH signal to the PLD array if the voltage at its positive terminal is greater than that at its negative terminal, otherwise it outputs a LOW signal. A small amount of hysteresis is provided by the comparator to reduce the effects of input noise.

The second subsystem is a programmable resistive divider that attenuates the input signal before it is fed into the comparator. This feature is used to determine the coarse range in which the comparator should trip (e.g. 1.8V, 3.3V, 5V). Twelve possible ranges are available from the input divider network.

The third subsystem is a programmable reference, which may be set to one of 32 possible values scaled in approximately 0.5% increments apart from each other, allowing for fine-tuning of the voltage monitor's trip points. One additional setting is provided to implement the 80mV 'near-ground' sense setting. This combination of coarse and fine adjustment supports 384 possible trip-point voltages for a given monitor circuit, in addition to the 'near-ground' sense setting. Because each monitor's reference and input divider settings are completely independent of those of the other monitor circuits, the user can set any input monitor to any of the 385 available settings.

A comparator will turn on at the specified trip-point and turn off at the specified trip-point minus the hysteresis. The hysteresis provided by the voltage monitor is a function of the input divider setting and is derived from the difference in voltage between the current setting and the one immediately below it. The following table lists the typical hysteresis versus voltage monitor trip-point.

Table 2. Comparator Hysteresis vs. Setpoint

Setpoint Range (V)		
Low Limit	**High Limit**	**Hysteresis (mV)**
5.017	5.932	30
4.221	4.99	25
3.241	3.833	19
2.724	3.221	16
2.289	2.706	14
1.931	2.282	12
1.618	1.913	10
1.363	1.61	8
1.142	1.35	7
0.962	1.137	6
0.808	0.954	5
0.68	0.803	4
80 mV		0 (disabled)

The fourth subsystem in the ispPAC-POWR1208P1's input voltage monitor is a synchronizer latch and optional digital filter. The synchronizer flip-flop samples the comparator's output state synchronously with the internal system clock. Synchronous sampling effectively eliminates the possibility of race conditions occurring in any state-controllers implemented in the ispPAC-POWR1208P1's internal PLD logic.

An optional digital filter is also provided for each comparator input for the purpose of suppressing glitches and other short transients. This filter is implemented using a saturating counter. When the comparator output is HIGH, the filter counts up to a maximum of '111', and when the comparator output is LOW the filter counts down to a minimum of '000'. When a '111' count is reached, the output of the filter is set HIGH, and when the '000' count is reached, the output is set LOW. Because the filter is clocked at the same rate as the synchronizer, the combination of the two imposes a delay of 8 sampling periods, or 32 clock cycles (32µs at 1MHz). The digital filters may be enabled or disabled individually on a channel-by-channel basis by the user.

PLD Architecture

The ispPAC-POWR1208P1 digital logic is composed of an internal PLD that is programmed to perform the sequencing functions. The PLD architecture allows flexibility in designing various state machines and control logic used for monitoring. The macrocell shown in Figure 3 is the heart of the PLD. There are 16 macrocells that can be used to control the functional states of the sequencer state machine or other control or monitoring logic. The PLD AND array shown in Figure 4 has 36 inputs, and 81 product terms (PTs). The resources from the AND array feed the 16 macrocells. The resources within the macrocells share routing and contain a product-term allocation array. The product term allocation array greatly expands the PLD's ability to implement complex logical functions by allowing logic to be shared between adjacent blocks and distributing the product terms to allow for wider decode functions.

The basic macrocell has five product terms that feed the OR gate and the flip-flop. The flip-flop in each macrocell is independently configured. It can be programmed to function as a D-Type or T-Type flip-flop. Combinatorial functions are realized by bypassing the flip-flop. By having the polarity control XOR, the logic reduction can be best fit to minimize the number of product terms. The flip-flop's clock is driven from a common clock that can be generated from a pre-scaled, on-board clock source or from an external clock. The macrocell also supports asynchronous reset and preset functions, derived from either product terms, the global reset input or the power-on reset signal.

Figure 3. ispPAC-POWR1208P1 Macrocell Block Diagram

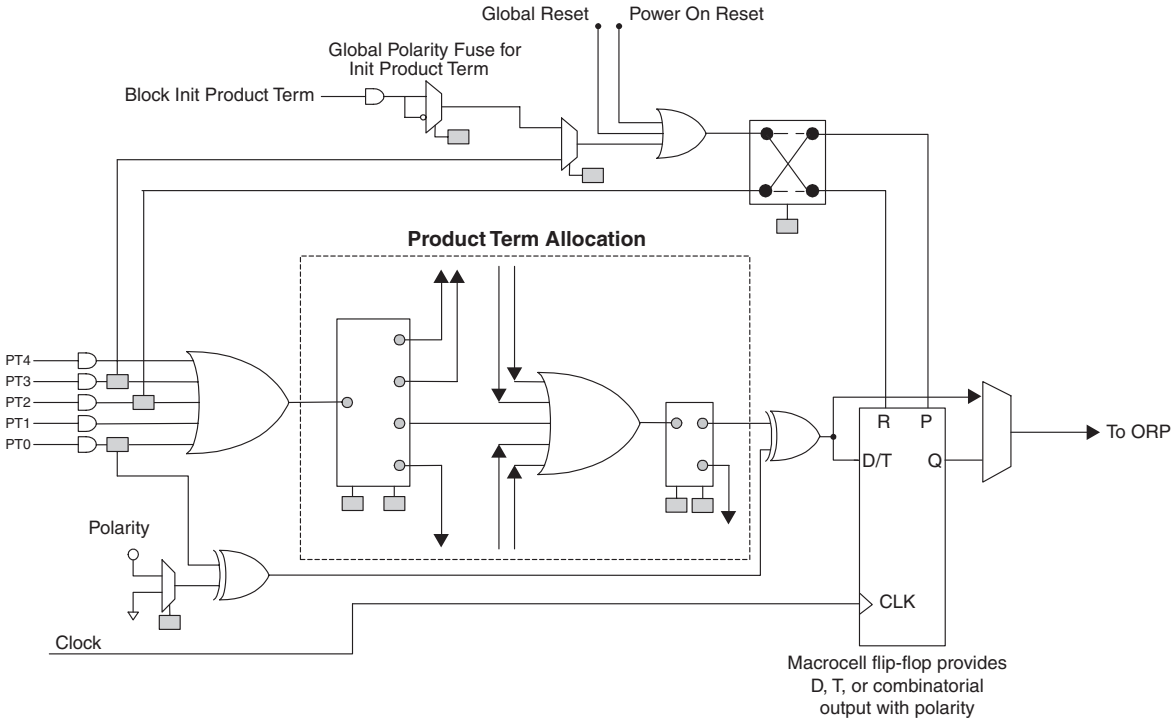
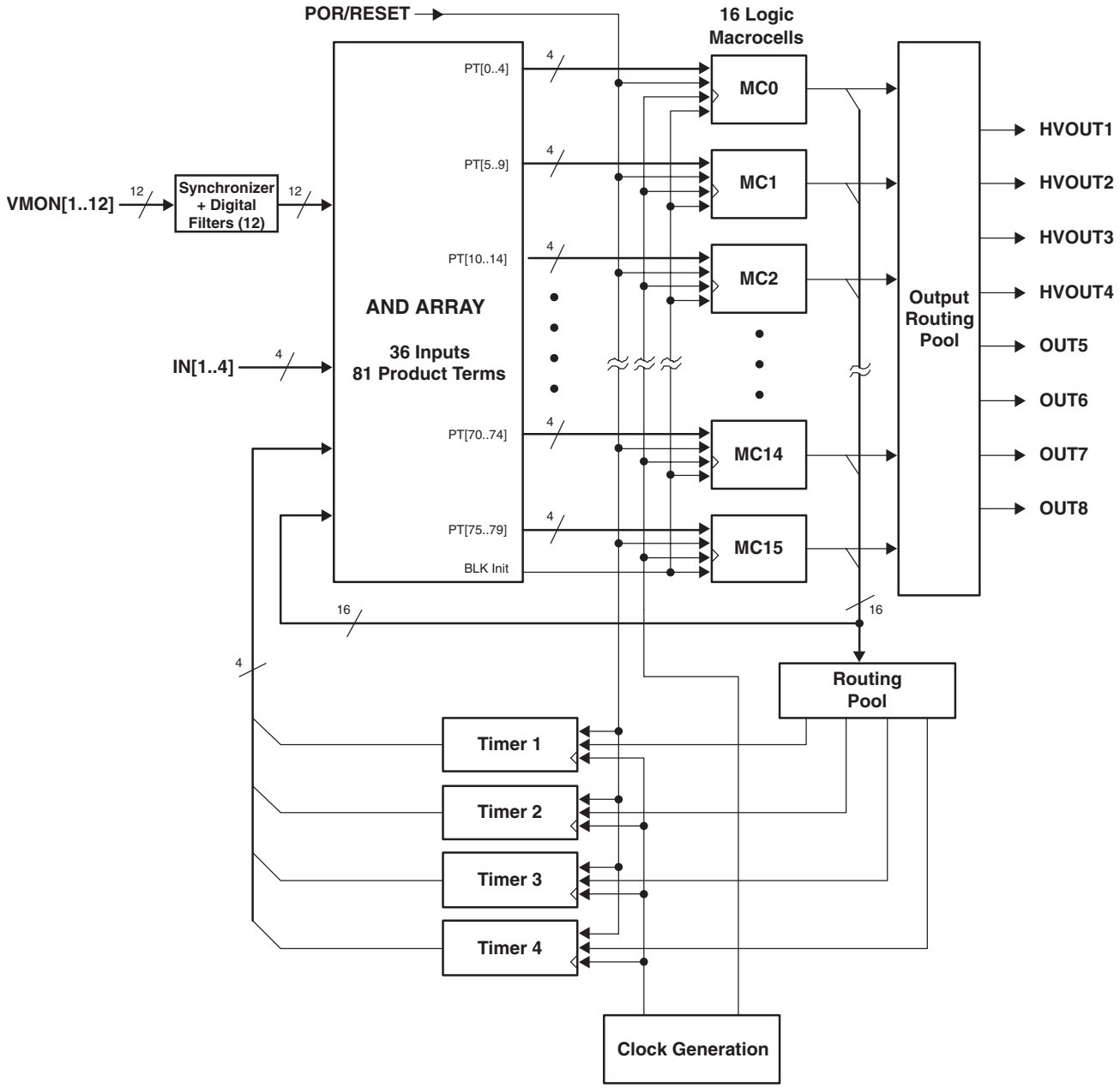


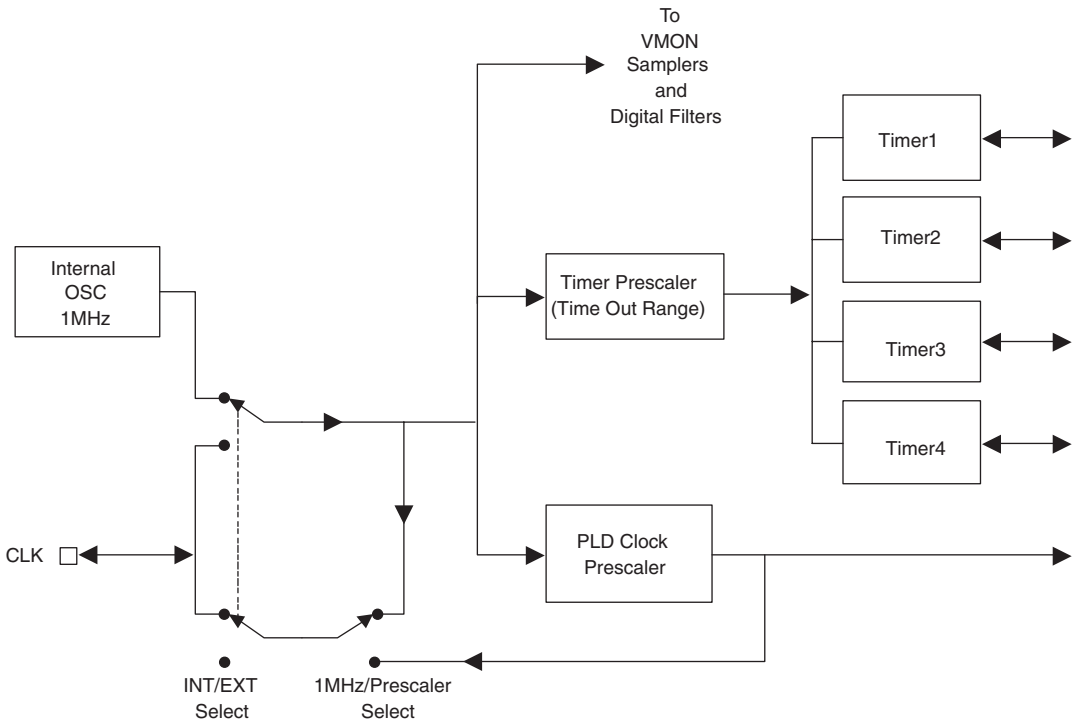
Figure 4. PLD and Timer Functional Block Diagram



Clock and Timer Systems

Figure 5 shows a block diagram of the ispPAC-POWR1208P1's internal clock and timer systems. The PLD clock can be programmed with eight different frequencies based on the internal oscillator frequency of 1MHz.

Figure 5. Clock and Timer Block



The internal oscillator runs at a fixed frequency of 1 MHz. This signal is used as a source for the PLD clock prescaler, the timer clock prescaler, and also for synchronizing the comparator outputs and clocking the digital filters in the voltage monitor circuits. Figure 5 shows a functional block diagram of the ispPAC-POWR1208P1's internal clock system. The ispPAC-POWR1208P1 can operate from either its own internal or an external supplied clock source. When the device is configured to use the internal clock source (Schematically, INT/EXT select switch is in upper position), the CLK pin operates as an output. The user may select either the 1MHz internal clock, or the output of the PLD clock prescaler to be driven out of this pin (1MHz/Prescaler select switch). When the device is configured to use the external clock source (INT/EXT select switch is in lower position), the CLK pin is configured as an input, and the externally applied clock signal is routed to all prescalers, synchronizers, and other internal functions.

The ispPAC-POWR1208P1 provides prescalers to provide for flexibility in selecting the PLD clock and wide dynamic range for the timers. The frequencies available for the PLD clock will be the external clock frequency divided by the chosen prescaler value (listed in Table 3).

Table 3. PLD Clock Frequency (kHz) PLD Prescaler Divider[1]

PLD Prescaler Divider	PLD Clock Frequency (kHz)
4	250
8	125
16	62.5
32	31.3
64	15.6
128	7.8
256	3.9
512	2.0

1. Frequency values based on 1MHz clock

Because the ispPAC-POWR1208P1's PLD array is clocked from a divided-down version of the device's 1MHz main clock, special considerations must be observed for asserting input data if it is to be reliably recognized by state machines implemented using the device. Data presented to the IN1 through IN4 digital inputs must be asserted for a minimum of at least one PLD clock period (4µs – 512µs depending on the PLD prescaler setting) to be recognized. For data presented to the VMON inputs, this minimum assertion time may need to be increased to account for the behavior of the VMON samplers and digital filters (when enabled).

The Timer Clock Pre-Scaler divides the internal 1MHz oscillator (or external clock, if selected) down before it generates the clock for the four programmable timers. The pre-scaler has eight different divider ratios, shown in Table 4. Each divider ratio provides a range of intervals to which each of the four timers may be independently programmed. Please note that since there is only one prescaler, all of the timer intervals must lie within the range associated with the selected prescaler value.

Table 4. Timer Values[1]

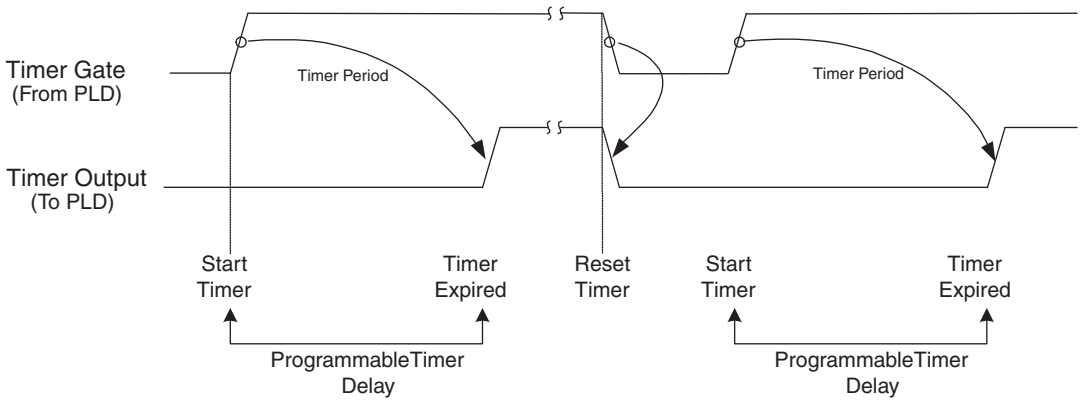
÷ 16 62.5 kHz	÷ 32 31.2 kHz	÷ 64 15.6 kHz	÷ 128 7.8 kHz	÷ 256 3.9 kHz	÷ 512 2.0 kHz	÷ 1024 1.0 kHz	÷ 2048 0.5 kHz
0.032 ms							
0.064 ms	0.064 ms						
0.128 ms	0.128 ms	0.128 ms					
0.256 ms	0.256 ms	0.256 ms	0.256 ms				
0.512 ms	0.512 ms	0.512 ms	0.512 ms	0.512 ms			
1.024 ms	1.024 ms	1.024 ms	1.024 ms	1.024 ms	1.024 ms		
2.048 ms	2.048ms	2.048ms	2.048ms	2.048ms	2.048ms	2.048ms	
4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms	4.096 ms
	8.192 ms	8.192 ms	8.192 ms	8.192 ms	8.192 ms	8.192 ms	8.192 ms
		16.384 ms	16.384 ms	16.384 ms	16.384 ms	16.384 ms	16.384 ms
			32.768 ms	32.768 ms	32.768 ms	32.768 ms	32.768 ms
				65.536 ms	65.536 ms	65.536 ms	65.536 ms
					131.072 ms	131.072 ms	131.072 ms
						262.144 ms	262.144 ms
							524.288 ms

1. Timer values based on 1MHz clock.

For design entry, the user can select the source for the clock and the PAC-Designer software will calculate the appropriate delays in an easy-to-select menu format.

The control inputs for Timer1-Timer4 can be driven by any of the 16 PLD macrocell outputs. The reset for the timers is a function of the Global Reset pin ($\overline{\text{RESET}}$), a power-on reset or when the timer gate goes low. The waveforms in Figure 6 show the basic timer start and reset functions. Timer and clock divider values are entered in during the design phase using PAC-Designer software, simple pull-down menus allow the user to select the clocking mode and the values for the timers and the PLD clock.

Figure 6. Timer Waveforms

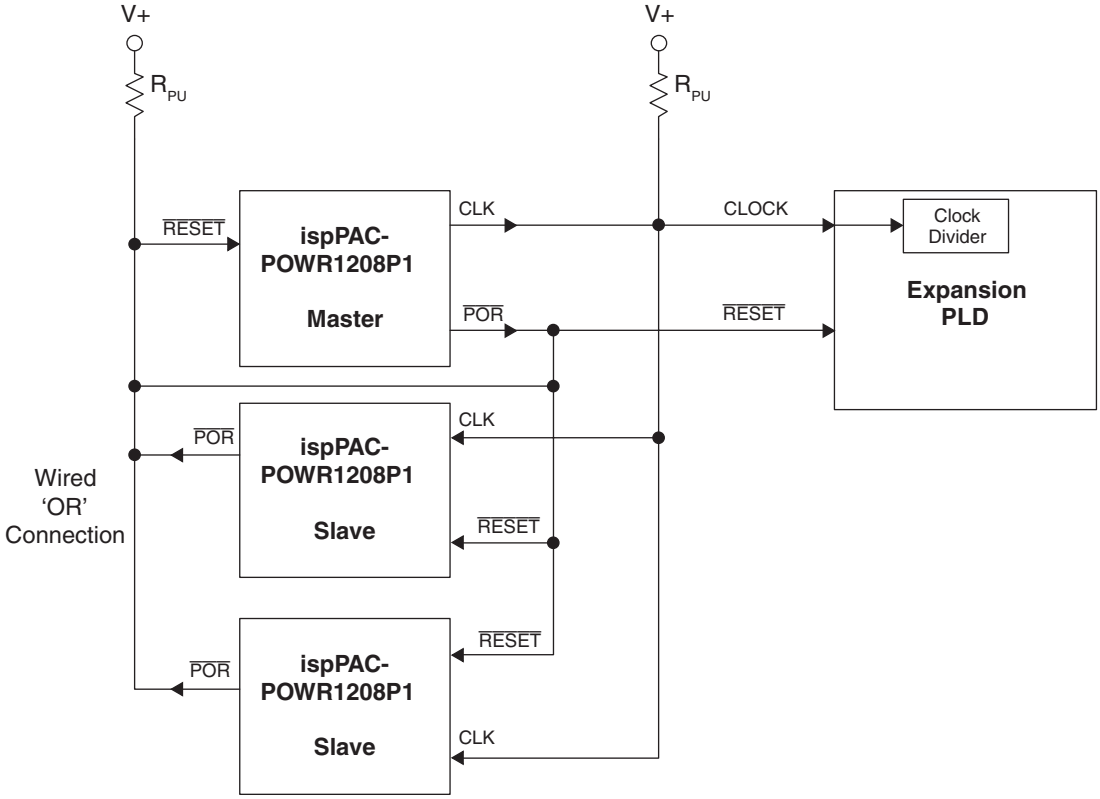


Note that if the clock module is configured as “slave” (i.e. the CLK is an input), the actual time-out of the four timers is determined by the external clock frequency.

Master-Slave and PLD Expansion Modes

To support designs requiring more I/O or logic resources than those provided by the ispPAC-POWR1208P1, it is possible to gang a number of devices together, or to add a CPLD to provide additional logic. Figure 7 shows an example of slaving a CPLD and two ispPAC-POWR1208P1's to a single master device

Figure 7. Example of ispPAC-POWR1208P1's and CPLD in Expansion Mode



In this circuit a 1 MHz CLK output is broadcast from the master device to all of the slave devices. The PLD prescaler should be set identically for both the master and slave ispPAC device to ensure synchronous operation. In the case of the CPLD, some internal logic will need to be used to essentially replicate the function of the ispPAC devices' PLD prescaler to ensure that it also operates synchronously.

The $\overline{\text{POR}}$ (power-on reset) signal from the master device is broadcast to all of the slave devices, holding them in a reset state until the master device's power-on-reset sequence completes. Because each of the ispPAC slave devices have their own power-on-reset circuitry, their signals are wire-OR'ed together and fed back into the master device's $\overline{\text{RESET}}$. This causes all of the devices to remain in a reset state until all power-on-reset sequences have been successfully completed.

While it is possible to also slave ispPAC-POWR1208 and ispPAC-POWR604 devices to an ispPAC-POWR1208P1, the converse is not true. This is because the ispPAC-POWR1208 and 604 devices operate from a 250kHz internal clock, while the ispPAC-POWR1208P1 requires a 1MHz clock to maintain proper internal operation. Table 5 summarizes the requirements for slaving a device to the ispPAC-POWR1208P1.

Table 5. ispPAC-POWR1208P1 Expansion Requirements

Slave Device	Slave Configuration	Master Configuration
ispPAC-POWR1208P1	External Clock Mode	Select 1MHz Clock Output
ispPAC-POWR1208 ispPAC-POWR604	External Clock Mode	Select PLD Prescaler Output
CPLD or FPGA	Clock Prescaler implemented in logic	Select 1MHz Clock Output
	No Clock Prescaler	Select PLD Prescaler output

Note that because different slave devices impose different requirements for master clock output frequency, there are limitations on what types of slave devices may be operated synchronously from a single master. For example, it is not generally possible to slave both ispPAC-POWR1208P1's and ispPAC-POWR1208's (or POWR604's) together to a single ispPAC-POWR1208P1.

Output Configuration Modes

The output pins for the ispPAC-POWR1208P1 device are programmable for different functional modes. The four outputs HVOUT1-HVOUT4, can be used as FET gate drivers or be programmed as open-drain digital outputs. Figure 8 explains the details of the gate driver mode.

Figure 8. Basic Function Diagram for an Output in High-Voltage MOSFET Gate Driver Mode

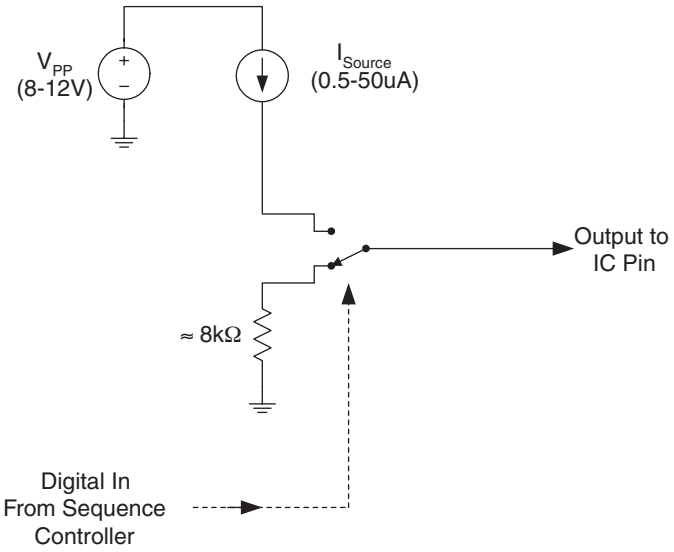
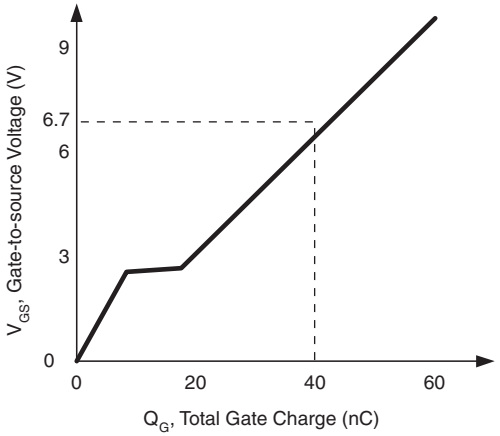


Figure 8 shows an output programmed for gate driver mode. In this mode the output is a current source that is programmable between 0.5µA to 50µA. The maximum voltage that the output level at the pin will rise is also programmable. The levels required depend on the gate-to-source threshold of the FET and the supply voltage. The maximum level needs to be sufficient to bias the gate-to-source threshold on and also accommodate the load voltage at the FET's source, since the source pin of the FET is tied to the supply of the target board. When the HVOUT pin is sourcing current, charging a FET gate, the current is programmable between 0.5µA and 50µA. When the driver is turned to the off state, the driver will sink current to ground through the 8kΩ resistor.

Predicting MOSFET Turn-on Time

Because the ispPAC-POWR1208P1's MOSFET output drivers source a precise and well-defined output current, it becomes possible to predict MOSFET gate rise times if one knows the value of the load capacitance presented by the MOSFET being driven. The other method is by relating the total gate charge to the gate-to-source voltage.

Figure 9. MOSFET Gate Charge vs. Gate-Source Voltage



Using this method, it becomes straightforward to estimate the gate rise time for a given charging current. As an example a MOSFET's source voltage (V_S) will be 3.3V when the device is fully switched on, while the gate voltage (V_G) will be 10V in this condition. The device's gate-to-source voltage (V_{GS}) will therefore be 6.7V. Reading across and down the plot of Figure 9, a V_{GS} of 6.7V corresponds to ~40 nC of gate charge (Q_G). Because charge is equal to the product of current (I) and time ($t_{CHARGE-TIME}$) when current is constant, gate charging time can be expressed as:

$$i = \frac{dQ}{dt} \quad (1)$$

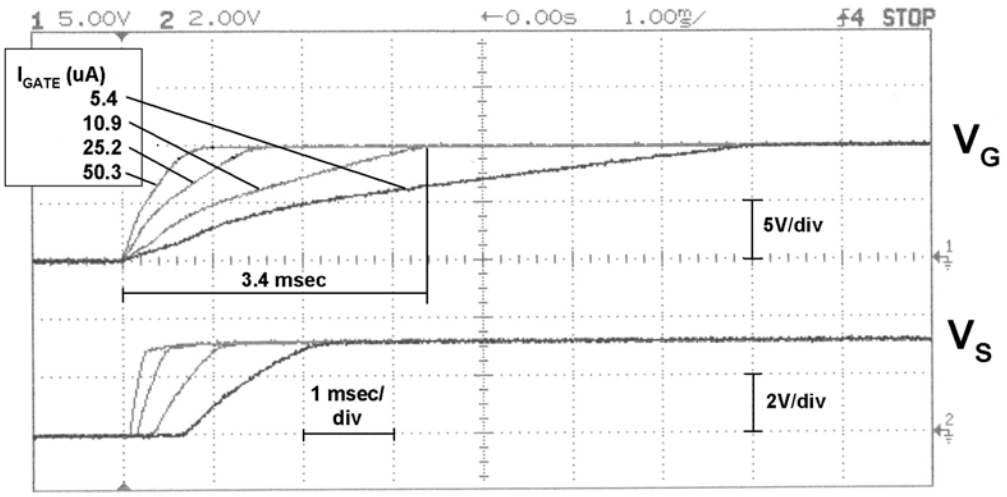
$$t_{CHARGE-TIME} = \frac{Q_G}{I} \quad (2)$$

For this example, let us assume a charging current of 10.9µA. Gate charging time is given by:

$$t_{CHARGE-TIME} = \frac{40 \times 10^{-9}C}{10.9 \times 10^{-6}A} = 3.7 \times 10^{-3}s \quad (3)$$

Validation of this result can be seen in the scope plot shown in Figure 10. The top set of traces shows gate rise times for various (5.5µA to 50.3µA) gate drive currents. The trace labeled 10.9µA shows gate voltage V_G rising from 0V to 10V in slightly over 3 milliseconds, which agrees to within 25% of our predicted value, well within the limits of device-to-device variation.

Figure 10. Gate and Source Voltage Responses for a 3.3V Supply



MOSFET gate capacitance ranges from hundreds to thousands of picoFarads. Refer to the MOSFET manufacturer's data sheet for values of Cgs (Capacitance gate-to-source). If slower ramps are required, an additional external low leakage capacitor (e.g. a polycarbonate or other poly type capacitor) can be added from the gate to ground. As a good design practice, it is recommended that a series resistor of 10-100Ω be placed in the gate drive signal near the FET gate pin to reduce the possibility that the FET may self-oscillate.

Charge Pump

Four internal charge pumps are provided to fully support external N-channel FET devices. No external components are required for the charge pumps. The output voltage is programmable from 8 to 12V in 0.5V steps. The user must select a high voltage limit no greater than 7.5V above V_{DD} (the software assists this process). This voltage is controlled with an on-chip feedback loop, and is independent of the actual supply voltage.

Programmable Output Voltage Levels for HVOUT1- HVOUT4

There are eight selectable steps for the output voltage of the FET drivers when in FET driver mode. The output pins HVOUT1-4 are current source outputs, each with a programmable current. The current is programmable in 32 different steps ranging from 0.5µA to 50µA. The voltage that the pin is capable of driving to is listed in Table 6. For each supply range, the charge-pump range will be set by the software.

Table 6. HVOUT Gate Driver Voltage Range

V_{DD} = 3.3V	V_{DD} = 5V
8	8
8.5	8.5
9	9
9.5	9.5
10	10
	10.5
	11
	12

IEEE Standard 1149.1 Interface

Communication with the ispPAC-POWR1208P1 is facilitated via an IEEE 1149.1 test access port (TAP). It is used by the ispPAC-POWR1208P1 as a serial programming interface, and not for boundary scan test purposes. There are no boundary scan logic registers in the ispPAC-POWR1208P1 architecture. This does not prevent the ispPAC-POWR1208P1 from functioning correctly, however, when placed in a valid serial chain with other IEEE 1149.1 compliant devices. Since the ispPAC-POWR1208P1 is used to powerup other devices, it should be programmed in a separate chain from PLDs, FPGAs or other JTAG devices.

A brief description of the ispPAC-POWR1208P1 serial interface follows. For complete details of the reference specification, refer to the publication, Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (which now includes IEEE Std 1149.1a-1993).

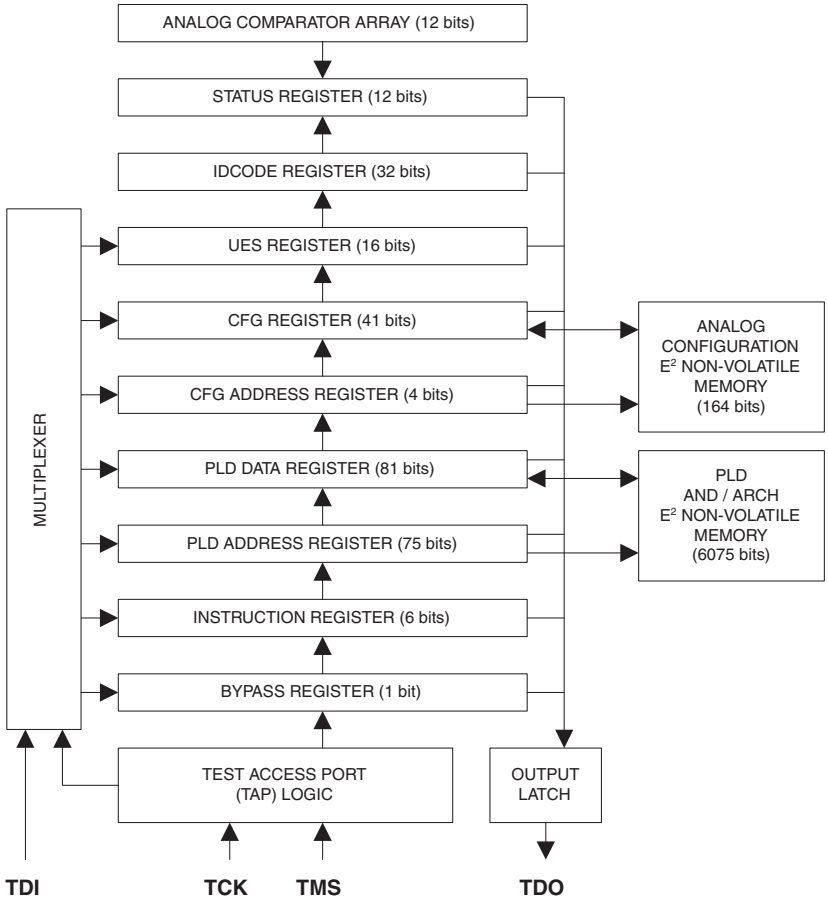
Overview

An IEEE 1149.1 test access port (TAP) provides the control interface for serially accessing the digital I/O of the ispPAC-POWR1208P1. The TAP controller is a state machine driven with mode and clock inputs. Under the correct protocol, instructions are shifted into an instruction register, which then determines subsequent data input, data output, and related operations. Device programming is performed by addressing various registers, shifting data in, and then executing the respective program instruction. The programming instructions transfer the data into internal E^2CMOS memory. It is these non-volatile memory cells that determine the configuration of the ispPAC-POWR1208P1. By cycling the TAP controller through the necessary states, data can also be shifted out of the various registers to verify the current ispPAC-POWR1208P1 configuration. Instructions exist to access all data registers and perform internal control operations.

For compatibility between compliant devices, two data registers are mandated by the IEEE 1149.1 specification. Other registers are functionally specified, but inclusion is strictly optional. Finally, there are provisions for optional user data registers that are defined by the manufacturer. The two required registers are the bypass and boundary-scan registers. For ispPAC-POWR1208P1, the bypass register is a 1-bit shift register that provides a short path through the device when boundary testing or other operations are not being performed. The ispPAC-POWR1208P1, as mentioned earlier has no boundary-scan logic and therefore no boundary scan register. All instructions relating to boundary scan operations place the ispPAC-POWR1208P1 in the BYPASS mode to maintain compliance with the specification.

The optional identification (IDCODE) register described in IEEE 1149.1 is also included in the ispPAC-POWR1208P1. Six additional user data registers are included in the TAP of the ispPAC-POWR1208P1 as shown in Figure 11. Most of these additional registers are used to program and verify the analog configuration (CFG) and PLD bits. A status register is also provided to read the status of the twelve analog comparators.

Figure 11. TAP Registers

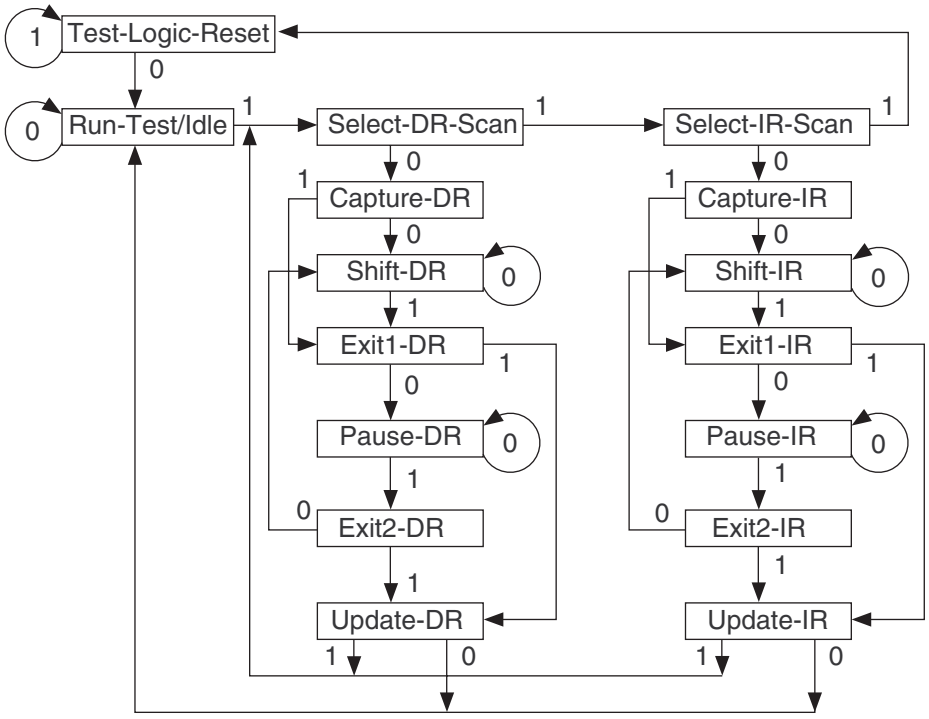


TAP Controller Specifics

The TAP is controlled by the Test Clock (TCK) and Test Mode Select (TMS) inputs. These inputs determine whether an Instruction Register or Data Register operation is performed. Driven by the TCK input, the TAP consists of a small 16-state controller. In a given state, the controller responds according to the level on the TMS input as shown in Figure 12. Test Data In (TDI) and TMS are latched on the rising edge of TCK, with Test Data Out (TDO) becoming valid on the falling edge of TCK. There are six steady states within the controller: Test-Logic-Reset, Run-Test/Idle, Shift-Data-Register, Pause-Data-Register, Shift-Instruction-Register, and Pause-Instruction-Register. But there is only one steady state for the condition when TMS is set high: the Test-Logic-Reset state. This allows a reset of the test logic within five TCKs or less by keeping the TMS input high. Test-Logic-Reset is the power-on default state.

When the correct logic sequence is applied to the TMS and TCK inputs, the TAP will exit the Test-Logic-Reset state and move to the desired state. The next state after Test-Logic-Reset is Run-Test/Idle. Until a data or instruction scan is performed, no action will occur in Run-Test/Idle (steady state = idle). After Run-Test/Idle, either a data or instruction scan is performed. The states of the Data and Instruction Register blocks are identical to each other differing only in their entry points. When either block is entered, the first action is a capture operation. For the Data Registers, the Capture-DR state is very simple; it captures (parallel loads) data onto the selected serial data path (previously chosen with the appropriate instruction). For the Instruction Register, the Capture-IR state will always load the IDCODE instruction. It will always enable the ID Register for readout if no other instruction is loaded prior to a Shift-DR operation. This, in conjunction with mandated bit codes, allows a “blind” interrogation of any device in a compliant IEEE 1149.1 serial chain.

Figure 12. TAP States



Note: The value shown adjacent to each state transition represents the signal present at TMS at the time of a rising edge at TCK.

From the Capture state, the TAP transitions to either the Shift or Exit1 state. Normally the Shift state follows the Capture state so that test data or status information can be shifted out or new data shifted in. Following the Shift state, the TAP either returns to the Run-Test/Idle state via the Exit1 and Update states or enters the Pause state via Exit1. The Pause state is used to temporarily suspend the shifting of data through either the Data or Instruction Register while an external operation is performed. From the Pause state, shifting can resume by re-entering the Shift state via the Exit2 state or be terminated by entering the Run-Test/Idle state via the Exit2 and Update states. If the proper instruction is shifted in during a Shift-IR operation, the next entry into Run-Test/Idle initiates the test mode (steady state = test). This is when the device is actually programmed, erased or verified. All other instructions are executed in the Update state.

Test Instructions

Like data registers, the IEEE 1149.1 standard also mandates the inclusion of certain instructions. It outlines the function of three required and six optional instructions. Any additional instructions are left exclusively for the manufacturer to determine. The instruction word length is not mandated other than to be a minimum of two bits, with only the BYPASS and EXTEST instruction code patterns being specifically called out (all ones and all zeroes respectively). The ispPAC-POWR1208P1 contains the required minimum instruction set as well as one from the optional instruction set. In addition, there are several proprietary instructions that allow the device to be configured, verified, and monitored. For ispPAC-POWR1208P1, the instruction word length is 6-bits. All ispPAC-POWR1208P1 instructions available to users are shown in Table 7.

Table 7. ispPAC-POWR1208P1 TAP Instruction Table

Instruction	Code	Description
EXTEST	000000	External Test. Defaults to BYPASS.
ADDPLD[1]	000001	Address PLD address register (75 bits).
DATAPLD[1]	000010	Address PLD column data register (81 bits).
ERASEAND[1, 2]	000011	Bulk Erase AND array.
ERASEARCH[1, 2]	000100	Bulk Erase Architect array.
PROGPLD[1, 2]	000101	Program PLD column data register into E^2.
PROGESF[1, 2]	000110	Program the Electronic Security Fuse bit.
BYPASS	000111	Bypass (connect TDI to TDO).
READPLD[1]	001000	Reads PLD column data from E^2 to the register (81 bits).
DISCHARGE[1]	001001	Fast VPP discharge.
ADDCFG[1]	001010	Address CFG array address (4 bits).
DATACFG[1]	001011	Address CFG data (41 bits).
ERASECFG[1, 2]	001100	Bulk Erase CFG data.
PROGCFG[1, 2]	001101	Program CFG data register into E^2.
READCFG[1]	001110	Read CFG column data from E^2 to the register (41 bits).
CFGBE[1, 2]	010110	Bulk Erase all E^2 memory (CFG, PLD, USE, and ESF).
SAFESTATE[1]	010111	Digital outputs hiZ (FET pulled L)
PROGRAMEN[1]	011000	Enable program mode (SAFESTATE IO)
IDCODE	011001	Address Identification Code data register (32 bits).
PROGRAMDIS	011010	Disable Program mode (normal IO)
ADDSTATUS	011011	Address STATUS register (12 bits).
SAMPLE	011100	Sample/Preload. Default to Bypass.
ERASEUES[1, 2]	011101	Bulk Erase UES.
SHIFTUES	011110	Reads UES data from E^2 and selects the UES register (16 bits).
PROGUES[1, 2]	011111	Program UES data register into E^2.
BYPASS	1xxxxx	Bypass (connect TDI to TDO).

1. When these instructions are executed, the outputs are placed in the same mode as the instruction SAFESTATE (as described later) to prevent invalid and potentially destructive power supply sequencing.
2. Instructions that erase or program the E^2CMOS memory must be executed only when the supply to the device is maintained at 3.0V to 5.5V.

BYPASS is one of the three required instructions. It selects the Bypass Register to be connected between TDI and TDO and allows serial data to be transferred through the device without affecting the operation of the ispPAC-POWR1208P1. The IEEE 1149.1 standard defines the bit code of this instruction to be all ones (111111).

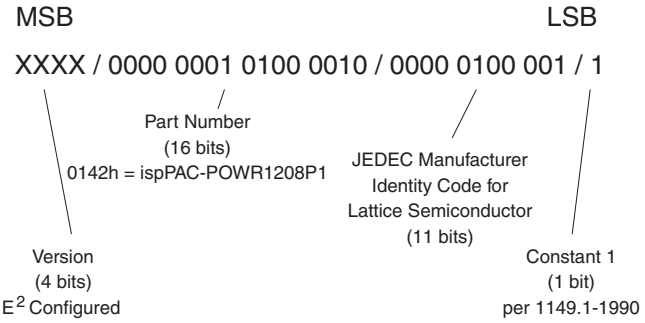
The required **SAMPLE/PRELOAD** instruction dictates the Boundary-Scan Register be connected between TDI and TDO. The ispPAC-POWR1208P1 has no boundary scan register, so for compatibility it defaults to the BYPASS mode whenever this instruction is received. The bit code for this instruction is defined by Lattice as shown in Table 7.

The **EXTEST** (external test) instruction is required and would normally place the device into an external boundary test mode while also enabling the boundary scan register to be connected between TDI and TDO. Again, since the ispPAC-POWR1208P1 has no boundary scan logic, the device is put in the BYPASS mode to ensure specification compatibility. The bit code of this instruction is defined by the 1149.1 standard to be all zeros (000000).

The optional **IDCODE** (identification code) instruction is incorporated in the ispPAC-POWR1208P1 and leaves it in its functional mode when executed. It selects the Device Identification Register to be connected between TDI and TDO. The Identification Register is a 32-bit shift register containing information regarding the IC manufacturer,

device type and version code (Figure 13). Access to the Identification Register is immediately available, via a TAP data scan operation, after power-up of the device, or by issuing a Test-Logic-Reset instruction. The bit code for this instruction is defined by Lattice as shown in Table 7.

Figure 13. ID Code



ispPAC-POWR1208P1 Specific Instructions

There are 21 unique instructions specified by Lattice for the ispPAC-POWR1208P1. These instructions are primarily used to interface to the various user registers and the E^2CMOS non-volatile memory. Additional instructions are used to control or monitor other features of the device. A brief description of each unique instruction is provided in detail below, and the bit codes are found in Table 7.

ADDPLD – This instruction is used to set the address of the PLD AND/ARCH arrays for subsequent program or read operations. This instruction also forces the outputs into the SAFESTATE.

DATAPLD – This instruction is used to shift PLD data into the register prior to programming or reading. This instruction also forces the outputs into the SAFESTATE.

ERASEAND – This instruction will bulk erase the PLD AND array. The action occurs at the second rising edge of TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

ERASEARCH – This instruction will bulk erase the PLD ARCH array. The action occurs at the second rising edge of TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

PROGPLD – This instruction programs the selected PLD AND/ARCH array column. The specific column is preselected by using ADDPLD instruction. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

PROGESF – This instruction is used to program the electronic security fuse (ESF) bit. Programming the ESF bit protects proprietary designs from being read out. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

READPLD – This instruction is used to read the content of the selected PLD AND/ARCH array column. This specific column is preselected by using ADDPLD instruction. This instruction also forces the outputs into the SAFESTATE.

DISCHARGE – This instruction is used to discharge the internal programming supply voltage after an erase or programming cycle and prepares ispPAC-POWR1208P1 for a read cycle. This instruction also forces the outputs into the SAFESTATE.

ADDCFG – This instruction is used to set the address of the CFG array for subsequent program or read operations. This instruction also forces the outputs into the SAFESTATE.

DATACFG – This instruction is used to shift data into the CFG register prior to programming or reading. This instruction also forces the outputs into the SAFESTATE.

ERASECFG – This instruction will bulk erase the CFG array. The action occurs at the second rising edge of TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

PROGCFG – This instruction programs the selected CFG array column. This specific column is preselected by using ADDCFG instruction. The programming occurs at the second rising edge of the TCK in Run-Test-Idle JTAG state. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

READCFG – This instruction is used to read the content of the selected CFG array column. This specific column is preselected by using ADDCFG instruction. This instruction also forces the outputs into the SAFESTATE.

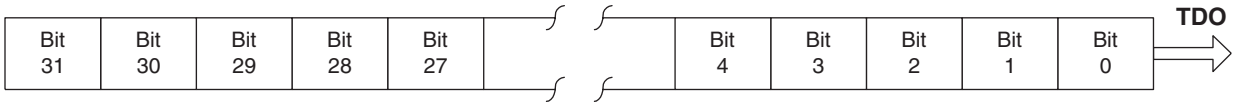
CFGBE – This instruction will bulk erase all E^2CMOS bits (CFG, PLD, UES, and ESF) in the ispPAC-POWR1208P1. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

SAFESTATE – This instruction turns off all of the open-drain output transistors. Pins that are programmed as FET drivers will be placed in the active low state. This instruction is effective after Update-Instruction-Register JTAG state.

PROGRAMEN – This instruction enables the programming mode of the ispPAC-POWR1208P1. This instruction also forces the outputs into the SAFESTATE.

IDCODE – This instruction connects the output of the Identification Code Data Shift (IDCODE) Register to TDO (Figure 14), to support reading out the identification code.

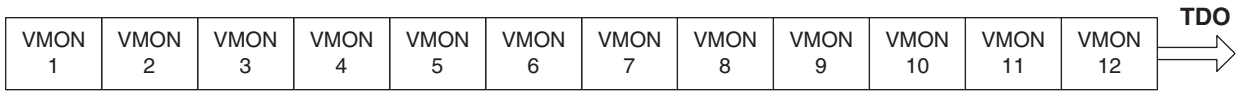
Figure 14. IDCODE Register



PROGRAMDIS – This instruction disables the programming mode of the ispPAC-POWR1208P1. The Test-Logic-Reset JTAG state can also be used to cancel the programming mode of the ispPAC-POWR1208P1.

ADDSTATUS – This instruction is used to both connect the status register to TDO (Figure 15) and latch the 12 voltage monitor (comparator outputs) into the status register. Latching of the 12 comparator outputs into the status register occurs during Capture-Data-Register JTAG state.

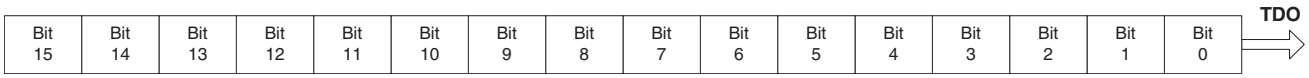
Figure 15. Status Register



ERASEUES – This instruction will bulk erase the content of the UES E^2CMOS memory. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

SHIFTUES – This instruction both reads the E^2CMOS bits into the UES register and places the UES register between the TDI and TDO pins (as shown in Figure U), to support programming or reading of the user electronic signature bits.

Figure 16. UES Register



PROGUES – This instruction will program the content of the UES Register into the UES E^2CMOS memory. The device must already be in programming mode (PROGRAMEN instruction). This instruction also forces the outputs into the SAFESTATE.

Notes:
In all of the descriptions above, SAFESTATE refers both to the instruction and the state of the digital output pins, in which the open-drains are tri-stated and the FET drivers are pulled low.

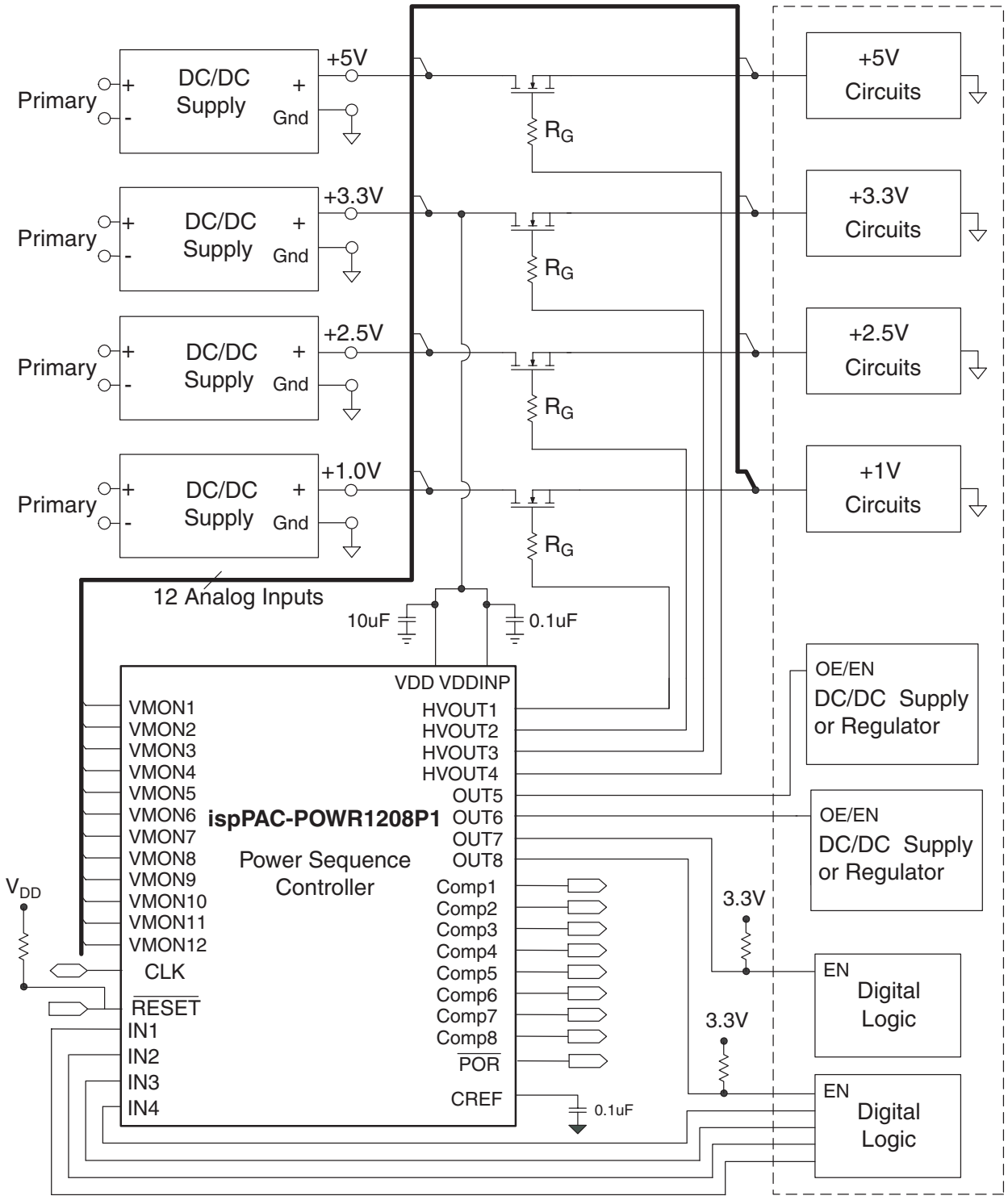
Before any of the above programming instructions are executed, the respective E^2CMOS bits need to be erased using the corresponding erase instruction.

Application Example

The ispPAC-POWR1208P1 device has 12 comparators to monitor various power supply levels. The comparators each have a programmable trip point that is programmed by the user at design time. The output of the comparators are latched and optionally filtered before being fed into the PLD logic array to drive the state machine logic or monitor logic. The comparator's filtered outputs COMP1...COMP8 are also routed to external pins to be monitored directly or can be used to drive additional control logic if expansion is required. The comparator outputs are open-drain type output buffers and require a pull up resistor to drive a logic high. All 12 comparators have hysteresis, the hysteresis is dependent on the voltage trip point scale that is set, it ranges from 4mV for a 0.680V trip point to 30mV for a 5.93V trip point. The comparators can be set with a trip point from 0.68V to 5.93V, with 384 different values. The application diagram shows a set-up that can monitor and control multiple power supplies. The ispPAC-POWR1208P1 device controls FET switches to ramp the supplies at different slew rates and time delays. The digital outputs and inputs are also used to interface with the board that is being powered up.

To reduce the possibility of RF oscillation, a gate resistor (R_G) is often inserted in series with the gate of the MOSFET power switch. This resistor should be placed physically close to the MOSFET gate terminal, and connected by as short a PCB trace as is feasible. An appropriate value for these gate resistors is highly dependent on both the characteristics of the MOSFET being used and the circumstances of the application, but will often be in the range of 10Ω to 100Ω.

Figure 17. Typical Application Example: ispPAC-POWR1208P1 Driving [4] FET Switches [4] Digital OE/EN Lines

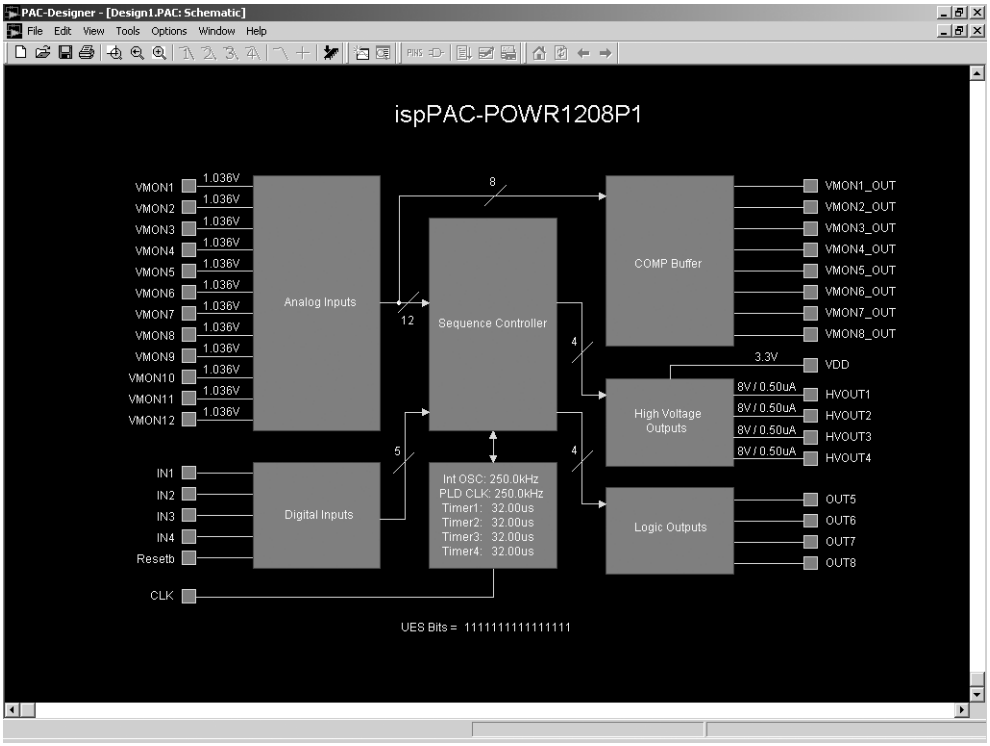


Software-Based Design Environment

Design Entry Software

All functions within the ispPAC-POWR1208P1 are controlled through a Windows-based software development tool called PAC-Designer. PAC-Designer is an easy-to-use graphical user interface (Figure 18) that allows the user to set up the ispPAC-POWR1208P1 to perform given functions, such as timed sequences for power supply and monitor trip points for the voltage monitor inputs. The software tool gives the user control over how the device drives the outputs and the functional configurations for all I/O pins. User-friendly dialog boxes are provided to set and edit all of the analog features of the ispPAC-POWR1208P1. An extension to the schematic screen is the LogiBuilder design environment (Figure 19) that is used to enter and edit control sequences. Again, user-friendly dialog boxes are provided in this window to help the designer to quickly implement sequences that take advantage of the powerful built-in PLD. Once the configurations are chosen and the sequence has been described by the utilities, the device is ready to program. A standard JTAG interface is used to program the E^2CMOS memory. PAC-Designer software supports downloading the device through the PC's parallel port. The ispPAC-POWR1208P1 can be reprogrammed using the software and ispDOWNLOAD® Cable assembly, to adjust for variations in supply timing, sequencing or scaling of voltage monitor inputs.

Figure 18. PAC-Designer Schematic Screen



The user interface (Figure 18) provides access to various internal function blocks within the ispPAC-POWR1208P1 device.

Analog Inputs: Accesses the programmable threshold trip-points for the comparators and pin naming conventions.

Digital Inputs: Digital input naming configurations and digital inputs feed into the internal PLD for the sequence controller.

Sequence Controller: Incorporates a PLD architecture for designing the state machine to control the order and functions associated with the user-defined power-up sequence/monitor and control.

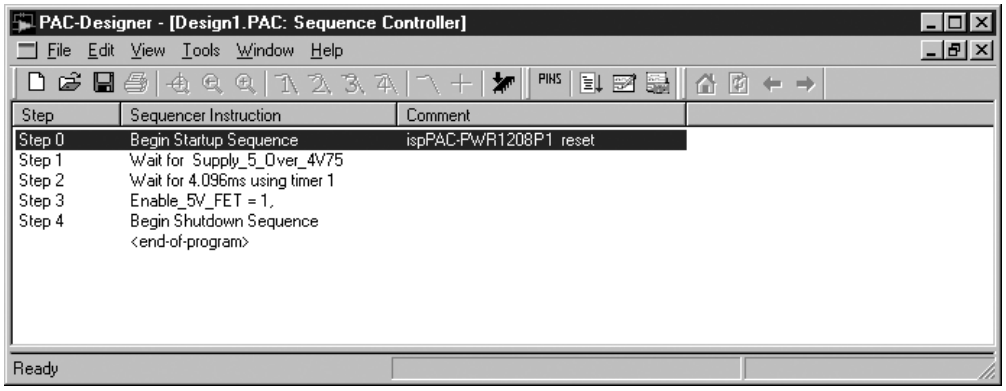
FET Drivers: Allows the user to define ramp rates by controlling the current driven to the gate of the external FETs. Maximum voltage levels and pin names are also set using this functional block. The four FET driver outputs HVOUT1-4 can also be configured as open-drain digital logic outputs.

Logic Outputs: These pins are configured and assigned in the Logic Output Functional Block. The four digital outputs are open-drain and require a pull-up resistor.

Internal Clock: The internal clock configuration and clock prescaler values are user-programmable, as well as the four internal programmable timers used for sequence delay.

User Electronic Signature (UES): Stores 16 bits of ID or board information in non-volatile E^2CMOS.

Figure 19. PAC-Designer LogiBuilder Screen



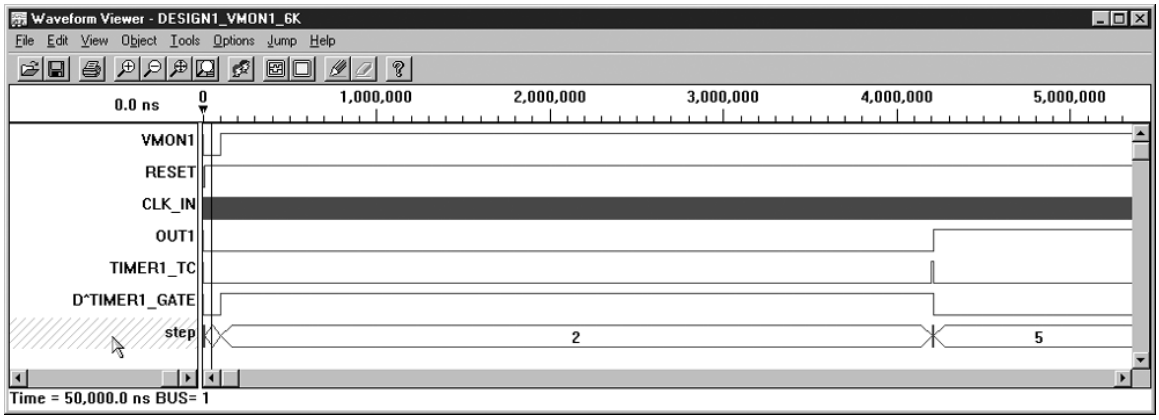
Programming of the ispPAC-POWR1208P1 is accomplished using the Lattice ispDOWNLOAD Cable. This cable connects to the parallel port of a PC and is driven through the PAC-Designer software. The software controls the JTAG TAP interface and shifts in the JEDEC data bits that set the configuration of all the analog and digital circuitry that the user has defined during the design process.

Power to the device must be set at 3.0V to 5.5V during programming, once the programming steps have been completed, the power supply to the ispPAC-POWR1208P1 can be set from 2.7V to 5.5V. Once programmed, the on-chip non-volatile E^2CMOS bits hold the entire design configuration for the digital circuits, analog circuits and trip points for comparators etc. Upon powering the device up, the non-volatile E^2CMOS bits control the device configuration. If design changes need to be made such as adjusting comparator trip points or changes to the digital logic functions, the device is simply re-programmed using the ispDOWNLOAD Cable.

Design Simulation Capability

Support for functional simulation of the control sequence is provided using the software tools Waveform Editor and Waveform Viewer. Both applications are spawned from the LogiBuilder environment of PAC-Designer. The simulation engine combines the design file with a stimulus file (edited by the user with Waveform Editor) to produce an output file that can be observed with the Waveform Viewer (Figure 20).

Figure 20. PAC-Designer Functional Simulation Screen



In-System Programming

The ispPAC-POWR1208P1 is an in-system programmable device. This is accomplished by integrating all E^{2}CMOS configuration memory and control logic on-chip. Programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E^{2}CMOS memory cells. The specifics of the IEEE 1149.1 serial interface and all ispPAC-POWR1208P1 instructions are described in the JTAG interface section of this data sheet.

User Electronic Signature

The User Electronic Signature (UES), allows the designer to include identification bits or serial numbers inside the device, stored in E^{2}CMOS memory. The ispPAC-POWR1208P1 contains 16 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Electronic Security

An Electronic Security Fuse (ESF) bit is provided to prevent unauthorized readout of the E^{2}CMOS bit pattern. Once programmed, this cell prevents further access to the functional user bits in the device. This cell can only be erased by reprogramming the device; this way the original configuration cannot be examined or copied once programmed. Usage of this feature is optional.

Production Programming Support

Once a final configuration is determined, an ASCII format JEDEC file can be created using the PAC-Designer software. Devices can then be ordered through the usual supply channels with the user's specific configuration already preloaded into the devices. By virtue of its standard interface, compatibility is maintained with existing production programming equipment, giving customers a wide degree of freedom and flexibility in production planning.

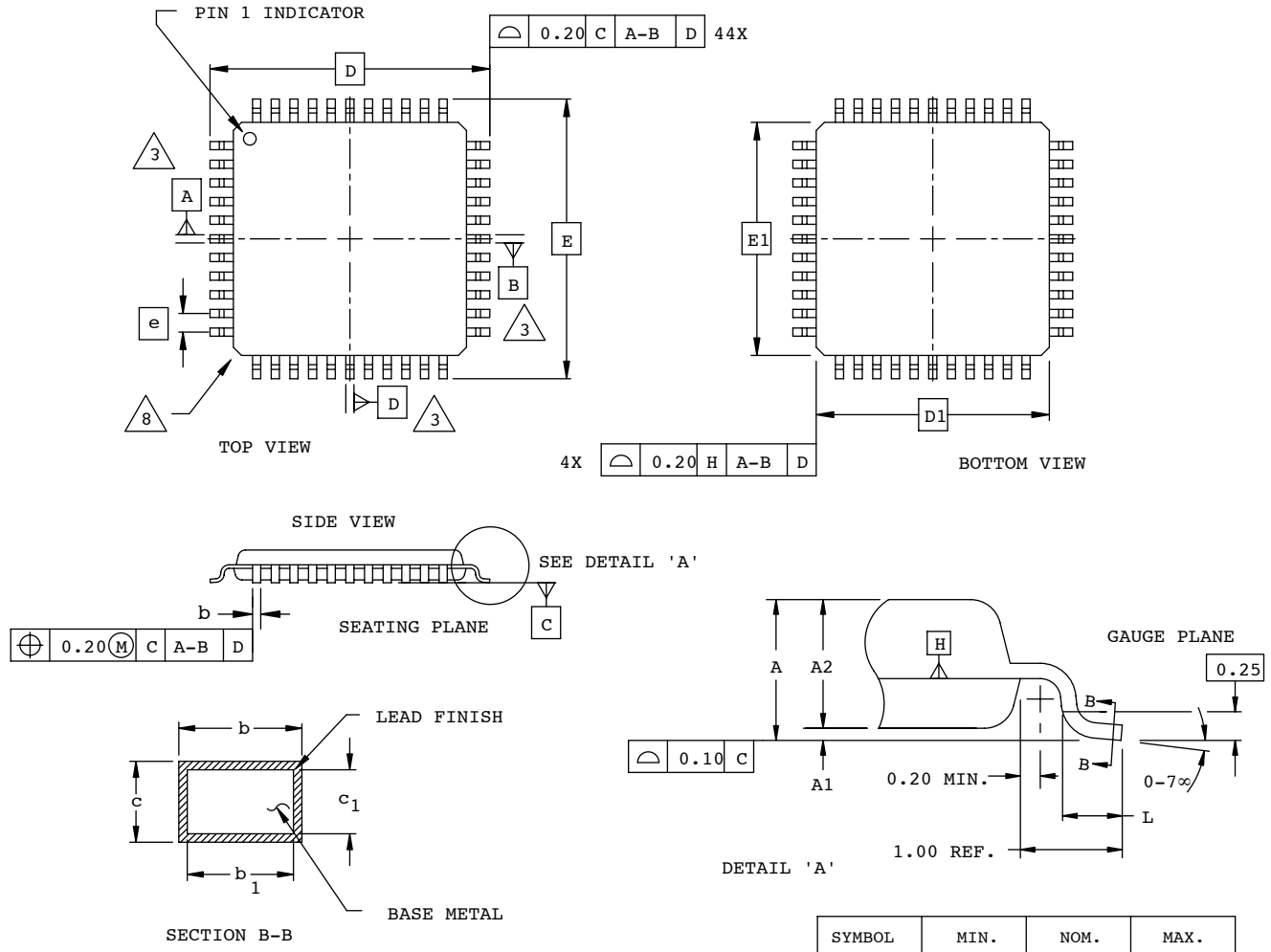
Part Number	Description
PAC-SYSPOWR1208P1	Complete system kit, evaluation board, ispDOWNLOAD Cable and software
PACPOWR1208P1-EV	Evaluation board only, with components, fully assembled

Evaluation Fixture

The ispPAC-POWR1208P1 Design Kit includes an engineering prototype board that can be connected to the parallel port of a PC using a Lattice ispDOWNLOAD cable. It demonstrates proper layout techniques for the ispPAC-POWR1208P1 and can be used in real time to check circuit operation as part of the design process. LEDs are supplied to debug designs without involving test equipment. Input and output connections as well as a "breadboard" circuit area are provided to speed debugging of the circuit. The board includes an area for prototyping other circuits and interconnect areas with pads for pins or cables. The user can check out designs on the hardware and make necessary changes to the design for the function required.

Package Diagrams

44-Pin TQFP (Dimensions in Millimeters)

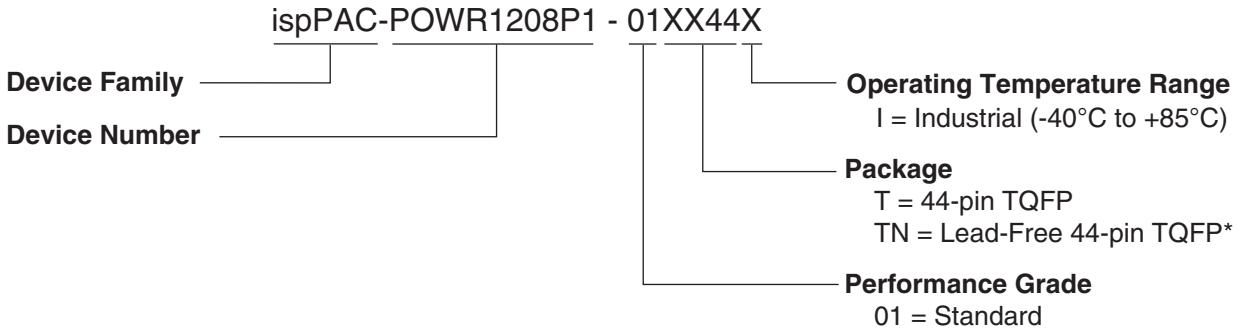


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
5. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MM.
6. SECTION B-B:
   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.
7. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
L	0.45	0.60	0.75
N		44	
e		0.80 BSC	
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
c	0.09	0.15	0.20
c1	0.09	0.13	0.16

Part Number Description



*Contact factory for package availability.

ispPAC-POWR1208P1 Ordering Information

Industrial

Part Number	Package	Pins
ispPAC-POWR1208P1-01T44I	TQFP	44

Lead-Free Industrial

Part Number	Package	Pins
ispPAC-POWR1208P1-01TN44I	Lead-free TQFP	44

Package Options