# MAXIM

# 12V/5V Hot-Plug Switch

*MAX34561*

## _____General Description

The MAX34561 is a dual, self-contained, hot-plug switch intended to be used on +12V and +5V power rails to limit through current and to control the power-up output-voltage ramp. The device contains two on-board n-channel power MOSFETs that are actively closed-loop controlled to ensure that an adjustable current limit is not exceeded. The maximum allowable current through the device is adjusted by external resistors connected between the LOAD and ILIM pins.

The device can control the power-up output-voltage ramp. Capacitors connected to the VRAMP pins set the desired voltage-ramp rate. The output voltages are unconditionally clamped to keep input overvoltage stresses from harming the load. The device also contains adjustable power-up timers. Capacitors connected to the TIMER pins determine how long after power-on reset (POR) the device should wait before starting to apply power to the loads. The TIMER pins can be driven with a digital logic output to create a device-enable function.

The device contains an on-board temperature sensor with hysteresis. If operating conditions cause the device to exceed an internal thermal limit, the device either unconditionally shuts down and latches off awaiting a POR, or waits until the device has cooled by the hysteresis amount and then restarts.

## _____Applications

RAID/Hard Drives

Servers/Routers

PCI/PCI Express®

InfiniBandTM/SM

Base Stations

## _____Features

♦ **Completely Integrated Hot-Plug Functionality for +12V and +5V Power Rails**

♦ **Dual Version of the DS4560**

♦ **On-Board Power MOSFETs (68m$\Omega$ and 43m$\Omega$)**

♦ **No High-Power R$_{SENSE}$ Resistors Needed**

♦ **Adjustable Current Limits**

♦ **Adjustable Output-Voltage Slew Rates**

♦ **Adjustable Power-Up Enable Timing**

♦ **Output Overvoltage Limiting**

♦ **On-Board Thermal Protection**

♦ **On-Board Charge Pump**

♦ **User-Selectable Latchoff or Automatic Retry Operation**

## _____Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX34561T+ | -40°C to +85°C | 24 TQFN-EP* |
| MAX34561T+T | -40°C to +85°C | 24 TQFN-EP* |

*+Denotes a lead(Pb)-free/RoHS compliant package.*
*T = Tape and reel.*
*\*EP = Exposed pad.*

*PCI Express is a registered trademark of PCI-SIG Corp.*

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***For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# 12V/5V Hot-Plug Switch

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on V$_{CC5}$ Relative to GND............-0.3V to +6.5V
Voltage Range on V$_{CC12}$ Relative to GND...........-0.3V to +18V
Voltage Range on ILIM5, VRAMP5,
   TIMER5, ARD5 Relative to GND.........-0.3V to (V$_{CC5}$ + 0.3V),
                                      not to exceed +6.5V
Voltage Range on ILIM12, VRAMP12
   Relative to GND ...............................-0.3V to (V$_{CC12}$ + 0.3V),
                                        not to exceed +18V
Voltage Range on TIMER12, ARD12
   Relative to GND .....................................-0.3V to +5V (V$_{REG}$)
5V Drain Current
  Continuous ...........................................................................2A
  Peak .....................................................................................4A

12V Drain Current
  Continuous ...........................................................................2A
  Peak .....................................................................................4A
Continuous Power Dissipation (T$_A$ = +70°C)
  TQFN (derate 20.8mW/°C above +70°C)...............1666.7mW
Operating Junction Temperature Range ......... -40°C to +135°C
Operating Temperature Range ........................ -40°C to +85°C
Storage Temperature Range ......................... -55°C to +135°C
Lead Temperature (soldering, 10s) ...............................+300°C
Soldering Temperature (reflow) .....................................+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING CONDITIONS

(T$_J$ = -40°C to +135°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| V$_{CC5}$ Voltage | V$_{CC5}$ | (Notes 1, 2) | 4.0 | 5.0 | 5.5 | V |
| V$_{CC12}$ Voltage | V$_{CC12}$ | (Notes 1, 2) | 9 | 12 | 13.2 | V |
| R$_{ILIM\_}$ Value | R$_{ILIM\_}$ | | 20 | | 400 | Ω |
| C$_{VRAMP\_}$ Value | C$_{VRAMP\_}$ | | 0.04 | | 5 | µF |
| C$_{TIMER\_}$ Value | C$_{TIMER\_}$ | | 0.04 | | 5 | µF |
| TIMER_ Turn-On Voltage | V$_{ON}$ | TIMER5 | 2.1 | | V$_{CC5}$ + 0.3 | V |
| | | TIMER12 | 2.6 | | 5.0 | |
| TIMER_ Turn-Off Voltage | V$_{OFF}$ | | -0.3 | | +1.5 | V |

## ELECTRICAL CHARACTERISTICS

(V$_{CC5}$ = +5V, V$_{CC12}$ = +12V, T$_J$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| V$_{CC5}$ Supply Current | I$_{CC5}$ | (Note 3) | | 1.5 | 2 | mA |
| V$_{CC12}$ Supply Current | I$_{CC12}$ | (Note 3) | | 1.5 | 2.25 | mA |
| 5V UVLO: Rising | V$_{UR5}$ | | | 3.7 | 3.95 | V |
| 5V UVLO: Falling | V$_{UF5}$ | | 2.7 | 3.2 | | V |
| 5V UVLO: Hysteresis | V$_{UH5}$ | | | 0.5 | | V |
| 12V UVLO: Rising | V$_{UR12}$ | | | 8 | 8.5 | V |
| 12V UVLO: Falling | V$_{UF12}$ | | 6.5 | 7 | | V |
| 12V UVLO: Hysteresis | V$_{UH12}$ | | | 1 | | V |
| 5V On-Resistance | R$_{ON5}$ | | | 43 | 56 | mΩ |
| 12V On-Resistance | R$_{ON12}$ | | | 68 | 88 | mΩ |
| 5V Internal Voltage Reference | V$_{REF5}$ | | | 1.80 | | V |
| 12V Internal Voltage Reference | V$_{REF12}$ | | | 2.35 | | V |

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## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC5}$ = +5V, $V_{CC12}$ = +12V, $T_J$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| 5V MOSFET Output Capacitance | $C_{OUT}$ | (Note 4) | | 400 | | pF |
| 12V MOSFET Output Capacitance | $C_{OUT}$ | (Note 4) | | 400 | | pF |
| 5V and 12V Delay Time from Enable to Beginning of Conduction | $t_{POND}$ | $C_{VRAMP\_}$ = 1µF | | 8 | | ms |
| 5V and 12V Gate-Charging Time from Conduction to 90% of $V_{OUT}$ | $t_{GCT}$ | $C_{VRAMP\_}$ = 1µF, $C_{LOAD\_}$ = 1000µF | 48 | 64 | 80 | ms |
| Shutdown Junction Temperature | $T_{SHDN}$ | (Note 4) | 120 | 135 | 150 | °C |
| Thermal Hysteresis | $T_{HYS}$ | (Note 4) | | 40 | | °C |
| TIMER_ Charging Current | $I_{TIMER}$ | | 64 | 80 | 96 | µA |
| VRAMP_ Charging Current | $I_{VRAMP}$ | | 64 | 80 | 96 | µA |
| 5V Overvoltage Clamp | $V_{OVC5}$ | | 5.5 | 6.0 | 6.5 | V |
| 12V Overvoltage Clamp | $V_{OVC12}$ | | 13.2 | 15 | 16.5 | V |
| 5V Power-On Short-Circuit Current Limit | $I_{SCL5}$ | $R_{ILIM5}$ = 47Ω (Note 5) | 0.6 | 1.0 | 1.5 | A |
| 12V Power-On Short-Circuit Current Limit | $I_{SCL12}$ | $R_{ILIM12}$ = 47Ω (Note 5) | 0.6 | 1.0 | 1.5 | A |
| 5V Operating Overload Current Limit | $I_{OVL5}$ | $R_{ILIM5}$ = 47Ω (Notes 4, 6) | 1.5 | 2.5 | 3.7 | A |
| 12V Operating Overload Current Limit | $I_{OVL12}$ | $R_{ILIM12}$ = 47Ω (Notes 4, 6) | 1.00 | 1.8 | 2.6 | A |
| 5V VRAMP5 Slew Rate | $SR_{VRAMP}$ | $C_{VRAMP5}$ = 1µF | 0.16 | 0.19 | 0.23 | V/ms |
| 12V VRAMP12 Slew Rate | $SR_{VRAMP}$ | $C_{VRAMP12}$ = 1µF | 0.13 | 0.15 | 0.18 | V/ms |
| ARD5 Pullup Resistor | $R_{PU5}$ | | | 100 | | kΩ |
| ARD12 Pullup Resistor | $R_{PU12}$ | | | | | kΩ |

**Note 1:** All voltages are referenced to ground. Currents entering the device are specified positive, and currents exiting the device are negative.
**Note 2:** This supply range guarantees that the LOAD_ voltage is not clamped by the overvoltage limit.
**Note 3:** Supply current specified with no load on the LOAD_ pin.
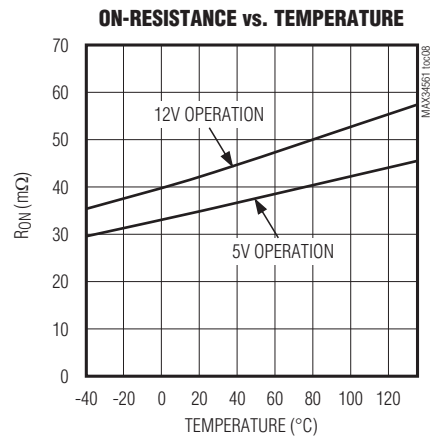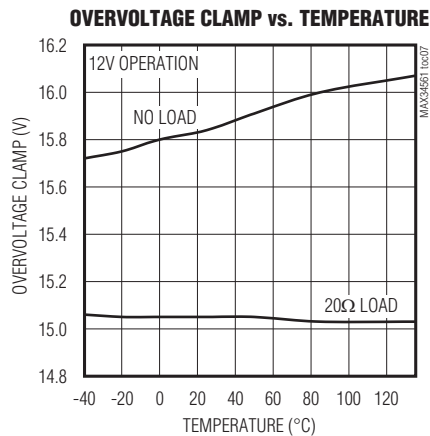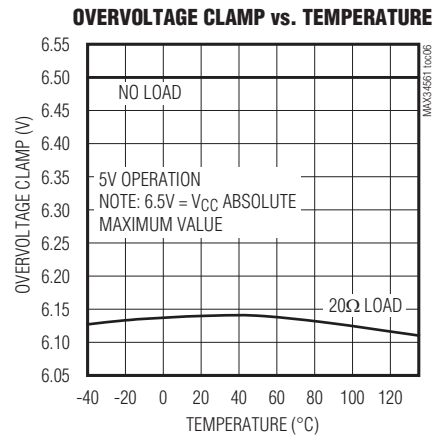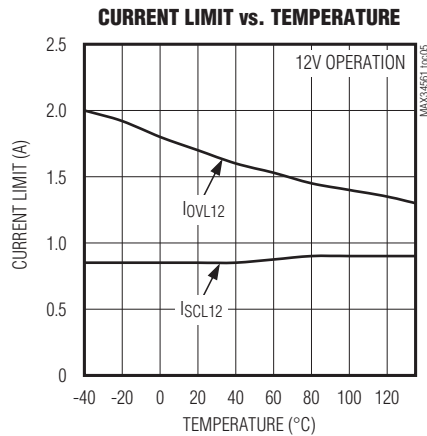**Note 4:** Guaranteed by design; not production tested.
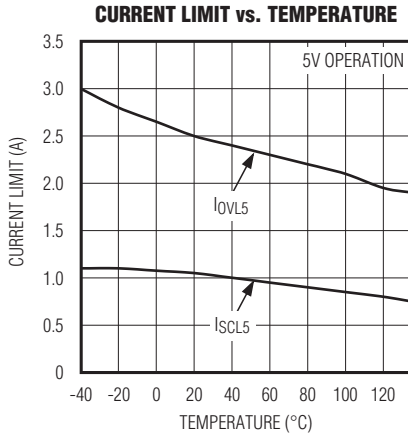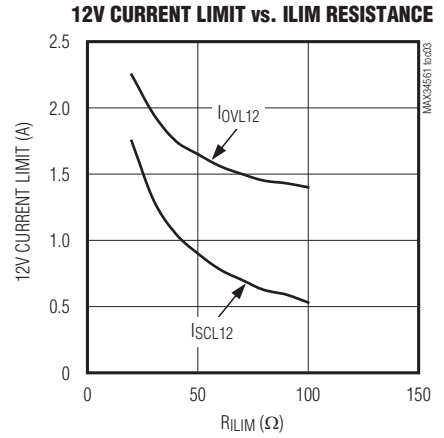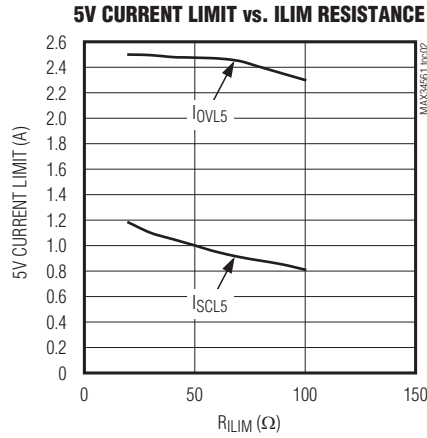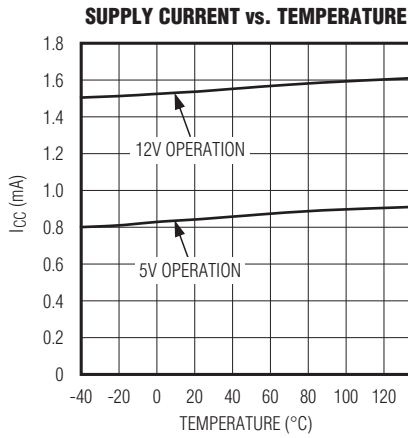**Note 5:** $I_{SCL\_}$ is the current limit when conduction begins.
**Note 6:** $I_{OVL\_}$ is the current limit after the on-board MOSFET is fully on.

# 12V/5V Hot-Plug Switch

## Typical Operating Characteristics
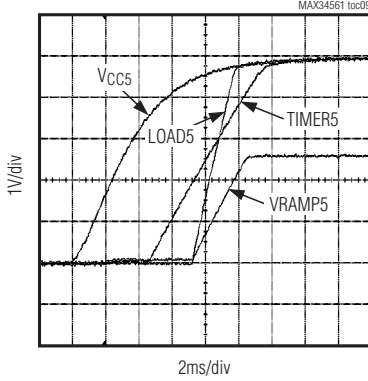
($T_A$ = +25°C, unless otherwise noted.)

### SUPPLY CURRENT vs. TEMPERATURE



### 5V CURRENT LIMIT vs. ILIM RESISTANCE



### 12V CURRENT LIMIT vs. ILIM RESISTANCE



### CURRENT LIMIT vs. TEMPERATURE



### CURRENT LIMIT vs. TEMPERATURE



### OVERVOLTAGE CLAMP vs. TEMPERATURE



### OVERVOLTAGE CLAMP vs. TEMPERATURE



### ON-RESISTANCE vs. TEMPERATURE



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## Typical Operating Characteristics (continued)

(T$_A$ = +25°C, unless otherwise noted.)

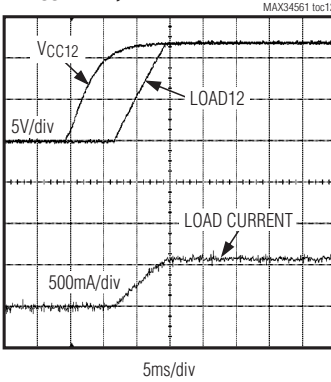**TYPICAL MAX34561 TURN-ON WAVEFORMS**
**V$_{CC}$ = 5V, 20Ω RESISTIVE LOAD**

MAX34561 toc09

1V/div

V$_{CC5}$
LOAD5
TIMER5
VRAMP5

2ms/div

**TYPICAL MAX34561 TURN-ON WAVEFORMS**
**V$_{CC}$ = 12V, 20Ω RESISTIVE LOAD**

MAX34561 toc10

2V/div

V$_{CC12}$
LOAD12
VRAMP12
TIMER12

5ms/div

**TURN-ON WAVEFORMS**
**V$_{CC}$ = 5V, 20Ω RESISTIVE LOAD**

MAX34561 toc11

V$_{CC5}$
LOAD5
2V/div

LOAD CURRENT
500mA/div

5ms/div

**TURN-ON WAVEFORMS**
**V$_{CC}$ = 12V, 20Ω RESISTIVE LOAD**

MAX34561 toc12

V$_{CC12}$
LOAD12
5V/div

LOAD CURRENT
500mA/div

5ms/div
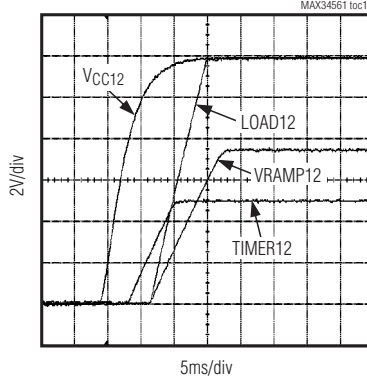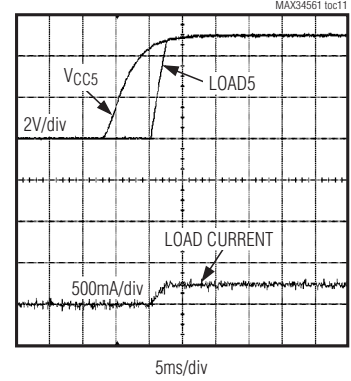
**TURN-ON WAVEFORMS**
**V$_{CC}$ = 5V, 3300µF CAPACITIVE LOAD**

MAX34561 toc13

V$_{CC5}$
LOAD5
2V/div

LOAD CURRENT
500mA/div

5ms/div
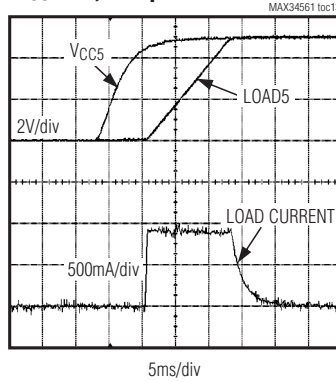
**TURN-ON WAVEFORMS**
**V$_{CC}$ = 12V, 3300µF CAPACITIVE LOAD**

MAX34561 toc14

V$_{CC12}$
LOAD12
5V/div

LOAD CURRENT
500mA/div

10ms/div
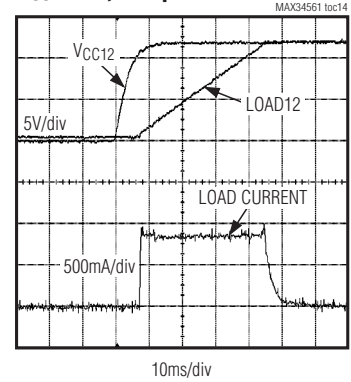
**THERMAL SHUTDOWN WITH AUTORETRY ENABLED**
**V$_{CC}$ = 5V, 2Ω RESISTIVE LOAD**

MAX34561 toc15

V$_{CC5}$
2V/div
LOAD5
LOAD CURRENT
500mA/div

1s/div
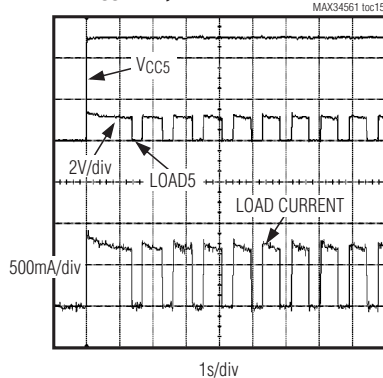
**THERMAL SHUTDOWN WITH AUTORETRY ENABLED**
**V$_{CC}$ = 12V, 2Ω RESISTIVE LOAD**

MAX34561 toc16

V$_{CC12}$
LOAD12
5V/div
LOAD CURRENT
500mA/div

500ms/div

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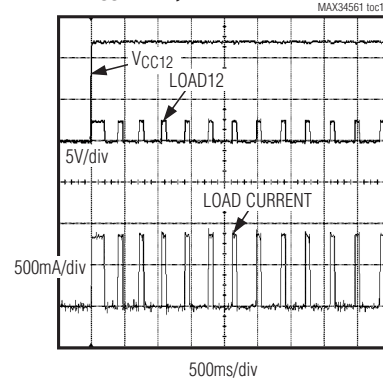
# 12V/5V Hot-Plug Switch

## Pin Configuration



TOP VIEW

MAX34561

THIN QFN
(4mm × 4mm)
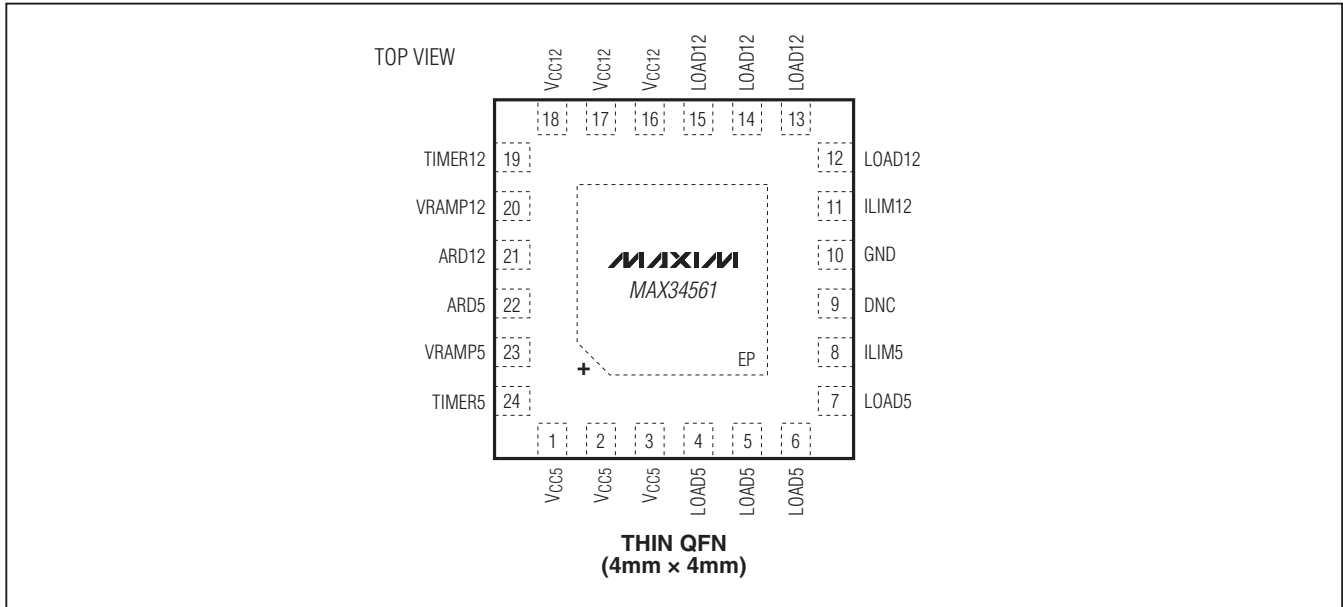
## Pin Description

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 1, 2, 3 | $V_{CC5}$ | 5V Supply Input. Power-supply input and n-channel power MOSFET drain connection. If the 5V side is not used, connect this pin to GND. |
| 4–7 | LOAD5 | 5V Load Output. n-channel power MOSFET source connection. |
| 8 | ILIM5 | 5V Supply Current-Limit Adjust. A resistor from this pin to LOAD5 determines the current limit for the 5V pass connection. For better accuracy, dedicate one LOAD pin to connect to ILIM through $R_{ILIM}$. See the *Applications Information* section for more information. |
| 9 | DNC | Do Not Connect. Do not connect any signal to this pin. |
| 10 | GND | Ground Connection |
| 11 | ILIM12 | 12V Supply Current-Limit Adjust. A resistor from this pin to LOAD12 determines the current limit for the 12V pass connection. For better accuracy, dedicate one LOAD pin to connect to ILIM through $R_{ILIM}$. See the *Applications Information* section for more information. |
| 12–15 | LOAD12 | 12V Load Output. n-channel power MOSFET source connection. |
| 16, 17, 18 | $V_{CC12}$ | 12V Supply Input. Power-supply input and n-channel power MOSFET drain connection. If the 12V side is not used, connect this pin to GND. |
| 19 | TIMER12 | 12V Enable Delay Control. A capacitor connected to this pin determines the enable delay according to the equation: Enable Delay = $C_{TIMER12}$ x ($V_{REF12}/I_{TIMER}$). |
| 20 | VRAMP12 | 12V Voltage Ramp Control. A capacitor connected to this pin determines the voltage ramp of the LOAD12 output during turn-on according to the equation: $dV_{LOAD12}$ = 2 x ($I_{VRAMP}/C_{VRAMP12}$). |
| 21 | ARD12 | 12V Autoretry Disable. Connect this pin to GND to disable automatic retry functionality; the device latches off during an overtemperature fault. Leave this pin open to enable automatic retry function. This pin contains a pullup ($R_{PU12}$) to 5V. This pin is only sampled on device power-on. If the 12V side is not used, connect this pin to GND. |

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| PIN | NAME | FUNCTION |
|---|---|---|
| 22 | ARD5 | 5V Autoretry Disable. Connect this pin to GND to disable automatic retry functionality; the device latches off during an overtemperature fault. Leave this pin open to enable automatic retry function. This pin contains a pullup ($R_{PU5}$) to $V_{CC5}$. This pin is only sampled on device power-on. If the 5V side is not used, connect this pin to GND. |
| 23 | VRAMP5 | 5V Voltage Ramp Control. A capacitor connected to this pin determines the voltage ramp of the LOAD5 output during turn-on according to the equation: $dV_{LOAD5} = 2.3332 \times (I_{VRAMP}/C_{VRAMP5})$. |
| 24 | TIMER5 | 5V Enable Delay Control. A capacitor connected to this pin determines the enable delay according to the equation: Enable Delay = $C_{TIMER5} \times (V_{REF5}/I_{TIMER})$. |
| — | EP | Exposed Pad. Connect to ground. The EP must be soldered to ground for proper thermal and electrical operation. |

## Detailed Description

The MAX34561 has hot-plug controls for both +12V and +5V power rails. The circuitry for the +12V and +5V controls are independent of each other and can be treated as two separate hot-plug switches, even though the GND pin is common between the two switches. The sections that follow are written from the +12V circuit perspective, but also apply for the +5V switch control.

The device begins to operate when the supply voltage $V_{CC12}$ (or $V_{CC5}$) exceeds its undervoltage lockout level, $V_{UR12}$ (or $V_{UR5}$). At this level, the corresponding enable circuit and TIMER12 (TIMER5) become active. Once the device has been enabled, a gate voltage is applied to the corresponding power MOSFET, allowing current to begin flowing from $V_{CC12}$ ($V_{CC5}$) to LOAD12 (LOAD5). The speed of the output-voltage ramp is controlled by the capacitance placed at the VRAMP12 (VRAMP5) pin. The load current is continuously monitored during the initial conduction ($I_{SCL12}$ or $I_{SCL5}$) and after the corresponding MOSFET is fully on ($I_{OVL12}$ or $I_{OVL5}$). If the current exceeds the current limit that is set by the external resistance at ILIM12 (ILIM5), the gate voltage of the corresponding power MOSFET is decreased, reducing the output current to the set current limit.

Current is limited by the device comparing the voltage difference between LOAD12 (LOAD5) and ILIM12 (ILIM5) to an internal reference voltage. If the output current exceeds the limit that is set by the $R_{ILIM12}$ ($R_{ILIM5}$) resistor, the gate voltage of the corresponding power MOSFET is decreased, which reduces the output current to the load.

When the output power is initially ramping up, the current limit is $I_{SCL12}$ ($I_{SCL5}$). Once the corresponding MOSFET is fully on, the current limit is $I_{OVL12}$ ($I_{OVL5}$). The $I_{SCL12}$ ($I_{SCL5}$) current limit protects the source if there is a dead short on initial power-up.

The device acts as a fuse and automatically disables the current flowing to the load when the temperature of the power corresponding MOSFET has exceeded the shutdown junction temperature, $T_{SHDN}$.
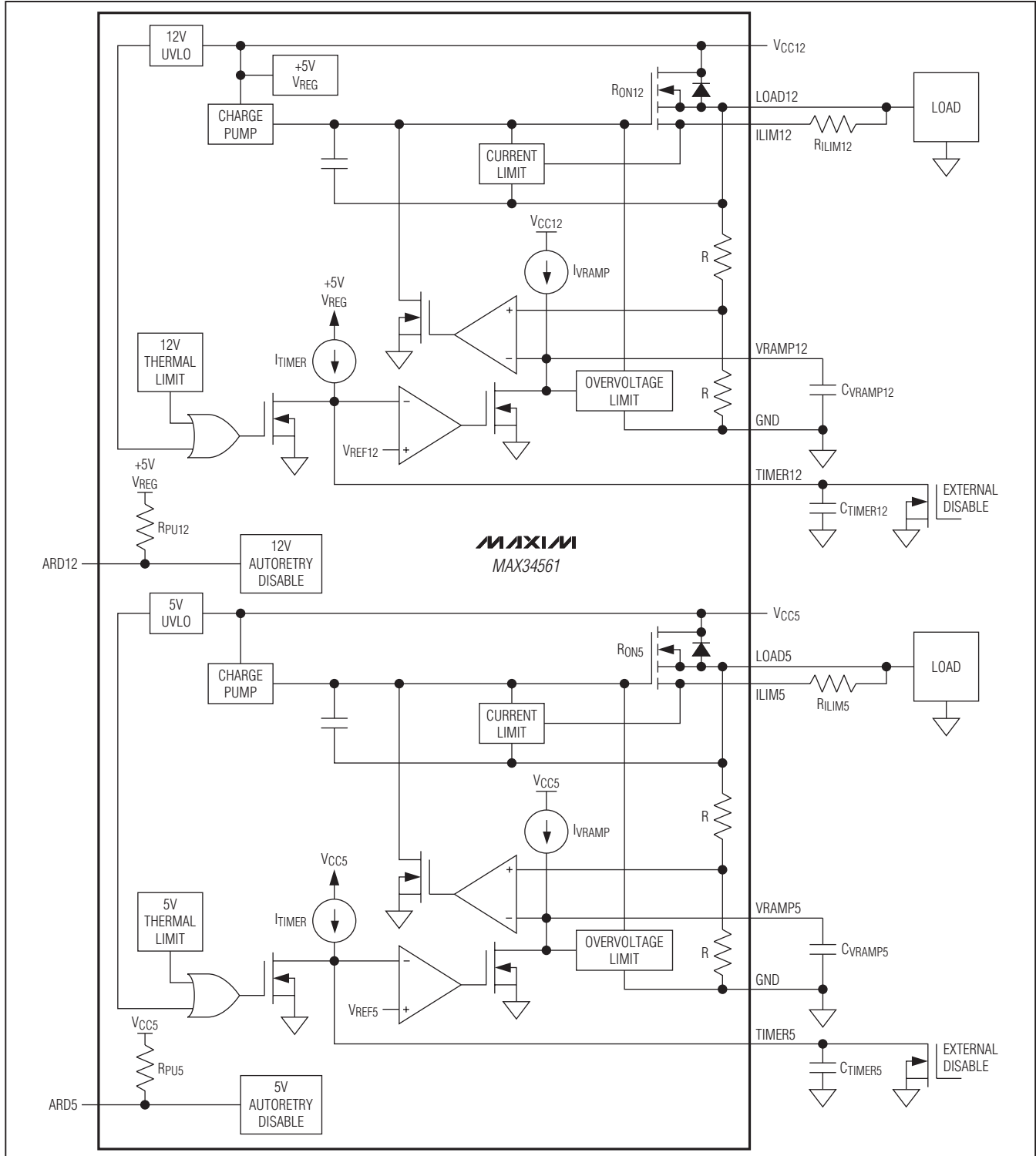
### Enable/Timer

The voltage level of TIMER12 (TIMER5) is compared to an internal source (see the *Functional Diagram*). When the level on the pin exceeds $V_{ON}$, the comparator outputs a low level. This then turns on the voltage ramp circuit, enabling the device's output. TIMER12 (TIMER5) can be configured into one of four different modes of operation as listed in Table 1. TIMER12 (TIMER5) pin was designed to work with most logic families. TIMER12 (TIMER5) has at least 250mV of hysteresis between $V_{ON}$ and $V_{OFF}$. It is recommended that any logic gate used to drive TIMER12 (TIMER5) be tested to ensure proper operation.

## Table 1. TIMER_ Pin Modes

| OPERATION MODE | TIMER PIN SETUP |
|---|---|
| Automatic Enable | No connection to TIMER12 (TIMER5) |
| Delayed Automatic Enable | Capacitor $C_{TIMER\_}$ connected to TIMER12 (TIMER5) |
| Enable/Disable | Open-collector device |
| Enable with Delay/Disable | Open-collector device and $C_{TIMER\_}$ |

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# 12V/5V Hot-Plug Switch

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Once the device has been enabled, there is a delay ($t_{POND}$) until conduction begins from $V_{CC12}$ ($V_{CC5}$) to LOAD12 (LOAD5). This delay is the time required for the charge pump to bring the gate voltage of the corresponding power MOSFET above its threshold level. Once the gate is above the threshold level, conduction begins and the output voltage begins ramping.

### Automatic-Enable Mode

When $V_{CC12}$ ($V_{CC5}$) exceeds $V_{UR12}$ ($V_{UR5}$), the gate holding the TIMER12 (TIMER5) node low is released. The internal current source brings the node to a level greater than $V_{ON}$, enabling the device.

### Delayed Automatic-Enable Mode

When $V_{CC12}$ ($V_{CC5}$) exceeds $V_{UR12}$ ($V_{UR5}$), the gate holding the TIMER12 (TIMER5) node low is released. The internal current source ($I_{TIMER}$) then begins charging $C_{TIMER\_}$. When $C_{TIMER\_}$ is charged to a level greater than $V_{REF12}$ ($V_{REF5}$), the device turns on. The equation for the delay time is:

$$t_{DELAY} = (C_{TIMER12} \times V_{REF12})/I_{TIMER}$$

$$t_{DELAY} = (C_{TIMER5} \times V_{REF5})/I_{TIMER}$$

### Enable/Disable Mode

A logic gate or open-collector device can be connected to TIMER12 (TIMER5) to enable or disable the device. When TIMER12 (TIMER5) is held low, the device is disabled. When an open-collector device is used to drive TIMER12 (TIMER5), the device is enabled when the open collector is in its high-impedance state by the internal current source bringing the TIMER12 (TIMER5) node high. TIMER12 (TIMER5) is also compatible with most logic families if the output high voltage level of the gate exceeds the $V_{ON}$ level, and the gate can sink the $I_{TIMER}$ current.

### Enable with Delay/Disable Mode

An open-collector device is connected in parallel with $C_{TIMER\_}$. When the pin is held low, the device is disabled. When the open-collector driver is high impedance, the internal current source begins to charge $C_{TIMER\_}$ as in the delayed mode.

### Output-Voltage Ramp

The voltage ramp circuit uses an operational amplifier to control the gate bias of the corresponding n-channel power MOSFET. When the timer/enable circuit is disabled, a FET is used to keep $C_{VRAMP\_}$ discharged, which forces the output voltage to GND. Once the enable/timer circuit has been enabled, an internal current source, $I_{VRAMP}$, begins to charge the external capacitor, $C_{VRAMP\_}$, connected to VRAMP12 (VRAMP5). The amplifier controls the gate of the corresponding power MOSFET so that the LOAD12 (LOAD5) output voltage divided by two tracks the rising voltage level of $C_{VRAMP\_}$. The output voltage continues to ramp until it reaches either the input $V_{CC12}$ ($V_{CC5}$) level or the overvoltage clamp limits. The equation for the output-voltage ramp function is:

$$dV_{LOAD}/dt = 2 \times (I_{VRAMP}/C_{VRAMP12}) \text{ for +12V circuit}$$

$$dV_{LOAD}/dt = 2.3332 \times (I_{VRAMP}/C_{VRAMP5}) \text{ for +5V circuit}$$

### Thermal Shutdown

The device enters a thermal shutdown state when the temperature of the corresponding power MOSFET reaches or exceeds $T_{SHDN}$, approximately +135°C. When $T_{SHDN}$ is exceeded, the thermal-limiting circuitry disables the device using the enable circuitry. Depending on the state of ARD12 (ARD5), the device attempts to autoretry once the device has cooled, or it latches off.

### Autoretry

If ARD12 (ARD5) is unconnected or connected high, the device continually monitors the temperature once it has entered thermal shutdown. If the junction temperature falls below approximately +95°C ($T_{SHDN}$ - $T_{HYS}$), the corresponding power MOSFET is re-enabled. See the Thermal Shutdown with Autoretry Enabled typical operating curves for details.

### Latchoff

If ARD12 (ARD5) is pulled low and the device has entered thermal shutdown, it does not attempt to turn back on. The only way to turn the device back on is to cycle the power to the device. When power is reapplied to $V_{CC12}$ ($V_{CC5}$), the junction temperature needs to be less than $T_{SHDN}$ for the device to be enabled.

### Overvoltage Limit

The overvoltage-limiting clamp monitors the VRAMP12 (VRAMP5) level compared to an internal voltage reference. When the voltage on VRAMP12 (VRAMP5) exceeds $V_{OVC12}/2$ (or $V_{OVC5}/2.3332$), the gate voltage of the corresponding n-channel power MOSFET is reduced, limiting the voltage on LOAD12 (LOAD5) to $V_{OVC12}$ ($V_{OVC5}$) even as $V_{CC12}$ ($V_{CC5}$) increases. If the device is in overvoltage for an extended period of time, the device could overheat and enter thermal shutdown. This is caused by the power created by the voltage

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drop across the corresponding power MOSFET and the load current. See the Thermal Shutdown with Autoretry Enabled typical operating curves for details.

## Applications Information

### Exposed Pad

The exposed pad is also a heatsink for the device. The exposed pad should be connected to a large trace or plane capable of dissipating heat from the device.

### Decoupling Capacitors

It is of utmost importance to properly bypass the device's supply pins. A decoupling capacitor absorbs the energy stored in the supply and board parasitic inductance when the FET is turned off, thereby reducing the magnitude of overshoot at $V_{CC}$. This can be accomplished by using a high-quality (low ESR, low ESL) ceramic capacitor connected directly between the $V_{CC}$ and GND pins. Any series resistance with this bypass capacitor lowers its effectiveness and is not recommended. A minimum 0.5µF ceramic capacitor is required. However, depending on the parasitic inductances present in the end application, a larger capacitor could be necessary.
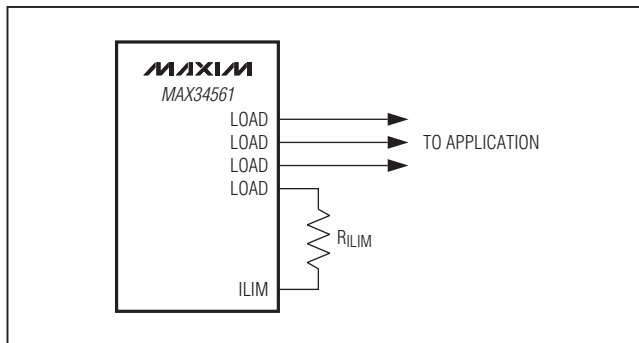


*Figure 1. LOAD and ILIM Connections*

### Unused Pins

If only one side (5V or 12V) of the device is being used, it is required that the unused $V_{CC}$, AR, CTIMER, and VRAMP pins be connected to GND. Leaving these input pins unconnected can result in interference of the proper operation of the active portion of the device.

### LOAD and ILIM Connections

Small parasitic resistances in the bond wires of the LOAD pins and in the traces connected to the LOAD pins can result in a voltage offset while current is flowing. Since the voltage drop across RILIM is used to set the $I_{SCL}$ and $I_{OVL}$ limits, this induced offset can increase the value of $I_{SCL}$ and $I_{OVL}$ from the specified values for any given $R_{ILIM}$. To greatly reduce this offset, it is recommended that one of the LOAD pins have a dedicated connection to ILIM though $R_{ILIM}$, and not be used to pass the LOAD current (Figure 1). This would leave three LOAD pins to pass $I_{LOAD}$, which should be sufficient. Because there is only a small amount of current passed from this lone LOAD pin to ILIM, there is a negligible voltage offset applied to the internal comparator. This method is the best way to attain an accurate current limit for $I_{LOAD}$.

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 24 TQFN-EP | T2444+4 | **21-0139** | **90-0022** |

# 12V/5V Hot-Plug Switch

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 11/10 | Initial release | — |

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