19-5819; Rev 0; 3/11

EVALUATION KIT AVAILABLE

MAX14895E

Enhanced VGA Port Protector

General Description

The MAX14895E integrates level-translating buffers and features RED, GRN, and BLU (RGB) port protection for VGA signals.

The device has horizontal sync (SYNCH_) and vertical sync (SYNCV_) translating buffers that convert low-level CMOS inputs from a graphics controller to meet full 5V, TTL-compatible outputs. Each output can drive ±10mA and meets the VESA℠ specification. In addition, the device translates the direct digital control (DDC) signals to a lower level that is safe for the graphics controller.

The device features both EN and $\overline{EN}$ inputs, accepting active-high or active-low enable inputs. The device also switches and current limits the 5V supply to a VGA connector or monitor.

The RED, GRN, and BLU terminals protect graphics controller outputs against electrostatic discharge (ESD) events. All eight outputs and $\overline{EN}$ have high-level ESD protection.

The MAX14895E is specified over the extended -40°C to +85°C temperature range and is available in a 16-pin, 3mm x 3mm TQFN package with exposed pad.

Applications

Notebook Computers	Servers
Desktops	Graphics Cards

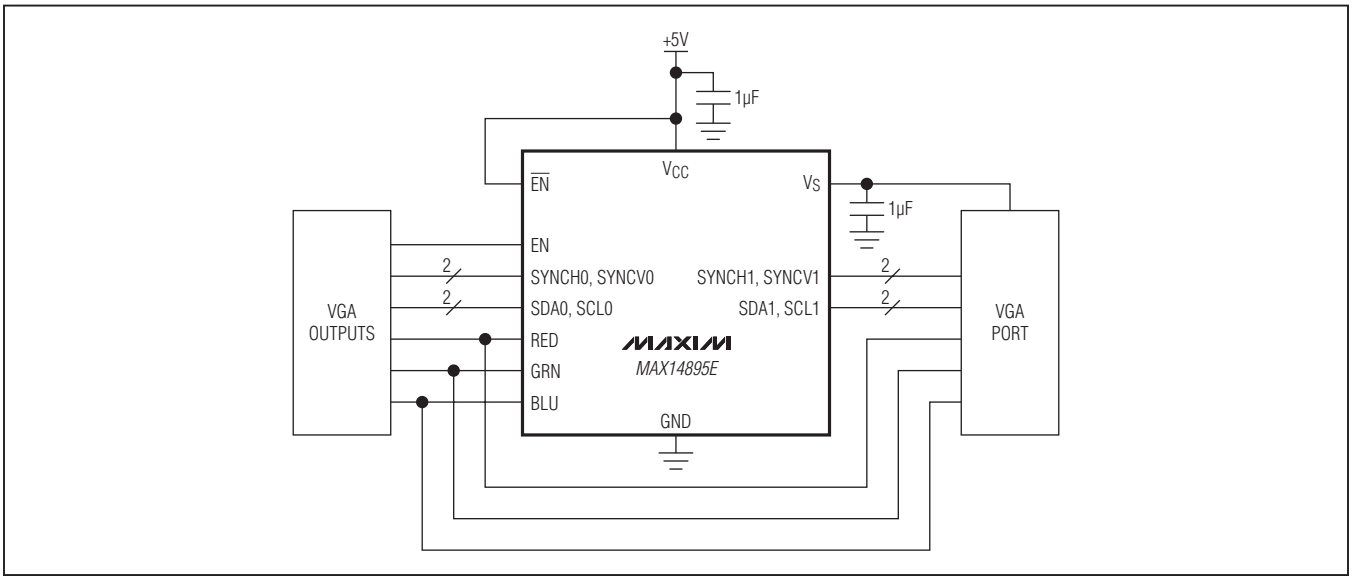
Benefits and Features

- **Saves Power in Portable Applications**
  - **Low Quiescent Supply Current: 430µA (typ)**
- **Eliminates Need for Costly External Components**
  - **High-ESD Protection on SDA1, SCL1, SYNCH1, SYNCV1, RED, GRN, BLU, $\overline{EN}$, V_S**
  - **±15kV Human Body Model (HBM)**
  - **±8kV IEC 61000-4-2 Contact Discharge**
- **Innovative Design Enables a High Level of Integration for Performance**
  - **Output Current-Limit Switch with Power-Off Protection**
  - **Low Capacitance on RGB Ports (2.2pF typ)**
  - **±10mA Drive on SYNCH1, SYNCV1**
- **Fully Integrated Solutions Saves Space in Portable Applications**
  - **DDC Outputs have Internal Pullups**
  - **3mm x 3mm, 16-Pin TQFN Package**

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX14895E.related**.*

Typical Operating Circuit



VESA is a service mark of the Video Electronics Standards Association Corporation.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC}, V_S, EN, SDA0, SCL0 .....-0.3V to +6V
SDA1, SCL1 ..... -0.3V to (V_S + 0.3V)
$\overline{EN}$, RED, GRN, BLU, SYNCH0,
SYNCH1, SYNCV0, SYNCV1..... -0.3V to (V_{CC} + 0.3V)
Continuous Current through SDA_, SCL_ ..... ±30mA
Continuous Short-Circuit Current SYNCH1, SYNCV1 ..... ±20mA

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 20.8mW/°C above +70°C).....1667mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS*

(V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range	V_{CC}		4.75		5.25	V
Quiescent Supply Current	I_Q	EN = V_{CC}, $\overline{EN}$ = GND, SYNCH0 = SYNCV0 = GND, SDA0 = SCL0 = unconnected		430	800	µA
Shutdown Supply Current	I_{SHDN}	EN = GND, $\overline{EN}$ = V_{CC}, SYNCH0 = SYNCV0 = GND, SDA0 = SCL0 = unconnected			8	µA
Undervoltage Lockout Threshold	V_{UVLO}	V_{CC} rising			4.3	V
Undervoltage Lockout Hysteresis				0.1		V
Internal Logic Supply Voltage	V_L	V_{CC} = +4.75V to +5.25V, SDA1/SCL1 = unconnected, measure SDA0/SCL0	1.6		2.9	V
		V_{CC} = +4.75V to +5.25V, SDA0/SCL0 = 200kΩ to GND, measure SDA0/SCL0, SDA1/SCL1 = unconnected	1.6		2.8	
RED, GRN, BLU						
RED, GRN, BLU Capacitance	C_{OUT}	f = 1MHz, $V_{RED, GRN, BLU}$ = $1V_{P-P}$		2.2		pF
RED, GRN, BLU Leakage Current			-1		+1	µA
SYNCH0, SYNCV0, EN, $\overline{EN}$						
Input Logic-High	V_{IH}		2.0			V
Input Logic-Low	V_{IL}				0.8	V

**The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

ELECTRICAL CHARACTERISTICS* (continued)

(V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCH0, SYNCV0 Leakage Current		SYNCH0/SYNCV0 = GND or V_{CC}	-1		+1	µA
EN, $\overline{EN}$ Input Resistance		EN = V_{CC}, $\overline{EN}$ = GND	200		800	kΩ
SYNCH1, SYNCV1						
Output Logic-High	V_{OH}	V_{CC} = +4.75V, source 10mA	2.4			V
Output Logic-Low	V_{OL}	V_{CC} = +4.75V, sink 10mA			0.5	V
Rising Time	t_R	R_L = 2.2kΩ, C_L = 10pF, 10% to 90% of V_{CC} (Note 3)			4	ns
Falling Time	t_F	R_L = 2.2kΩ, C_L = 10pF, 90% to 10% of V_{CC} (Note 3)			4	ns
Propagation Delay	t_{PD}	R_L = 2.2kΩ, C_L = 10pF, EN = V_{CC}, $\overline{EN}$ = GND (Figure 1)		16		ns
Enable Time	t_{EN}	R_L = 2.2kΩ, C_L = 10pF, V_{SYNCH1}, V_{SYNCV1} = +4.75V (Figure 1)		17		µs
SDA_, SCL_ (DDC)						
On-Resistance	R_{ON}	V_{SDA0} = V_{SCL0} = 0.5V, I_{LOAD} = 10mA			55	Ω
SDA0, SCL0 Off-Leakage Current		EN = GND, $\overline{EN}$ = V_{CC}, SDA0 = SCL0 = V_{CC}, SDA1 = SCL1 = GND	-1		+1	µA
SDA1, SCL1 Reverse-Leakage Current		V_{CC} = 0V, V_S = +5.25V, V_{SDA1} = V_{SCL1} = +5.25V	-10		+10	µA
SDA1, SCL1 Pullup Resistor	R_{PULLUP}	V_{CC} = +4.75V, SDA0 = SCL0 = unconnected, EN = V_{CC} , $\overline{EN}$ = GND, I_{LOAD} = 100µA	1.25	2.5	4.0	kΩ
V_S OUTPUT						
Forward Voltage Drop		I_{LOAD} = 60mA, V_{CC} = 5V			0.25	V
Reverse-Leakage Current		V_{CC} = 0V, V_S = 5.25V			10	µA
Current Limit	I_{LIM}		200		600	mA
Discharge Resistor	R_{VS}	I_{LOAD} = 1mA		300	500	Ω
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				+150		°C
Thermal Shutdown Hysteresis				10		°C
ESD PROTECTION						
SDA1, SCL1, SYNCH1, SYNCV1, RED, GRN, BLU, $\overline{EN}$, V_S		HBM		±15		kV
		IEC 61000-4-2 Contact		±8		kV

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: Guaranteed by design.

*The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

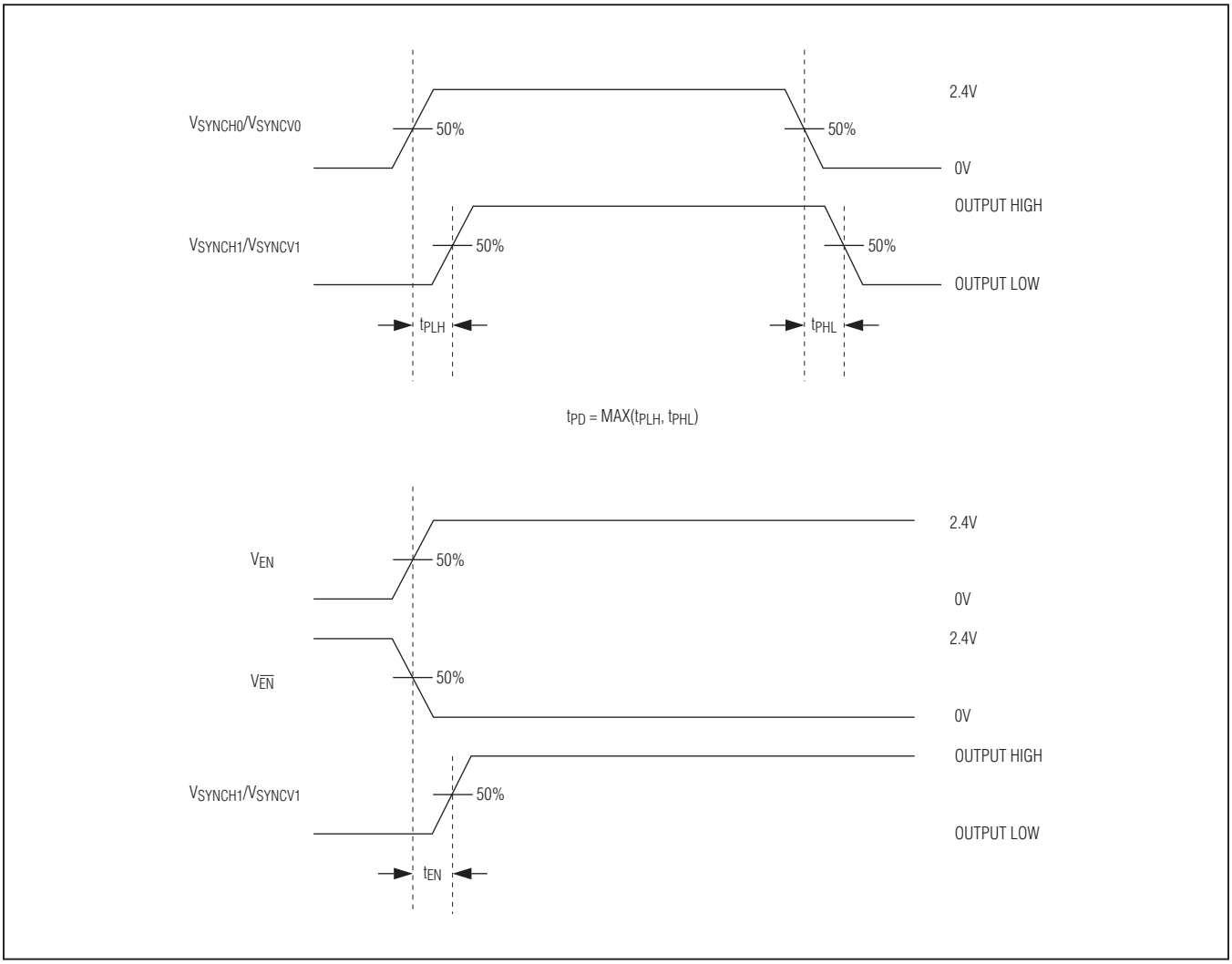
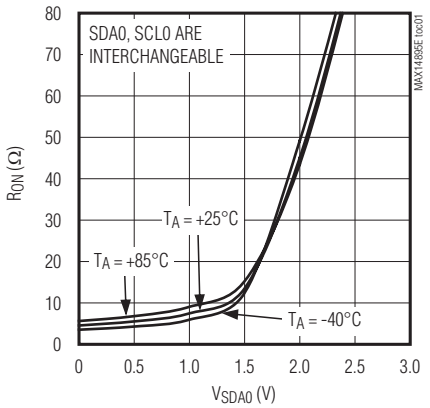


Figure 1. Timing Diagram

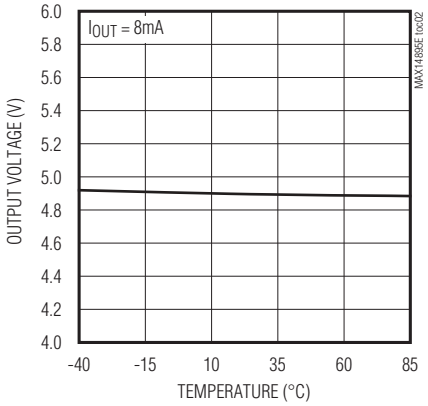
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

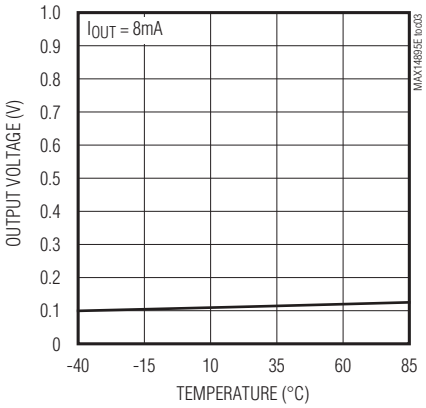
ON-RESISTANCE vs. SDA0 VOLTAGE



HV BUFFER OUTPUT-VOLTAGE HIGH vs. TEMPERATURE

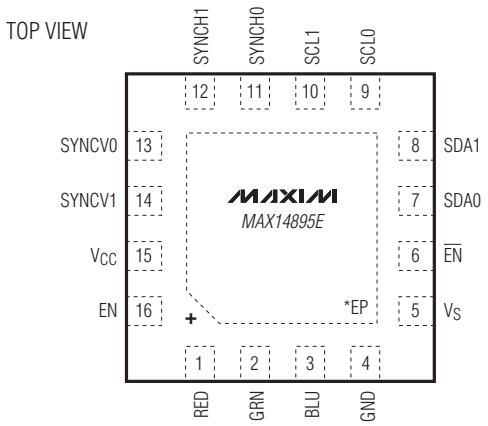


HV BUFFER OUTPUT-VOLTAGE LOW vs. TEMPERATURE



Enhanced VGA Port Protector

Pin Configuration



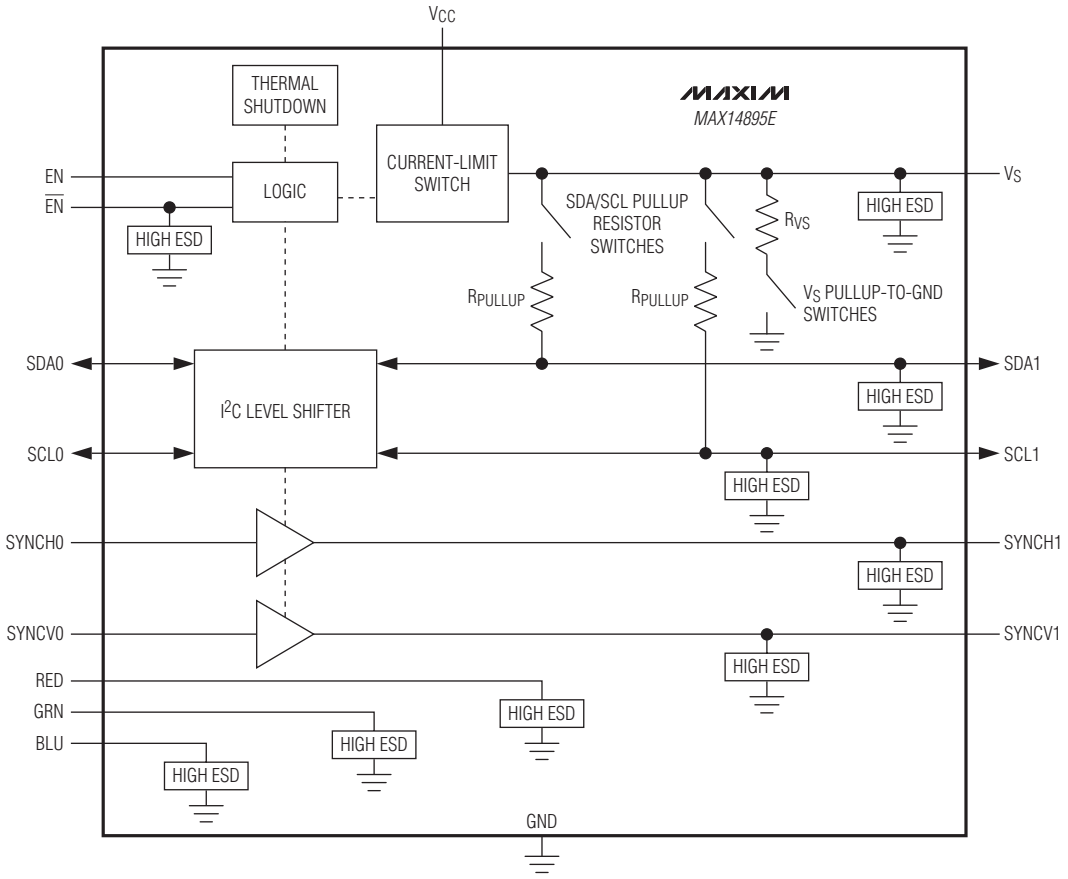
TQFN
(3mm x 3mm)

*CONNECT EP TO GND.

Pin Description

PIN	NAME	FUNCTION
1	RED	High-ESD Protection Diodes for RGB Signals
2	GRN	High-ESD Protection Diodes for RGB Signals
3	BLU	High-ESD Protection Diodes for RGB Signals
4	GND	Ground
5	V_S	Supply Voltage Output with Current-Limit Switch. V_S provides a current-limited voltage from V_{CC} when the device is enabled. Bypass V_S to GND with a 1µF or larger ceramic capacitor as close as possible to the device.
6	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ high and EN low to disable the device. $\overline{EN}$ is weakly pulled up internally.
7	SDA0	DDC Data Input from Graphics Controller
8	SDA1	DDC Data Output to VGA Monitor. Internally pulled up to V_{CC}.
9	SCL0	DDC Clock Input from Graphics Controller
10	SCL1	DDC Clock Output to VGA Monitor. Internally pulled up to V_{CC}.
11	SYNCH0	Horizontal Sync Input
12	SYNCH1	Horizontal Sync Output
13	SYNCV0	Vertical Sync Input
14	SYNCV1	Vertical Sync Output
15	V_{CC}	Supply Voltage Input. Apply a voltage between +4.75V and +5.25V to V_{CC} to power the device. Bypass V_{CC} to GND with a 1µF or larger ceramic capacitor as close as possible to the device.
16	EN	Active-High Enable Input. Drive EN low and $\overline{EN}$ high to disable the device. $\overline{EN}$ is weakly pulled down internally.
—	EP	Exposed Pad. Connect EP to GND. For enhanced thermal dissipation, connect EP to a large ground plane. Do not use EP as the only ground connection.

Functional Diagram/Truth Table



EN	$\overline{EN}$	DEVICE LOGIC
0	0	Enable
0	1	Disable
1	0	Enable
1	1	Enable

DEVICE LOGIC/ EVENT	SYNCH_/SYNCV_ BUFFER	I²C LEVEL SHIFTER	CURRENT-LIMIT SWITCH	SDA/SCL PULLUP RESISTOR SWITCHES	VS PULL-TO-GND SWITCH
Enable No Overcurrent	On	On	On	On	Off
Enable Overcurrent	On	On	Current Limit	On	Off
Enable Overcurrent Thermal Shutdown	Output 0V	Off	Off	Off	On
Disable	Output 0V	Off	Off	Off	On
V_{CC} = 0V	Off	Off	Off	Off	Off

Detailed Description

The MAX14895E integrates level-translating buffers and features RED, GRN, and BLU port protection for VGA signals. Horizontal and vertical synchronization (SYNCH0, SYNCV0) inputs feature level-shifting buffers to support low-voltage CMOS or standard TTL-compatible graphics controllers. Each output can drive ±10mA and meets VESA specifications. The device also features I^2C level shifting using two nMOS devices.

The device generates its own internal bias supply to clamp SCL0 and SDA0 to a safe level, removing the need for another external supply. The device also provides a current-limited V_{CC} output with power-off protection. This output can be used to switch power to a VGA connector or the VGA interface of a monitor.

Horizontal/Vertical Sync Level Shifter

SYNCH0 and SYNCV0 are buffered to provide level shifting and drive capability to meet the VESA specification. The level-shifted outputs (SYNCH1, SYNCV1) are pulled low when EN is low and $\overline{EN}$ is high, or when the device is in thermal shutdown (see the *Functional Diagram/Truth Table*). Logic-level outputs (V_{OL}, V_{OH}) are 5V TTL-compatible. These two buffers are identical and each can drive either the horizontal or the vertical synch signal.

Display Data Channel Switches

The device incorporates two nMOS switches for I^2C level shifting. The SDA0 and SCL0 terminals are voltage clamped to a diode drop less than the internal V_L voltage. Voltage clamping provides protection and compatibility with the SDA0 and SCL0 signals and low-voltage ASICs. When power is off (V_{CC} = 0V), SDA1 and SCL1 are protected against reverse-leakage current up to V_S = +5.25V. The SDA_ and SCL_ switches are identical, and each switch can be used to route SDA_ or SCL_ signals.

RGB Ports

The device includes three terminals for RED, GRN, and BLU signals. These terminals provide high-level ESD protection to the RGB lines while keeping the capacitance on the RGB lines to a minimum. The RED, GRN, BLU terminals are identical, and any of the three terminals can be used to protect red, green, or blue video signals.

EN, $\overline{EN}$

The device has dual complementary EN and $\overline{EN}$ enable inputs and can accept either active-low or active-high enable signals. Pull EN low and $\overline{EN}$ high to place the device in shutdown (see the *Functional Diagram/Truth Table*).

V_S Output

The device provides a current-limited voltage on V_S when the part is enabled. V_S is used as the pullup voltage for internal pullup resistors on SDA1 and SCL1, and can be used as an external supply. The internal pullup resistors from SDA1 and SCL1 to V_S are active when the device is enabled, and are disabled when the device is in thermal shutdown (see the *Functional Diagram/Truth Table*).

The V_S supply includes an internal resistor to discharge the supply when the device is in thermal shutdown or is disabled (see the *Functional Diagram/Truth Table*). V_S is current limited to prevent damage to host devices. When power is off (V_{CC} = 0V), V_S is protected against reverse-leakage current up to V_S = +5.25V.

Thermal Shutdown

Thermal-shutdown circuitry protects the device from overheating. The device enters thermal shutdown when the junction temperature exceeds +150°C (typ) and returns to normal operation when the temperature drops by approximately +10°C (typ) below the thermal-shutdown threshold. When the device is in thermal shutdown, both SYNCH1 and SYNCV1 are pulled down to ground, the I^2C level shifters are disabled, the SDA1 and SCL1 pullups are off, and the V_S discharge resistor is on (see the *Functional Diagram/Truth Table*).

Applications Information

Power-Supply Decoupling

Bypass V_{CC} and V_S to ground with 1µF ceramic capacitors as close as possible to the device.

PCB Layout

High-speed switches such as the MAX14895E require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and are as short as possible. Connect the exposed pad to a solid ground plane.

ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all terminals to protect against electrostatic discharges encountered during handling and assembly. Additionally, the device is protected to ±15kV on the RED, GRN, BLU, $\overline{EN}$, V_S, SYNCH1, SYNCV1, SCL1, and SDA1 terminals by the HBM. For optimum ESD performance, bypass V_{CC} to ground with a 1µF ceramic capacitor.

ESD protection can be tested in various ways. The RED, GRN, BLU, $\overline{EN}$, V_S, SYNCH1, SYNCV1, SCL1, and SDA1 terminals of the device are characterized for protection to the following limits:

- ±15kV using the HBM
- ±8kV using IEC 61000-4-2 Contact Discharge

Human Body Model

Figure 2 shows the HBM. Figure 3 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

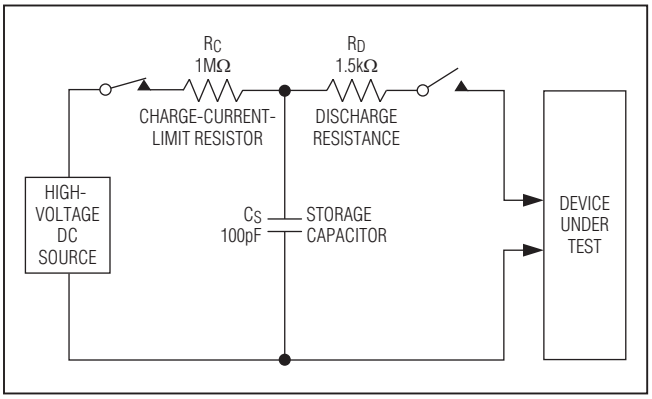


Figure 2. Human Body ESD Test Model

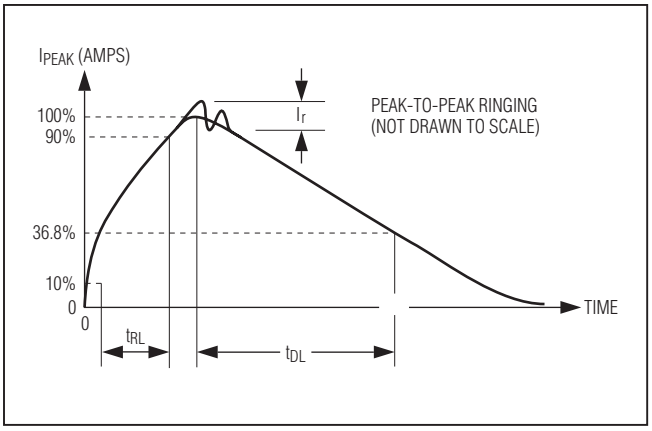


Figure 3. Human Body Current Waveform

IEC 61000-4-2

The IEC 6100-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The device assists in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. Figure 4 shows the IEC 61000-4-2 model, and Figure 5 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

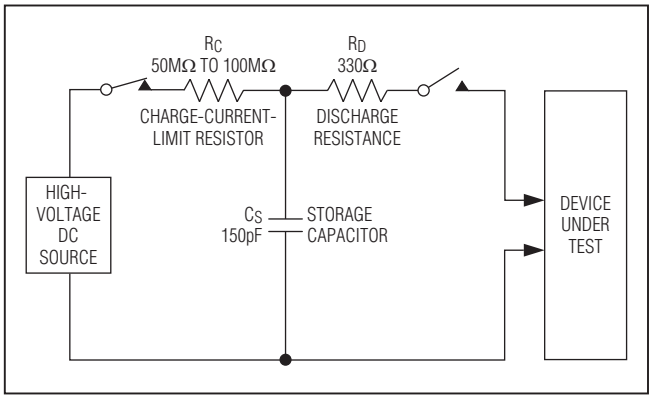


Figure 4. IEC 61000-4-2 ESD Test Model

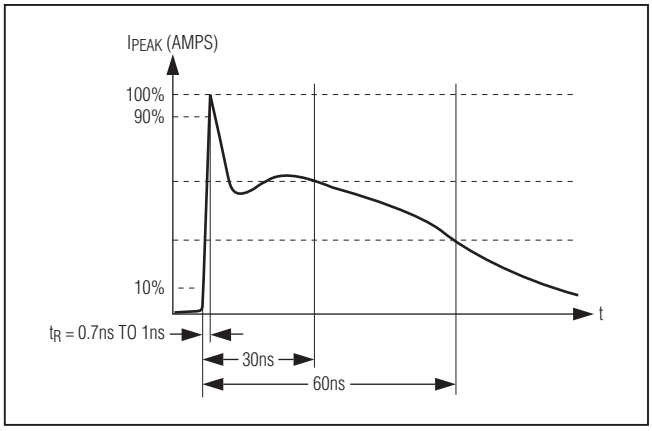


Figure 5. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14895EETE+T	-40°C to +85°C	16 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+4	21-0136	90-0031

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—