32-Channel Serial to Parallel Converter with P-Channel Open Drain Outputs

Features

- Processed with HVCMOS® Technology
- Output voltages to -220V
- Source current minimum 60mA
- Shift register speed 8.0MHz
- Polarity and blanking inputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Can be used with the HV5622 to provide 220V push-pull operation
- 44-lead PLCC surface mount package

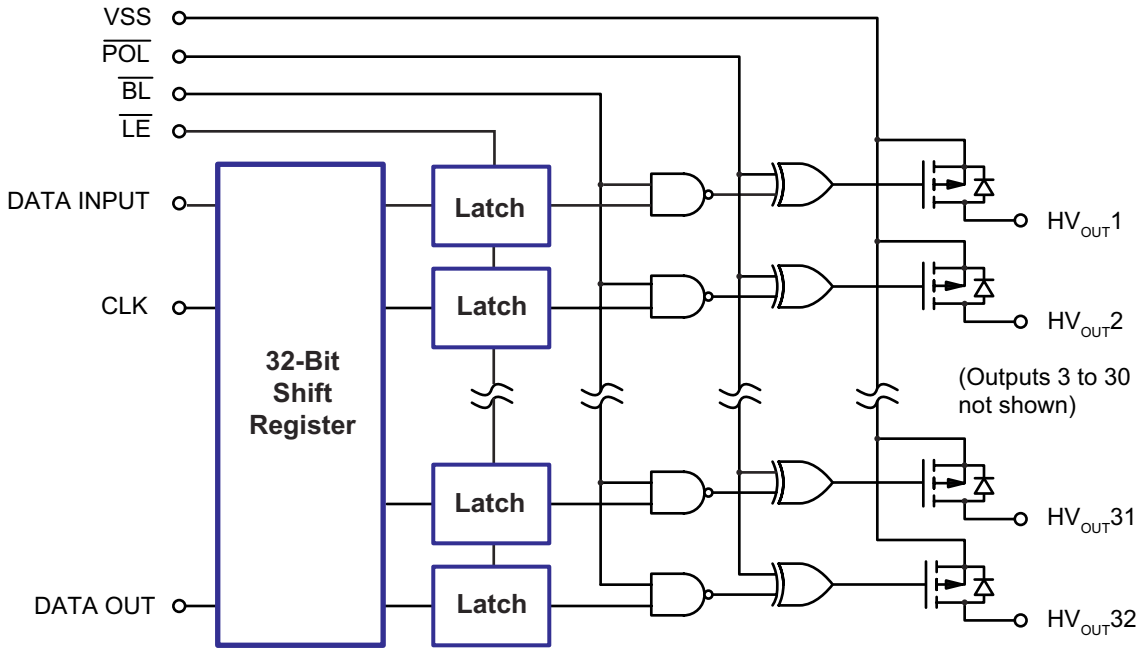
General Description

The HV4622 is a low-voltage serial to high-voltage parallel converter with P-Channel open drain outputs. This device has been designed for use a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high-voltage current source capabilities, such as driving inkjet and electrostatic print heads, plasma panels, or vacuum fluorescent displays.

This device consists of a 32-bit shift register, 32 data latches, and control logic to perform polarity and blanking functions. Data is shifted through the shift register on the logic high-to-low transition of the clock. The HV4622 shifts in the clockwise direction (when viewed from the top of the package). A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. The data in the shift register is latched when the latch enable pin is brought to logic high, and then returned to ground. If the latch enable pin is held high, the latch becomes transparent and the shift register data is directly reflected in the outputs.

For applications requiring active pull down as well as pull up, the HV4622 can be paired with the HV5622.

Functional Block Diagram



Ordering Information

Device	Package Options
	44-Lead PLCC ***.653x.653in body*** ***.180in height (max)*** ***.050in pitch***
HV4622	HV4622PJ-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

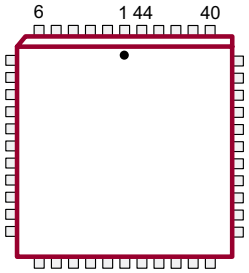
Parameter	Value
Supply voltage, V_{DD}	+0.5V to -16V
Output voltage, V_{PP}	+0.5V to -240V
Logic input levels	+0.5V to V_{DD} -0.3V
Ground current[1]	1.5A
Continuous total power dissipation[2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to V_{SS}.

Notes:

1. *Duty cycle limited by the total power dissipated in the package.*
2. *For operation above 25°C ambiant derate linearly to maximum operating temperature at 20mW/°C.*

Pin Configuration



44-Lead PLCC (PJ)
(top view)

Product Marking

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*
_____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

44-Lead PLCC (PJ)

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	-10.8	-13.2	V
V_{PP}	Output voltage	+0.3	-220	V
V_{IH}	High-level input voltage (Logic "1")	V_{DD} +2.0V	V_{DD}	V
V_{IL}	Low-level input voltage (Logic "0")	0	-2.0	V
f_{CLK}	Clock frequency	-	8.0	MHz
T_A	Operating free-air temperature	-40	+85	°C

Note:

All voltages are referenced to V_{SS}.

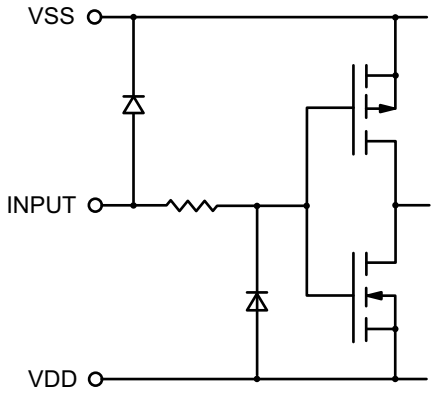
DC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	-15	mA	f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz
I_{DDQ}	Quiescent V_{DD} supply current		-	-100	µA	V_{IN} = V_{SS} or V_{DD}
$I_{O(OFF)}$	Off state output current		-	-100	µA	All SWS parallel
I_{IH}	High-level logic input current		-	-1.0	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	+1.0	µA	V_{IL} = V_{SS}
V_{OH}	High level output		V_{DD} +1.0V	-	V	I_{DOUT} = -100µA
V_{OL}	Low level output	HV_{OUT}	-	-30	V	I_{HVOUT} = -60mA
		D_{OUT}	-	-1.0	V	I_{DOUT} = -100µA
V_{OC}	HV_{OUT} clamp voltage		-	+1.5	V	I_{OL} = +60mA

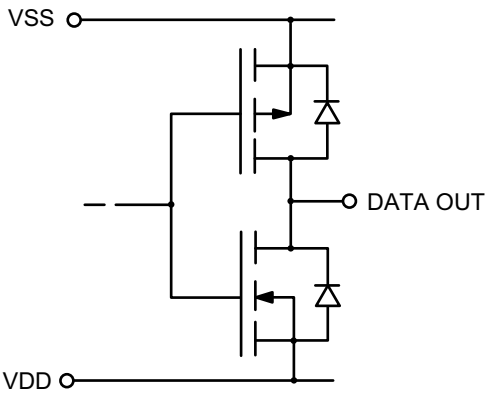
AC Electrical Characteristics *(V_{DD} = -12V, T_C = 25°C)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_{WH}, t_{WL}	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	50	-	ns	---
t_H	Data hold time after clock rises	20	-	ns	---
t_{ON}	Turn on time, HV_{OUT} from enable	-	400	ns	R_L = 10KΩ to V_{OO} max
t_{DHL}	Delay time clock to data high to low	-	100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high	-	100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ high to low	50	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	50	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	50	-	ns	---

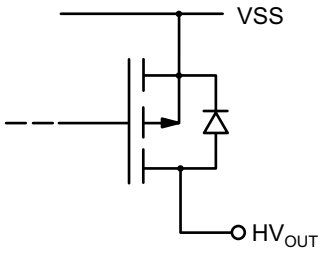
Input and Output Equivalent Circuits



Logic Inputs

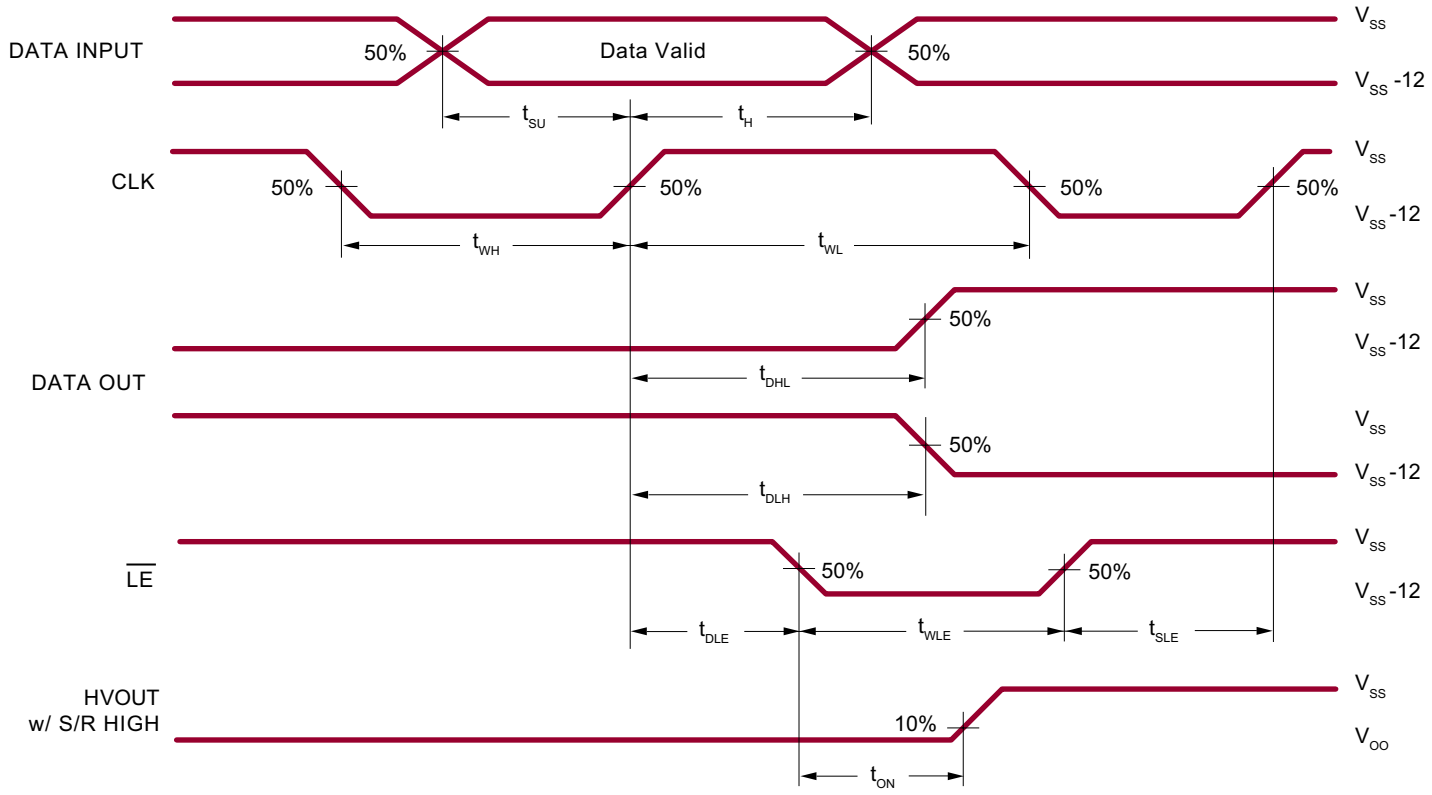


Logic Data Output



High Voltage Output

Switching Waveforms



Function Table

Function	Inputs					Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	Shift Reg		HV Outputs		Data Out
						1	2...32	1	2...32	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↓	L	H	H	H or L	*...*	*	*...*	*
Load latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↓	H	H	H	L	*...*	L	*...*	*
	H	↓	H	H	H	H	*...*	H	*...*	*

Notes:

H = high level = -12V, L = low level = 0V, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition.

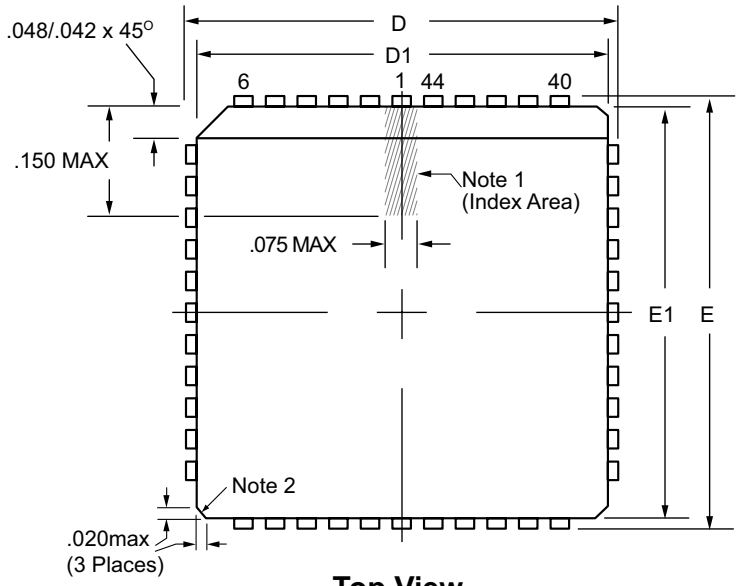
* = dependent on previous stage's state before the last CLK high-to-low transition or last $\overline{LE}$ high.

Pin Description

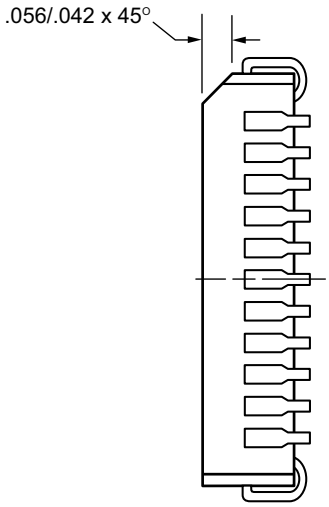
Pin #	Function	Description
1	$HV_{OUT}16$	High voltage outputs.
2	$HV_{OUT}15$	
3	$HV_{OUT}14$	
4	$HV_{OUT}13$	
5	$HV_{OUT}12$	
6	$HV_{OUT}11$	
7	$HV_{OUT}10$	
8	$HV_{OUT}9$	
9	$HV_{OUT}8$	
10	$HV_{OUT}7$	
11	$HV_{OUT}6$	
12	$HV_{OUT}5$	
13	$HV_{OUT}4$	
14	$HV_{OUT}3$	
15	$HV_{OUT}2$	
16	$HV_{OUT}1$	
17	N/C	No connect.
18	Data Out	Data output pin.
19	N/C	No connect.
20	N/C	
21	N/C	
22	$\overline{POL}$	Inverts the polarity of the HV_{OUT} pins
23	CLOCK	Clock pin, shift registers shifts data on rising edge of input clock.
24	VSS	Reference voltage, usually ground.
25	VDD	Logic supply voltage.
26	$\overline{LE}$	Logic enable pin, data is shifted from shift register to latches on logic input low.
27	Data In	Data input pin.
28	$\overline{BL}$	Blanking pin, logic input low sets all HV_{OUT} pins low.
29	$HV_{OUT}32$	High voltage outputs.
30	$HV_{OUT}31$	
31	$HV_{OUT}30$	
32	$HV_{OUT}29$	
33	$HV_{OUT}28$	
34	$HV_{OUT}27$	
35	$HV_{OUT}26$	
36	$HV_{OUT}25$	
37	$HV_{OUT}24$	
37	$HV_{OUT}23$	
39	$HV_{OUT}22$	
40	$HV_{OUT}21$	
41	$HV_{OUT}20$	
42	$HV_{OUT}19$	
43	$HV_{OUT}18$	
44	$HV_{OUT}17$	

44-Lead PLCC Package Outline (PJ)

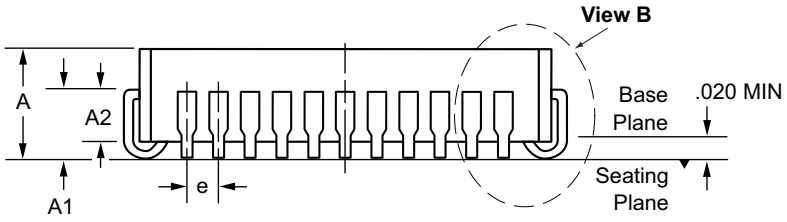
.653x.653in body, .180in height (max), .050in pitch



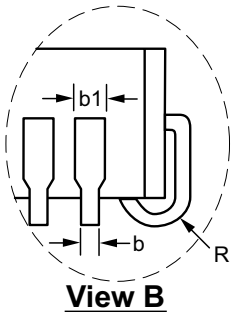
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-44PLCCPJ, Version F031111.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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