Four-Channel, High Speed, ±75V 1.25A Ultrasound Pulser

Features

- HVCMOS technology for high performance
- High density integration ultrasound transmitter
- 0 to ±75V output voltage
- ±1.25A source and sink current in pulse mode
- ±400mA source and sink current in CW mode
- Up to 20MHz operating frequency
- Matched delay times
- 1.2V to 5.0V CMOS logic interface
- Built-in output drain bleed resistors

Application

- Portable medical ultrasound imaging
- Piezoelectric transducer drivers
- NDT ultrasound transmission
- Pulse waveform generator

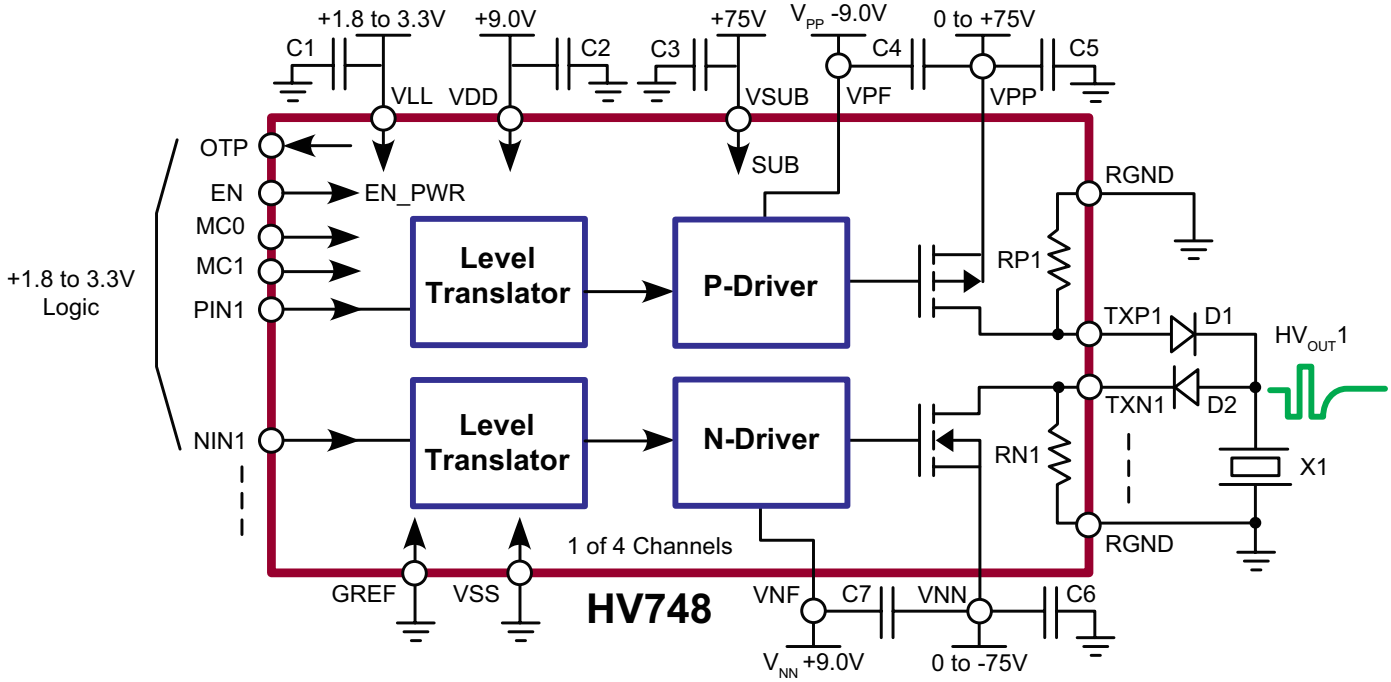
General Description

The Supertex HV748 is a four-channel, monolithic, high voltage, high speed pulse generator. It is designed for portable medical ultrasound applications. This high voltage and high speed integrated circuit can also be used for piezoelectric, capacitive or MEMS sensing in ultrasonic nondestructive detection and sonar ranger applications.

The HV748 consists of a controller logic interface circuit, level translators, MOSFET gate drives and high power P-channel and N-channel MOSFETs as the output stage for each channel.

The output stages of each channel are designed to provide peak output currents over ±1.8A for pulsing, when in mode 4, with up to ±75 volt swings. When in mode 1, all the output stages drop the peak current to ±400mA for low-voltage CW mode operation to decrease the power consumption of the IC. The P and N type of power FETs gate drivers are supplied by two floating 9.0VDC power supplies reference to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers not only eliminates two high voltage capacitors per channel, but also makes the PCB layout easier.

Typical Application Circuit



Ordering Information

Device	48-Lead QFN *7.00x7.00mm body* *1.00mm height (max)* *0.50mm pitch*
HV748	HV748K6-G

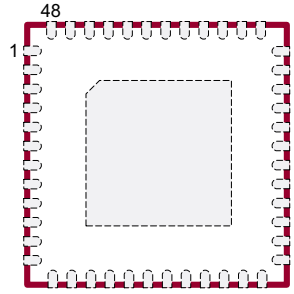
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{SS}, Power supply reference	0V
V_{LL}, Positive logic supply	-0.5V to +7.0V
V_{DD}, Positive logic and level translator supply	-0.5V to +14V
(V_{PP} -V_{PF}) Positive floating gate drive supply	-0.5V to +14V
(V_{NF}- V_{NN}) Negative gate floating drive supply	-0.5V to +14V
(V_{PP}-V_{NN}) Differential high voltage supply	+170V
V_{PP}, High voltage positive supply	-0.5V to +85V
V_{NN}, High voltage negative supply	+0.5V to –85V
OTP, Over Temperature Protection output	-0.5V to +7.0V
All logic input PIN_X, NIN_X and EN voltages	-0.5V to +7.0V
(V_{SUB}- V_{SS}) Substrate to V_{SS} voltage difference	+170V
(V_{PP} –TXP_X) V_{PP} to TXP_X voltage difference	+170V
(V_{SUB}- TXP_X) Substrate to TXP_X voltage difference	+170V
(TXN_X-V_{NN}) TXN_X to V_{NN} voltage difference	+170V
Operating temperature	-40°C to 125°C
Storage temperature	-65°C to 150°C
Thermal resistance, θ_{JA}	29°C/W
Thermal resistance, θ_{JC} (junction to thermal pad)	0.5°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



48-Lead QFN
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or

48-Lead QFN

Power-Up Sequence

Step	Description
1	V_{SUB}
2	V_{LL} with logic signal low
3	V_{DD}
4	(V_{PP} -V_{PF}) and (V_{NF} –V_{NN})
5	V_{PP} and V_{NN}
6	Logic control signals

Power-Down Sequence

Step	Description
1	All logic signals go to low
2	V_{PP} and V_{NN}
3	(V_{PP} -V_{PF}) and (V_{NF} –V_{NN})
4	V_{DD}
5	V_{LL}
6	V_{SUB}

Operating Supply Voltages and Current (4 Channel Active)

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9.0V, V_{PP}-V_{PF} = +9.0V, V_{NN}-V_{NF} = -9.0V, V_{PP} =+75V, V_{NN} = -75V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic voltage reference	1.2	1.8 to 3.3	5.0	V	---
V_{DD}	Internal voltage supply	8.0	9.0	12	V	---
V_{PF}	Positive gate driver supply	(V_{PP}-12)	(V_{PP}-9.0)	(V_{PP}-8.0)	V	Floating driver voltage supplies.
V_{NF}	Negative gate drive supply	(V_{NN}+8.0)	(V_{NN}+9.0)	(V_{NN}+12.0)	V	
V_{SUB}	IC substrate voltage	V_{DD}	V_{PP}	+75	V	Must be the most positive potential of the IC.
V_{PP}	Positive HV supply	0	-	+75	V	---
V_{NN}	Negative HV supply	-75	-	0	V	---
SR_{MAX}	Slew rate limit of V_{PP}, V_{NN}	-	-	25	V/µs	Built-in slew rate detection protection.
I_{LL}	V_{LL} Current EN = Low	-	35	120	µA	---
I_{DDQ}	V_{DD} Current EN = Low	-	15	-	µA	---
I_{DDEN}	V_{DD} Current EN = High	-	0.75	2.0	mA	f = 0MHz
I_{DDEN}	V_{DD} Current MODE = 4	-	0.75	-	mA	f = 5.0MHz, continuous, no loads
I_{DDENCW}	V_{DD} Current MODE = 1	-	2.0	-	mA	
I_{PPQ}	V_{PP} Current EN = Low	-	10	25	µA	f = 0MHz
I_{PPEN}	V_{PP} Current MODE = 4	-	250	-	mA	f = 5.0MHz, continuous, no loads
I_{PPENCW}	V_{PP} Current MODE = 1	-	170	-	mA	
I_{NNQ}	V_{NN} Current EN = Low	-	15	30	µA	f = 0MHz
I_{NNEN}	V_{NN} Current MODE = 4	-	250	-	mA	f = 5.0MHz, continuous, no loads
I_{NNENCW}	V_{NN} Current MODE = 1	-	170	-	mA	
I_{PFQ}	V_{PF} Current EN = Low	-	10	25	µA	f = 0MHz
I_{PFEN}	V_{PF} Current MODE = 4	-	50	-	mA	f = 5.0MHz, continuous, no loads
I_{PFENCW}	V_{PF} Current MODE = 1	-	12	-	mA	
I_{NFQ}	V_{NF} Current EN = Low	-	20	30	µA	f = 0MHz
I_{NFEN}	V_{NF} Current MODE = 4	-	25	-	mA	f = 5.0MHz, continuous, no loads
I_{NFENCW}	V_{NF} Current MODE = 1	-	12	-	mA	

Note:

All supply current values are for reference only.

Under Voltage and Over Temperature Protection

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PULL_UP}	Open drain pull-up voltage	-	-	5.0	V	---
V_{UVDD}	V_{DD} threshold	3.5	-	6.5	V	---
V_{UVLL}	V_{LL} threshold	0.7	-	1.0	V	---
V_{UVVF}	V_{PF}, V_{NF} threshold	3.5	-	6.5	V	---
V_{OL_OTP}	OTP flag output low voltage	-	-	1.0	V	V_{LL} = 3.3V, OTP = Active, I_{PULL_UP} = 1.0mA.
I_{OTP}	Max. open drain output current	-	1.0	-	mA	---
T_{OTP}	Over-temperature threshold	95	110	125	°C	If over-temperature occurred, OTP low and all TX outputs will be HiZ.
T_{HYS}	OTP output reset hysteresis	-	7.0	-		

DC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} = 0V, V_{LL} = +3.3V, V_{DD} = +9V, V_{PF} = V_{PP} -9V, V_{NF} = V_{NN} + 9V, V_{PP} = +75V, V_{NN} = -75V, T_A = 25°C)

Output P-Channel MOSFET, TXP (Mode 4)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	1.25	1.8	-	A	---
R_{ON}	Channel resistance	-	8.0	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	100*	-	pF	V_{DS} = 25V, f = 1.0MHz

Output N-Channel MOSFET, TXN (Mode 4)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	1.25	1.8	-	A	---
R_{ON}	Channel resistance	-	7.5	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	40*	-	pF	V_{DS} = 25V, f = 1.0MHz

MOSFET Drain Bleed Resistor

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{P/N1\sim4}$	Output bleed resistance	10	15	30	kΩ	---
P_{RO}	Bleed resistors power limit	-	-	40	mW	---

Logic Inputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	(V_{LL}-0.4)	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	0.4	V	---
I_{IH}	Input logic high current	-	-	10	µA	---
I_{IL}	Input logic low current	-10	-	-	µA	---
C_{IN}	Input logic capacitance	-	-	5.0*	pF	---

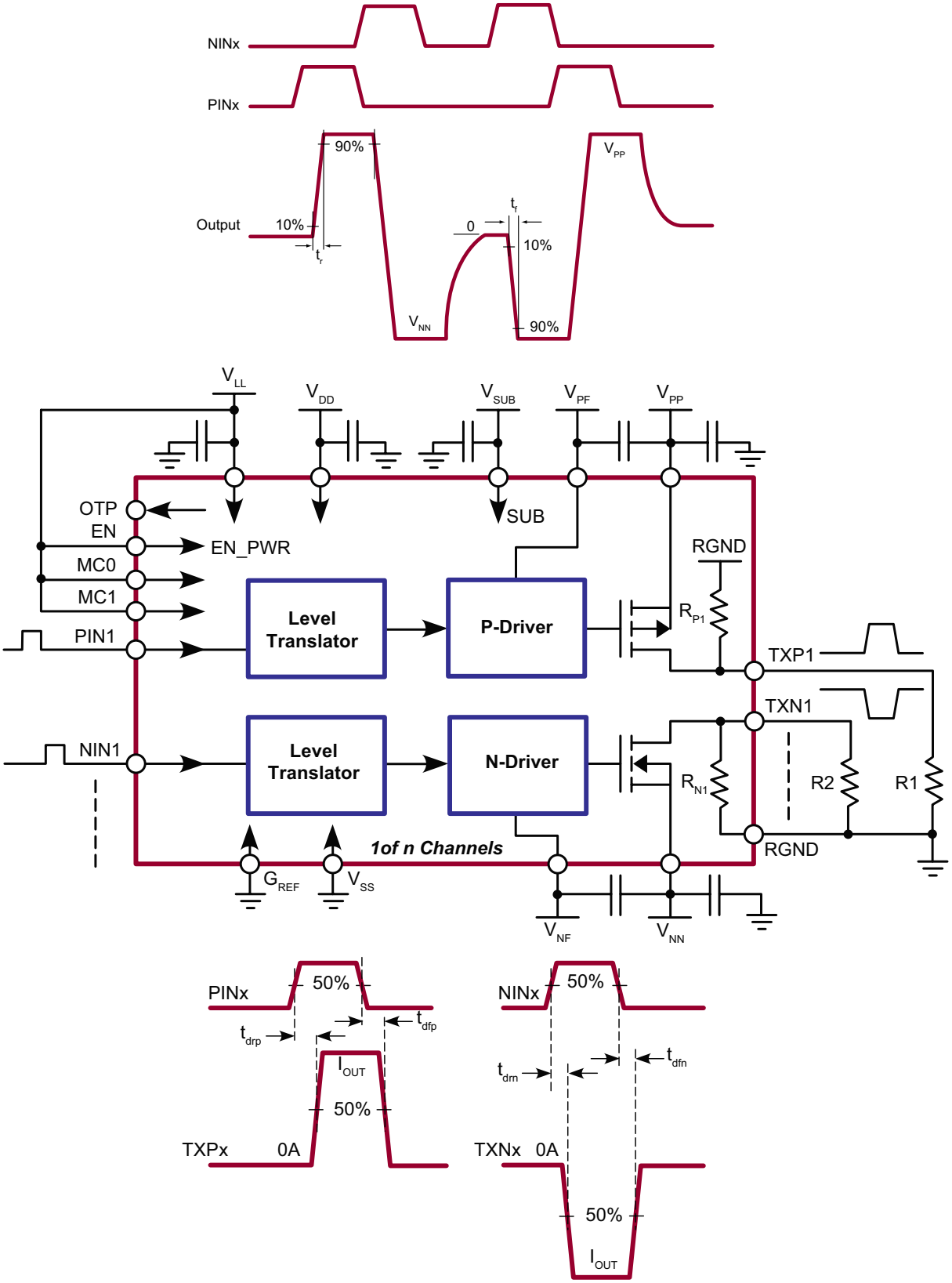
AC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS} =0V, V_{LL} = +3.3V, V_{DD} = +9V, V_{PF} = (V_{PP} - 9V), V_{NF} = (V_{NN} +9V), V_{PP} = +75V, V_{NN} = -75V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_r	Output rise time	-	35	-	ns	330pF//2.5kΩ load
t_f	Output fall time	-	43	-	ns	
f_{OUT}	Output frequency range	-	-	20	MHz	100Ω resistor load
HD2	Second harmonic distortion	-	-40*	-	dB	
t_{EN}	Enable time	-	180	500	µs	
t_{DIS}	Disable time	-	2.8	10	µs	
t_{dr}	Delay time on inputs rise	-	18	-	ns	3.9Ω resistor load (see timing diagram)
t_{df}	Delay time on inputs fall	-	18	-	ns	
Δt_{DELAY}	Delay time matching	-	±2.0	-	ns	P to N, channel to channel
t_{dm}	Delay on mode change	-	2.5	10	µs	100Ω resistor load
t_j	Delay jitter on rise or fall	-	15*	-	ps	V_{PP}/V_{NN} = ±25V, input t_r 50% to HV_{OUT} t_r or t_f 50%, with 330pF//2.5kΩ load

* *Guaranteed by design.*

Switch AC Test Timing Diagram



Truth Table (All Modes)

Logic Inputs			Output	
EN	PIN_x	NIN_x	TXP_x	TXN_x
1	0	0	OFF	OFF
1	1	0	ON	OFF
1	0	1	OFF	ON
1	1	1	ON†	ON†
0	X	X	OFF	OFF

† *Not allowed, may damage IC.*

Drive Mode Control Table

Mode	MC1	MC0	I_{SC} (A)	R_{ONP} (Ω)	R_{ONR} (Ω)
1	0	0	0.41	35	33
2	0	1	0.58	25	23
3	1	0	0.97	15	14
4	1	1	1.8	8.0	7.5

Notes:

1. *V_{PP}/V_{NN} = +/-75V, $V_{DD} = (V_{PP} – V_{PF}) = (V_{NF} – V_{NN})$ = +9.0V*
2. *I_{SC} is current into 1.0Ω to GND*
3. *R_{ON} calculated from V_{OUT} into 100Ω load*

Pin Descriptions

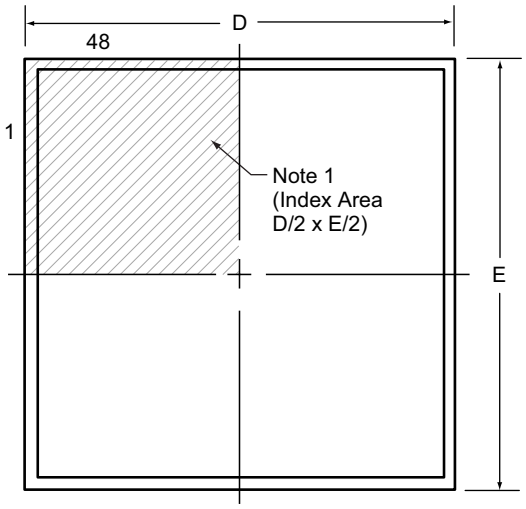
Pin #	Name	Function
1	VDD	Positive internal voltage supply (+9.0V).
2	VSS	Power supply return (0V).
3	PIN1	Input logic control of high voltage output P-FET of channel 1, Hi = on, Low = off.
4	NIN1	Input logic control of high voltage output N-FET of channel 1, Hi = on, Low = off.
5	PIN2	Input logic control of high voltage output P-FET of channel 2, Hi = on, Low = off.
6	NIN2	Input logic control of high voltage output N-FET of channel 2, Hi = on, Low = off.
7	PIN3	Input logic control of high voltage output P-FET of channel 3, Hi = on, Low = off.
8	NIN3	Input logic control of high voltage output N-FET of channel 3, Hi = on, Low = off.
9	PIN4	Input logic control of high voltage output P-FET of channel 4, Hi = on, Low = off.
10	NIN4	Input logic control of high voltage output N-FET of channel 4, Hi = on, Low = off.
11	VSS	Power supply return (0V).
12	VDD	Positive internal voltage supply (+9.0V).
13	OTP	Over temperature protection output, open N-FET drain, active low if IC temperature >110°C.
14	MC1	Output current mode control pins, see Drive Mode Control Table.
15	MC0	
16	Thermal Pad (VSUB)	Substrate of the IC, Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.

Pin Descriptions *(cont.)*

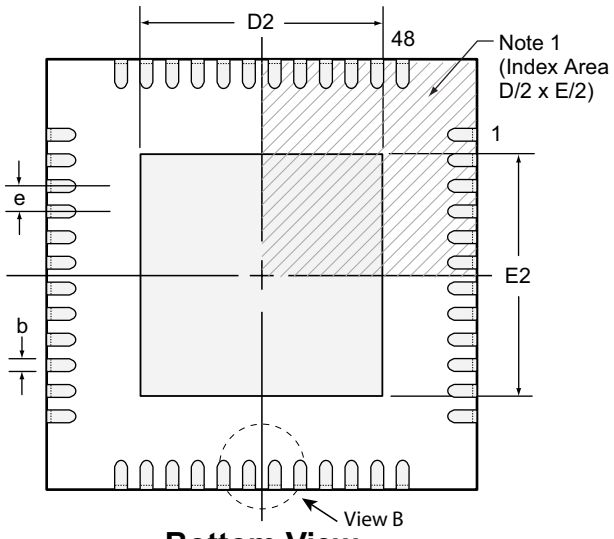
Pin #	Name	Function
17	VPF	P-FET drive floating power supply, (V_{PP}- V_{PF}) = +9.0V.
18	VPP	Positive high voltage power supply (+75V).
19		
20		
21	VNN	Negative high voltage power supply (-75V).
22		
23		
24	VNF	N-FET drive floating power supply, (V_{NF}- V_{NN}) = +9.0V.
25	Thermal Pad (VSUB)	Substrate of the IC, Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
26	RGND	Bleed resistors common return ground. (Both pins must be used)
27	TXN4	Output N-FET drain (open drain output) for channel 4.
28	TXP4	Output P-FET drain (open drain output) for channel 4.
29	TXN3	Output N-FET drain (open drain output) for channel 3.
30	TXP3	Output P-FET drain (open drain output) for channel 3.
31	TXN2	Output N-FET drain (open drain output) for channel 2.
32	TXP2	Output P-FET drain (open drain output) for channel 2.
33	TXN1	Output N-FET drain (open drain output) for channel 1.
34	TXP1	Output P-FET drain (open drain output) for channel 1.
35	RGND	Bleed resistors common return ground. (Both pins must be used)
36	Thermal Pad (VSUB)	Substrate of the IC, Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
37	VNF	N-FET drive floating power supply, (V_{NF}- V_{NN}) = +9.0V.
38	VNN	Negative high voltage power supply (-75V).
39		
40		
41	VPP	Positive high voltage power supply (+75V).
42		
43		
44	VPF	P-FET drive floating power supply, (V_{PP}- V_{PF}) = +9.0V.
45	Thermal Pad (VSUB)	Substrate of the IC, Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.
46	EN	Chip power enable Hi = on, Low = off.
47	GREF	Logic Low reference, logic ground (0V).
48	VLL	Logic Hi voltage reference input (+3.3V).

48-Lead QFN Package Outline (K6)

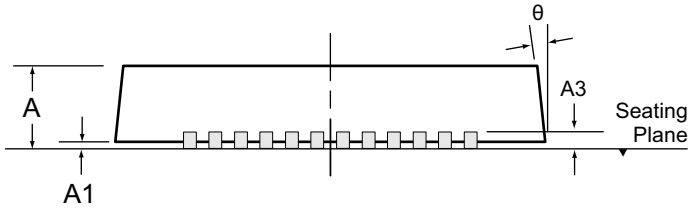
7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch



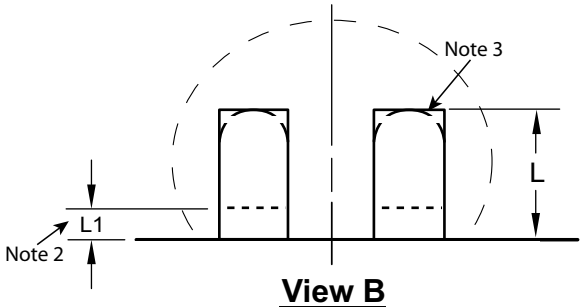
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	6.85*	1.25	6.85*	1.25	0.50 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.25	7.00	-	7.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	7.15*	5.45	7.15*	5.45		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
Supertex Doc.#: *DSPD-48QFNK67X7P050, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com