Dual, High Speed, ±75V, 2.5A Ultrasound Pulser

Features

- HVCMOS technology for high performance
- High density integration ultrasound transmitter
- 0 to ±75V output voltage
- ±2.5A source and sink current in PW mode
- ±800mA source and sink current in CW mode
- Up to 20MHz operation frequency
- Matched delay times
- 1.2V to 5.0V CMOS logic interface
- Over temperature sensing
- Under voltage protections
- Built-in output drain bleed resistors

Applications

- Portable medical ultrasound imaging
- Piezoelectric transducer drivers
- NDT ultrasound equipment
- Pulse waveform generator

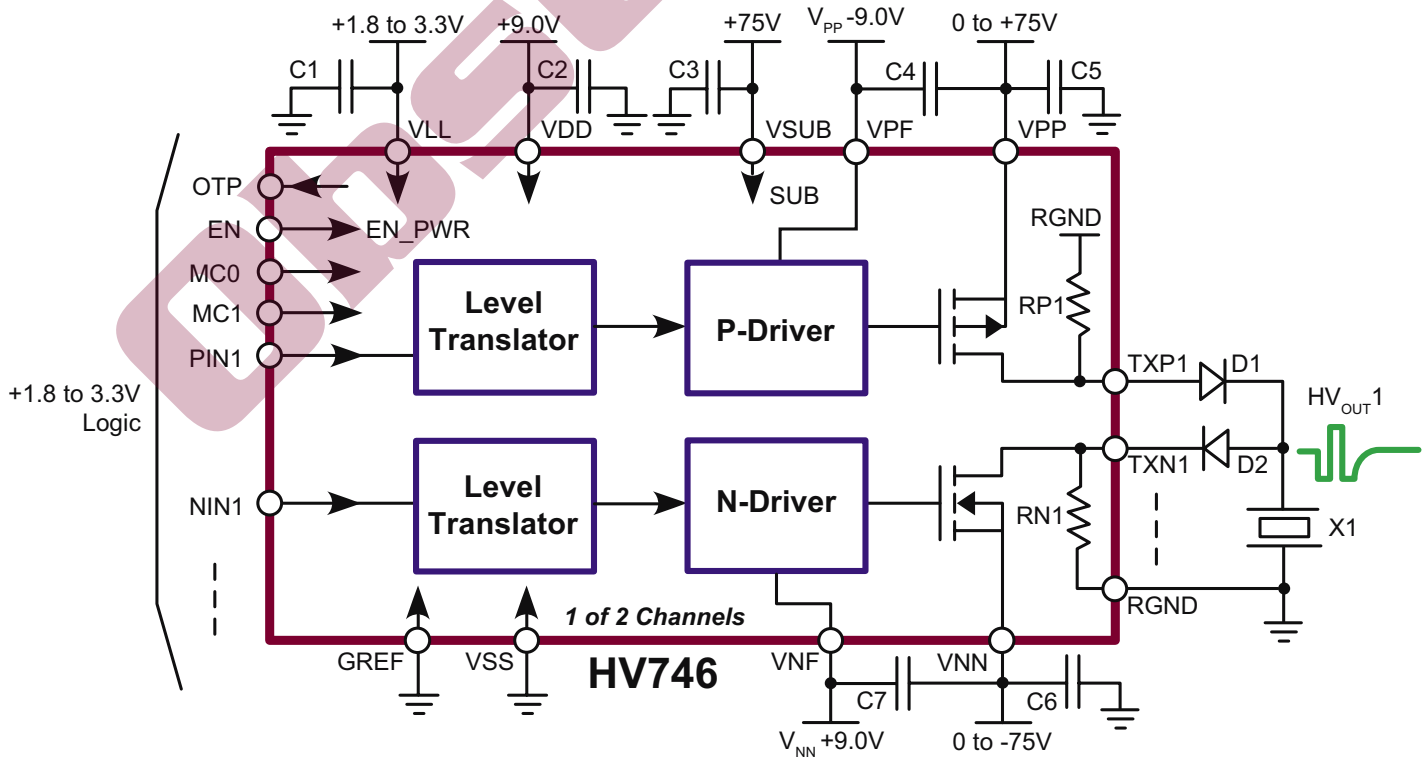
General Description

The Supertex HV746 is a dual-channel monolithic high voltage high-speed pulse generator. It is designed for portable medical ultrasound applications. This high voltage and high-speed integrated circuit can also be used for other piezoelectric, capacitive or MEMS sensor in ultrasonic nondestructive detection and sonar ranger applications.

The HV746 consists of controller logic interface circuit, level translators, MOSFET gate drives and high current power P-channel and N-channel MOSFETs as the output stage for each channel. A 2-bit mode control is provided that allows the maximum output current to be reduced for power saving.

The output stages of each channel are designed to provide peak output currents over ±3.6A for pulsing, when in mode 4, with up to ±75V swings. When in mode 1, all the output stages drop the peak current to ±800mA for low-voltage CW mode operation to save power consumption of the IC. The P and N type of power FETs gate drivers are supplied by two floating 9.0VDC power supplies reference to V_{PP} and V_{NN}. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

Typical Application Circuit



Ordering Information

Device	Package Option
	48-Lead QFN *7.00x7.00mm body* *1.00mm height (max)* *0.50mm pitch*
HV746	HV746K6-G

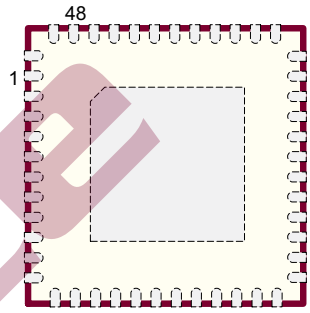
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{SS}, Power supply reference	0V
V_{LL}, Positive logic supply	-0.5V to +7.0V
V_{DD}, Positive logic and level translator supply	-0.5V to +14V
(V_{PP} -V_{PF}) Positive floating gate drive supply	-0.5V to +14V
(V_{NF}- V_{NN}) Negative gate floating drive supply	-0.5V to +14V
(V_{PP}-V_{NN}) Differential high voltage supply	+170V
V_{PP}, High voltage positive supply	-0.5V to +85V
V_{NN}, High voltage negative supply	+0.5V to –85V
OTP, Over Temperature Protection output	-0.5V to +7.0V
All logic input PIN_X, NIN_X and EN voltages	-0.5V to +7.0V
(V_{SUB} - V_{SS}) Substrate to V_{SS} voltage difference	+170V
(V_{PP} –TXP_X) V_{PP} to TXP_X voltage difference	+170V
(V_{SUB}- TXP_X) Substrate to TXP_X voltage difference	+170V
(TXN_X-V_{NN}) TXN_X to V_{NN} voltage difference	+170V
Operating temperature	-40°C to 125°C
Storage temperature	-65°C to 150°C
Thermal resistance, θ_{JA}	29°C/W
Thermal resistance, θ_{JC} (junction to thermal pad)	0.5°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



48-Lead QFN (K6)
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or

48-Lead QFN (K6)

Power-Up Sequence

Step	Description
1	V_{SUB}
2	V_{LL} with logic signal low
3	V_{DD}
4	(V_{PP} –V_{PF}) and (V_{NF}–V_{NN})
5	V_{PP} and V_{NN}
6	Logic control signals go to hi

Power-Down Sequence

Step	Description
1	Logic control signals go to low
2	V_{PP} and V_{NN}
3	(V_{PP} –V_{PF}) and (V_{NF}–V_{NN})
4	V_{DD}
5	V_{LL}
6	V_{SUB}

Operating Supply Voltages and Current (2 Channel Active)

(Operating conditions, unless otherwise specified, V_{SS}= 0V, V_{LL}= +3.3V, V_{DD}= +9.0V, V_{PP}-V_{PF}= +9.0V, V_{NN}- V_{NF}= -9.0V, V_{PP}= +75V, V_{NN}= -75V,T_A= 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic voltage reference	1.2	1.8 to 3.3	5.0	V	---
V_{DD}	Internal voltage supply	8.0	9.0	12	V	---
V_{PF}	P-FET gate driver supply	(V_{PP}-12)	(V_{PP}-9.0)	(V_{PP}-8.0)	V	Floating driver voltage supplies.
V_{NF}	N-FET gate drive supply	(V_{NN}+8.0)	(V_{NN}+9.0)	(V_{NN}+12)	V	
V_{SUB}	IC substrate voltage	V_{DD}	V_{PP}	+75	V	Must connect to the most positive potential of the IC.
V_{PP}	Positive HV supply	0	-	+75	V	---
V_{NN}	Negative HV supply	-75	-	0	V	---
SR_{MAX}	Slew rate limit of V_{PP}, V_{NN}	-	-	25	V/µs	Built-in slew rate detection protection.
I_{LL}	V_{LL} Current EN = Low	-	35	120	µA	---
I_{DDQ}	V_{DD} Current EN = Low	-	15	-	µA	---
I_{DDEN}	V_{DD} Current EN = High	-	0.75	2.0	mA	f = 0MHz
I_{DDEN}	V_{DD} Current MODE = 4	-	0.75	-	mA	f = 5.0MHz, continuous, no loads
I_{DDENCW}	V_{DD} Current MODE = 1	-	2.0	-		
I_{PPQ}	V_{PP} Current EN = Low	-	10	25	µA	---
I_{PPEN}	V_{PP} Current MODE = 4	-	250	-	mA	f = 5.0MHz, continuous, no loads
I_{PPENCW}	V_{PP} Current MODE = 1	-	170	-		
I_{NNQ}	V_{NN} Current EN = Low	-	15	30	µA	---
I_{NNEN}	V_{NN} Current MODE = 4	-	250	-	mA	f = 5.0MHz, continuous, no loads
I_{NNENCW}	V_{NN} Current MODE = 1	-	170	-		
I_{PFQ}	V_{PF} Current EN = Low	-	10	25	µA	---
I_{PFEN}	V_{PF} Current MODE = 4	-	50	-	mA	f = 5.0MHz, continuous, no loads
I_{PFENCW}	V_{PF} Current MODE = 1	-	12	-		
I_{NFQ}	V_{NF} Current EN = Low	-	20	30	µA	---
I_{NFEN}	V_{NF} Current MODE = 4	-	25	-	mA	f = 5.0MHz, continuous, no loads
I_{NFENCW}	V_{NF} Current MODE = 1	-	12	-		

Under Voltage and Over Temperature Protection

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PULL_UP}	Open drain pull-up voltage	-	-	5.0	V	---
V_{UVDD}	V_{DD} threshold	3.5	-	6.5	V	---
V_{UVLL}	V_{LL} threshold	0.7	-	1.0	V	---
V_{UVVF}	V_{PF}, V_{NF} threshold	3.5	-	6.5	V	---
V_{OL_OTP}	OTP flag output low voltage	-	-	1.0	V	V_{LL}= 3.3V, OTP = Active, $I_{PULL-UP}$= 1.0mA
I_{OTP}	Max. open drain output current	-	1.0	-	mA	V_{LL}= 3.3V, OTP = Active, $I_{PULL-UP}$= 1.0mA
T_{OTP}	Over temperature threshold	95	110	125	°C	If over temperature occurs, OTP low and all TX outputs will be HiZ.
T_{HYS}	OTP output reset hysteresis	-	7.0	-	°C	

DC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS}= 0V, V_{LL}= +3.3V, V_{DD}= +9.0V, V_{PP}-V_{PF}= +9.0V, V_{NN}- V_{NF}= -9.0V, V_{PP}= +75V, V_{NN}= -75V,T_A= 25°C)

Output P-Channel MOSFET, TXP (Mode 4)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	2.5	3.6	-	A	---
R_{ON}	Channel resistance	-	4.0	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	200*	-	pF	V_{DS} = 25V, f = 1.0MHz

Output N-Channel MOSFET, TXN (Mode 4)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	2.5	3.6	-	A	---
R_{ON}	Channel resistance	-	3.75	-	Ω	I_{SD} = 100mA
C_{OSS}	Output capacitance	-	80*	-	pF	V_{DS} = 25V, f = 1.0MHz

MOSFET Drain Bleed Resistor

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{P/N1\sim4}$	Output bleed resistance	5.0	7.5	15	kΩ	---
P_{RO}	Bleed resistors power limit	-	-	80	mW	---

Logic Inputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	(V_{LL}-0.4)	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	0.4	V	---
I_{IH}	Input logic high current	-	-	10	µA	---
I_{IL}	Input logic low current	-10	-	-	µA	---
C_{IN}	Input logic capacitance	-	-	10*	pF	---

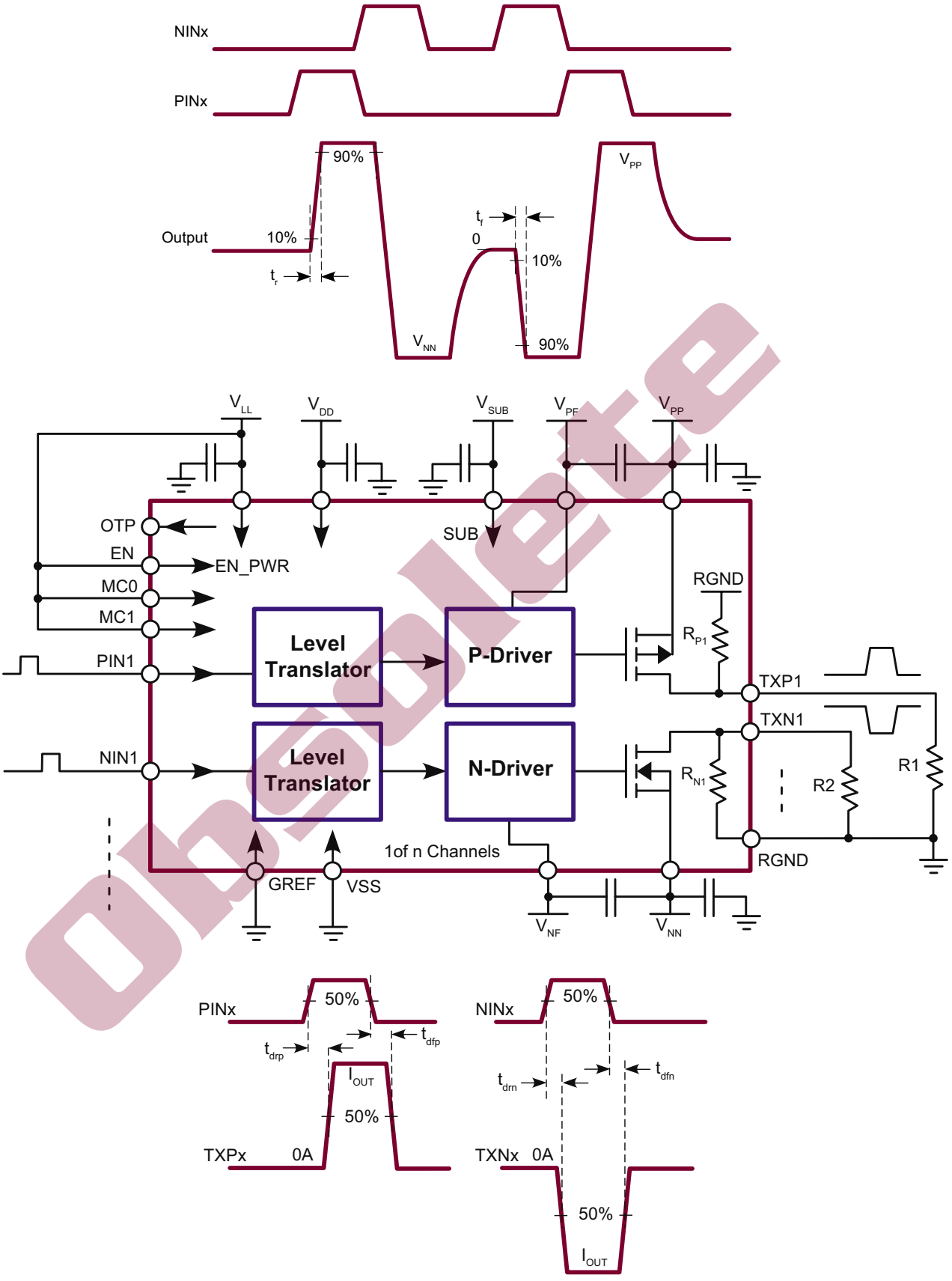
AC Electrical Characteristics

(Operating conditions, unless otherwise specified, V_{SS}= 0V, V_{LL}= +3.3V, V_{DD}= +9.0V, V_{PP}-V_{PF}= +9.0V, V_{NN}- V_{NF}= -9.0V, V_{PP}= +75V, V_{NN}= -75V,T_A= 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_r	Output rise time	-	18	-	ns	330pF//2.5kΩ load
t_f	Output fall time	-	18	-	ns	
f_{OUT}	Output frequency range	-	-	20	MHz	100Ω resistor load
HD2	Second harmonic distortion	-	-28*	-	dB	
t_{EN}	Enable time	-	180	500	µs	
t_{DIS}	Disable time	-	2.8	10	µs	
t_{dr}	Delay time on inputs rise	-	18	-	ns	2.0Ω resistor load (see timing diagram)
t_{df}	Delay time on inputs fall	-	18	-	ns	
Δt_{delay}	Delay time matching	-	±2.0	-	ns	P to N, channel to channel
t_{dm}	Delay on mode change	-	2.5	10	µs	100Ω resistor load
t_J	Delay jitter on rise or fall	-	15*	-	ps	V_{PP}/V_{NN}= +/-25V, input t_r 50% to HV_{OUT} t_r or t_f 50%, with 330pF//2.5kΩ load

* *Guaranteed by design.*

Switch AC Test Timing Diagram



Truth Table (Mode = X)

Logic Inputs			Output	
EN	PIN_x	NIN_x	TXP_x	TXN_x
1	0	0	OFF	OFF
1	**1**	0	**ON**	OFF
1	0	**1**	OFF	**ON**
1	**1**	**1**	**ON†**	**ON†**
0	X	X	OFF	OFF

† Not allowed, may damage IC.

Drive Mode Control Table

Mode	MC1	MC0	I_{SC} (A)	$R_{ON\ P}$ (Ω)	$R_{ON\ N}$ (Ω)
1	0	0	0.82	18	17
2	0	1	1.16	13	12
3	1	0	1.94	7.5	7.0
4	1	1	3.6	4.0	3.8

Notes:

1. *V_{PP}/V_{NN} = +/-75V, V_{DD} = (V_{PP} – V_{PP}) = (V_{NF}–V_{NN}) = +9.0V*
2. *I_{SC} is current into 1.0Ω to GND*
3. *R_{ON} calculated from V_{OUT} into 100Ω load*

Pin Descriptions

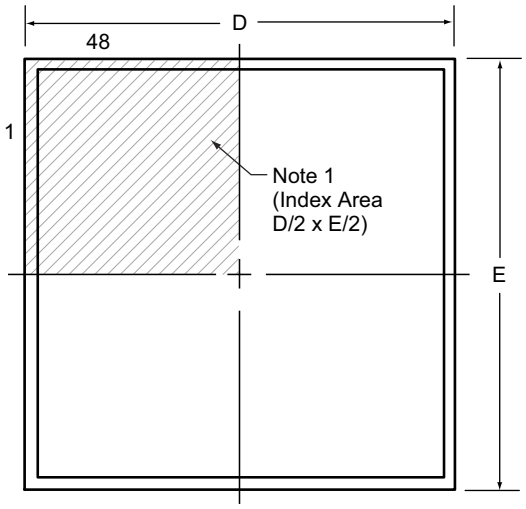
Pin #	Name	Function
1	VDD	Positive internal voltage supply (+9.0V).
2	VSS	Power supply return (0V).
3	PIN1	Input logic control of high voltage output P-FET of channel 1, Hi = ON, Low = OFF.
4	NIN1	Input logic control of high voltage output N-FET of channel 1, Hi = ON, Low = OFF.
5, 6, 7, 8	N/C	Not Connected
9	PIN2	Input logic control of high voltage output P-FET of channel 2, Hi = ON, Low = OFF.
10	NIN2	Input logic control of high voltage output N-FET of channel 2, Hi = ON, Low = OFF.
11	VSS	Power supply return (0V).
12	VDD	Positive internal voltage supply (+9.0V).
13	OTP	Over temperature protection output, open N-FET drain, active low if IC temperature >110°C.

Pin Descriptions *(cont.)*

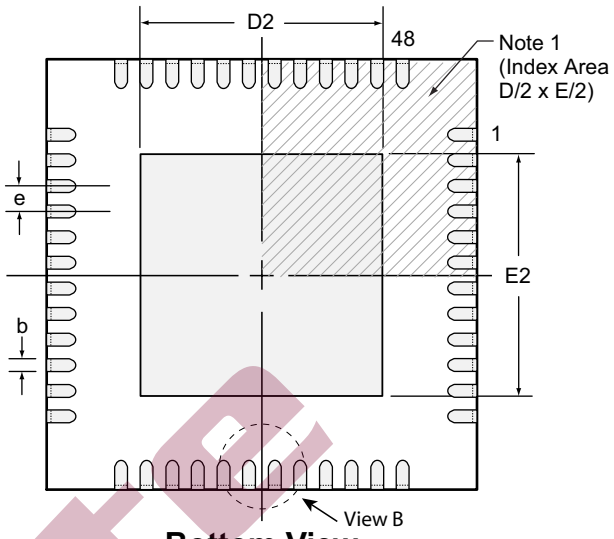
Pin #	Name	Function
14	MC1	Output current mode control pins, see Drive Mode Control Table.
15	MC0	
16	VSUB	Substrate of the IC, All VSUB pins must connect to the most positive potential of the IC externally.
17	VPF	P-FET gate driver floating power supply, (V_{PP}- V_{PF}) = +9.0V.
18,19, 20	VPP	Positive high voltage power supply (+75V).
21, 22, 23	VNN	Negative high voltage power supply (-75V).
24	VNF	N-FET gate driver floating power supply, (V_{NF}- V_{NN}) = +9.0V.
25	VSUB	Substrate of the IC, all VSUB pins must connect to the most positive potential of the IC externally.
26	RGND	Bleed resistors common return ground.
27	TXN2	Output N-FET drain (open drain output) for channel 2.
28		
29	TXP2	Output P-FET drain (open drain output) for channel 2.
30		
31	TXN1	Output N-FET drain (open drain output) for channel 1.
32		
33	TXP1	Output P-FET drain (open drain output) for channel 1.
34		
35	RGND	Bleed resistors common return ground.
36	VSUB	Substrate of the IC, all VSUB pins must connect to the most positive potential of the IC externally.
37	VNF	N-FET gate driver floating power supply, (V_{NF}- V_{NN}) = +9.0V.
38, 39, 40	VNN	Negative high voltage power supply (-75V).
41, 42, 43	VPP	Positive high voltage power supply (+75V).
44	VPF	P-FET gate driver floating power supply, (V_{PP}- V_{PF}) = +9.0V.
45	VSUB	Substrate of the IC, all VSUB pins must connect to the most positive potential of the IC externally.
46	EN	Chip power enable Hi = ON, Low = OFF.
47	GREF	Logic low reference, logic ground (0V).
48	VLL	Logic Hi voltage reference input (+3.3V).
Thermal Pad (VSUB)		Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to VSUB, the most positive potential of the IC externally.

48-Lead QFN Package Outline (K6)

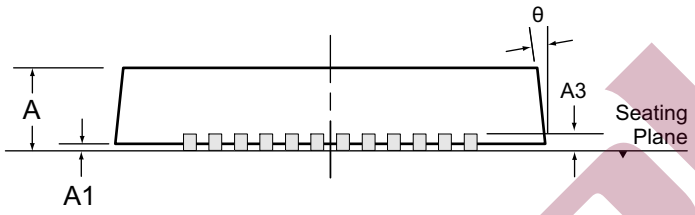
7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch



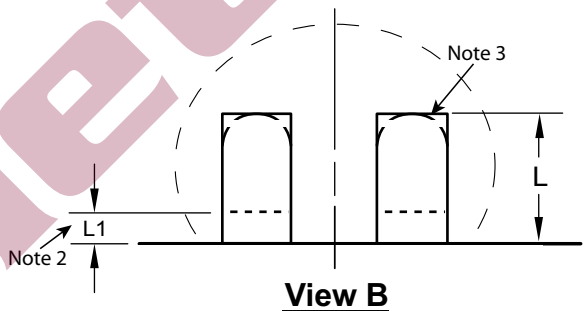
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	6.85*	1.25	6.85*	1.25	0.50 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.25	7.00	-	7.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	7.15*	5.45	7.15*	5.45		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
Supertex Doc.#: *DSPD-48QFNK67X7P050, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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