

High Voltage PIN Diode Driver

Features

- ▶ Processed with HVCMOS® technology
- ▶ 5.0V CMOS logic - low power dissipation
- ▶ DMOS output voltage up to 220V
- ▶ Low power level shifting -2.5 to 220V
- ▶ Source current 1.7mA
- ▶ Output fault detection
- ▶ Latched data output

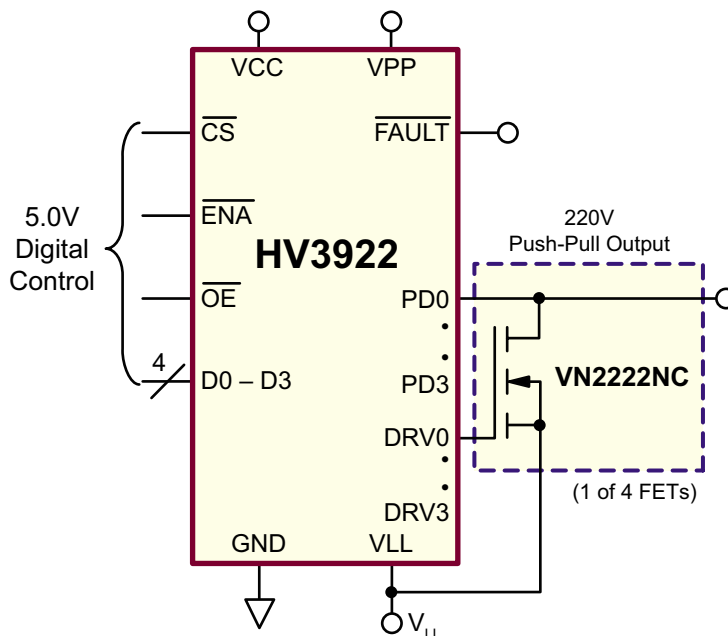
General Description

The HV3922 is a monolithic, high voltage quad-output driver that is designed to be used in conjunction with the Supertex VN2222NC, a separate N-channel DMOS FET quad array, whose device characteristics are briefly described below. Together, these devices perform a 220V push-pull function that is especially suited for driving PIN diodes in applications such as frequency-hopping radios, microwave communication systems and phased array radar.

Used as a microwave or RF switch, the HV3922 has 4 high voltage P-channel outputs: PD0, PD1, PD2 and PD3. Additional controls are Chip Select (\overline{CS}) and Output Enable (\overline{OE}) functions. The HV3922 also has an output fault detection function that protects the outputs from damage by putting them into a high impedance state when a short is detected. The HV3922 provides 4 low voltage outputs - DRV0, DRV1, DRV2 and DRV3 - that drive the gates of the 4 N-channel FETs.

The VN2222NC is an N-channel DMOS FET quad array recommended for use in conjunction with HV3922 outputs to form four 220V push-pull outputs. Each of the four devices has a max $R_{DS(ON)}$ of 1.25Ω , min $I_{D(ON)}$ of 5.0 amps, and BV_{DSS} of 220V.

Typical Application Circuit



Ordering Information

Device	Package Options		
	20-Lead Ceramic Side-Brazed .980x.280in body .200in height (max) .100in pitch	28-Lead Quad Cerpac .450x.450in body .190in height (max) .050in pitch	28-Lead PLCC .453x.453in body .180in height (max) .050in pitch
HV3922	HV3922C	HV3922DJ	HV3922PJ-G

-G indicates package is RoHS compliant ("Green")



Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{CC}	-0.5V to +7.0V
Logic input voltage	-0.3V to V_{CC} +0.3V
Supply voltage, V_{LL}	-5.0V
Supply voltage, V_{PP}	+230V
Maximum power dissipation	0.8W
Junction temperature	+150°C
Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +125°C
Lead temperature*	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

* 1.6mm from case for 10 seconds.

Recommended Operating Conditions

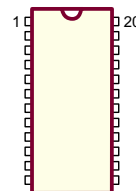
Sym	Parameter	Min	Max	Units
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IN}	DC logic input voltage	0	V_{CC}	V
V_{LL}	V_{LL} supply voltage	-3.5	-2.5	V
V_{PP}	V_{PP} supply voltage	200	220	V
$IP_{D(N)H}$	High-state continuous $P_{D(N)}$ source current	-	1.7	mA
T_A	Ambient operating temp	-55	+125	°C
C_L	$D_{RV(N)}$ load capacitance	0	0.006	µF

Notes:

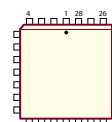
- V_{PP} rise time (dv/dt) should be less than 50V/µS.
- Power-up sequence should be the following:
 - Connect ground
 - Apply V_{CC}
 - Apply V_{LL}
 - Apply V_{PP}
 - Set all inputs to a known state.

Power-down sequence should be the reverse of the above.

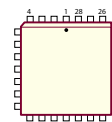
Pin Configurations



20-Lead Ceramic Side-Brazed (C)
(top view)



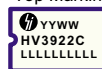
28-Lead Quad Cerpac (DJ)
(top view)



28-Lead PLCC (PJ)
(top view)

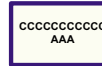
Product Markings

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number

Bottom Marking

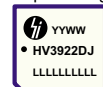


C = Country of Origin*
A = Assembler ID*

*May be part of top marking

20-Lead Ceramic Side-Brazed (C)

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number

Bottom Marking

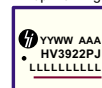


C = Country of Origin*
A = Assembler ID*

*May be part of top marking

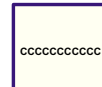
28-Lead Quad Cerpac (DJ)

Top Marking



YY = Year Sealed
WW = Week Sealed
A = Assembler ID
L = Lot Number

Bottom Marking



C = Country of Origin*

— = "Green" Packaging
*May be part of top marking

28-Lead PLCC (PJ)

Electrical Characteristics

DC Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter	Min	Max	Units	Conditions
I_{CCQ}	Quiescent V_{CC} supply current	-	1.0	mA	$V_{CC} = 5.5V$ all outputs open.
I_{LLQ}	Quiescent V_{LL} supply current	-	4.0	mA	$V_{LL} = -3.5V$ $D_{RV(N)}$ high or low.
I_{PPQ}	Quiescent V_{PP} supply current	-	100	μA	$V_{PP} = 220V$ $P_{D(N)}$ high or low.
I_{IH}	High-level logic current	-	10	μA	$V_{IN} = V_{CC}$
I_{IL}	Low-level logic current	-	10	μA	$V_{IN} = 0V$
V_{FH}	High-level logic output voltage (fault detect)	4.4	-	V	$V_{CC} = 4.5V$, $I_O = 20\mu A$
V_{FL}	Low-level logic output voltage (fault detect)	-	0.1	V	$V_{CC} = 5.5V$, $I_O = -20\mu A$
V_{DH}	$P_{D(N)}$ high-level output voltage	198	-	V	$V_{PP} = 203V$, $I_{OH} = 1.7mA$
	$D_{RV(N)}$ high-level output voltage	4.0	-	V	$V_{CC} = 4.5V$, $I_{OH} = 100\mu A$
V_{DL}	$D_{RV(N)}$ low-output voltage	-	-2.3	V	$V_{LL} = -2.5V$, $I_{DL} = -500\mu A$
V_{TH}	Fault threshold trip point for $P_{D(N)}$ output high	$0.5 \times V_{PP}$ fault	$0.85 \times V_{PP}$ fault	V	$P_{D(N)} = HIGH$, $\overline{OE} = V_{CC}$
V_{TL}	Fault threshold trip point for $P_{D(N)}$ output Hi-Z	$V_{(PDN)} = 0$	$V_{(PDN)} = 25$	V	$P_{D(N)} = Hi-Z$, $\overline{OE} = V_{CC}$

AC Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter	Min	Max	Units	Conditions
t_{WCS}	\overline{CS} pulse to latch data	100	-	ns	$V_{CC} = 4.5V$, $\overline{ENA} = 0V$
t_{WENA}	\overline{ENA} pulse width to latch data	100	-	ns	$V_{CC} = 4.5V$, $\overline{CS} = 0V$
t_{WOE}	\overline{OE} pulse width	10	50	μs	$V_{CC} = 4.5V$, $\overline{OE} = 0V$, $V_{PP} = 220V$, $P_{D(N)}$ LOAD = 20K Ω to GND
		16	50	μs	$V_{PP} = 220V$, $P_{D(N)}$ LOAD = 20K Ω and 3000pF to GND
t_T	Input transition rise and fall time	0	200	ns	$V_{CC} = 4.5V$
t_{SU1}	Set-up time D_N and \overline{CS} to \overline{ENA}	150	-	ns	$V_{CC} = 4.5V$
t_{SU2}	Set-up time \overline{ENA} to \overline{OE} falling edge	150	-	ns	$V_{CC} = 4.5V$
t_H	Hold time	5.0	-	ns	$V_{CC} = 4.5V$
C_{IN}	Input capacitance	-	10	pF	Not tested, reference only
t_{OH}	$P_{D(N)}$ transition time from \overline{OE} low to $P_{D(N)}$ high/low	1.0	50	μs	$V_{PP} = 220V$, $P_{D(N)}$ output loaded by 20K Ω and 3000pF to GND

Function Table

Input					Output				
\overline{CS}	\overline{ENA}	\overline{OE}	Data $D_{(N)}$	V_{TH} Level ¹	Internal Latch Q(n)	Internal FF QF(n)	$P_{D(N)}$	$D_{RV(N)}$	\overline{Fault}
H	X	H	X	Pass	Previous state Q(n-1)	Previous state QF(n-1)	Previous state	Previous state	VFH
X	H	H	X	Pass	Previous state Q(n-1)	Previous state QF(n-1)	Previous state	Previous state	VFH
L	L	H	H	Pass	Set	Previous state QF(n-1)	Previous state	Previous state	VFH
L	L	H	L	Pass	Reset	Previous state QF(n-1)	Previous state	Previous state	VFH
L	L	↓	H	P/F	Set	Set	VDH	VDL	VFH
L	L	↓	L	P/F	Reset	Reset	Hi-Z	VDH	VFH
H	X	↓	X	P/F	Previous state Q(n-1)	Set if Q(n-1) = Set	VDH	VDL	VFH
H	X	↓	X	P/F	Previous state Q(n-1)	Reset if Q(n-1) = Reset	Hi-Z	VDH	VFH
X	H	↓	X	P/F	Previous state Q(n-1)	Set if Q(n-1) = Set	VDH	VDL	VFH
X	H	↓	X	P/F	Previous state Q(n-1)	Reset if Q(n-1) = Reset	Hi-Z	VDH	VFH
X	X	H	X	Fail	X	X	Hi-Z	VDL	VFL

(At Power Up)

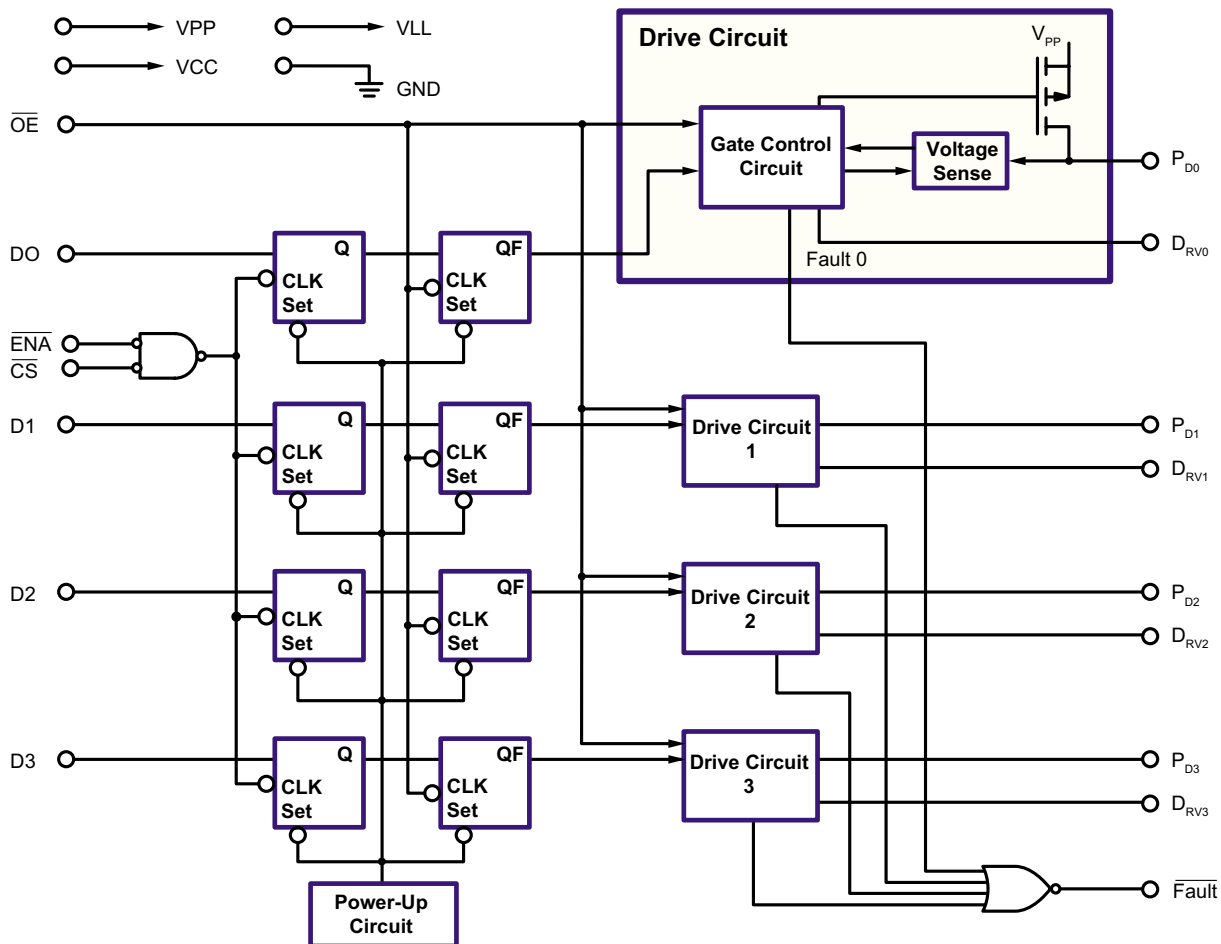
X	X	H	X	P/F	Set	Set	VDH	VDL	VFH
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Notes:

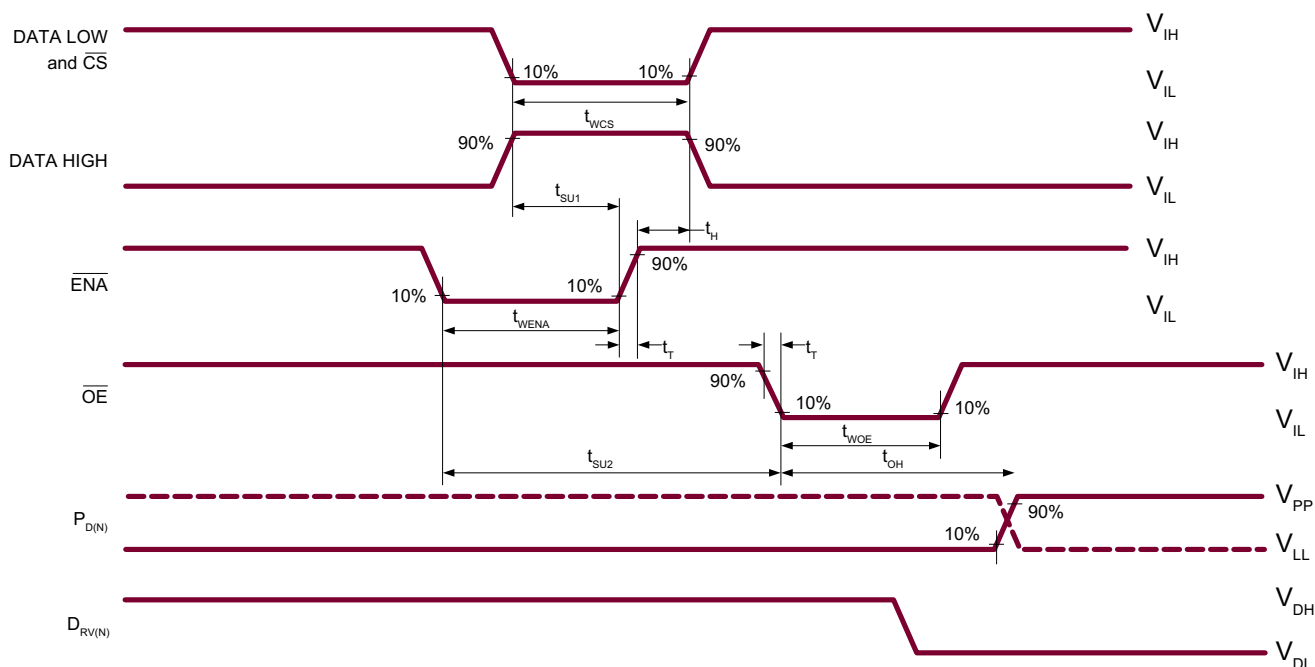
- The output threshold is internally tested for each $P_{D(N)}$ output; the pass condition occurs when $\overline{OE} = H$ and:
 - $P_{D(N)}$ driving high with output $> V_{TH(MAX)}$, or may occur if $P_{D(N)}$ driving high and $V_{TH(MIN)} < output < V_{TH(MAX)}$.
OR
 - $P_{D(N)}$ driving Low with output $< V_{TH(MIN)}$, or may occur if $P_{D(N)}$ driving low and $V_{TL(MIN)} < output < V_{TL(MAX)}$.
- \overline{FAULT} output = V_{FL} indicates a fault has been detected in at least one of the $P_{D(N)}$ output loads when $\overline{OE} = H$. All other outputs shall function normally when a fault condition has been detected for one of the outputs. The \overline{FAULT} output shall remain in the low state, regardless of the state of the output which initiated the fault status, until the next falling edge of \overline{OE} . Whenever $\overline{OE} = L$, the \overline{FAULT} output is forced to V_{FHP} and the fault latch is reset. If the fault condition persists, the fault response repeats each time the \overline{OE} input is set to H.
- Hi-Z indicates no current is sourced to output $P_{D(N)}$.
- P/F indicates "Pass" or "Fail" fault threshold conditions.

- ↓ = High to Low transition
- H = High
- L = Low
- X = Don't care

Functional Block Diagram



Timing Diagram



Pin Description - 20-Lead Ceramic Side-Brazed (C)

Pin #	Function
1	D1
2	D2
3	D3
4	VLL
5	GND
6	DRV3
7	DRV2
8	PD3
9	PD2
10	PD1

Pin #	Function
11	PD0
12	DRV1
13	DRV0
14	VPP
15	VCC
16	$\overline{\text{ENA}}$
17	$\overline{\text{OE}}$
18	$\overline{\text{CS}}$
19	$\overline{\text{FAULT}}$
20	D0

Pin Description - 28-Lead Quad Cerpac (DJ)

Pin #	Function
1	D1
2	D2
3	D3
4	NC
5	VLL
6	GND
7	NC
8	DRV3
9	DRV2
10	NC
11	PD3
12	NC
13	PD2
14	NC

Pin #	Function
15	PD1
16	PD0
17	NC
18	DRV1
19	DRV0
20	NC
21	VPP
22	NC
23	VCC
24	$\overline{\text{ENA}}$
25	$\overline{\text{OE}}$
26	$\overline{\text{CS}}$
27	$\overline{\text{FAULT}}$
28	D0

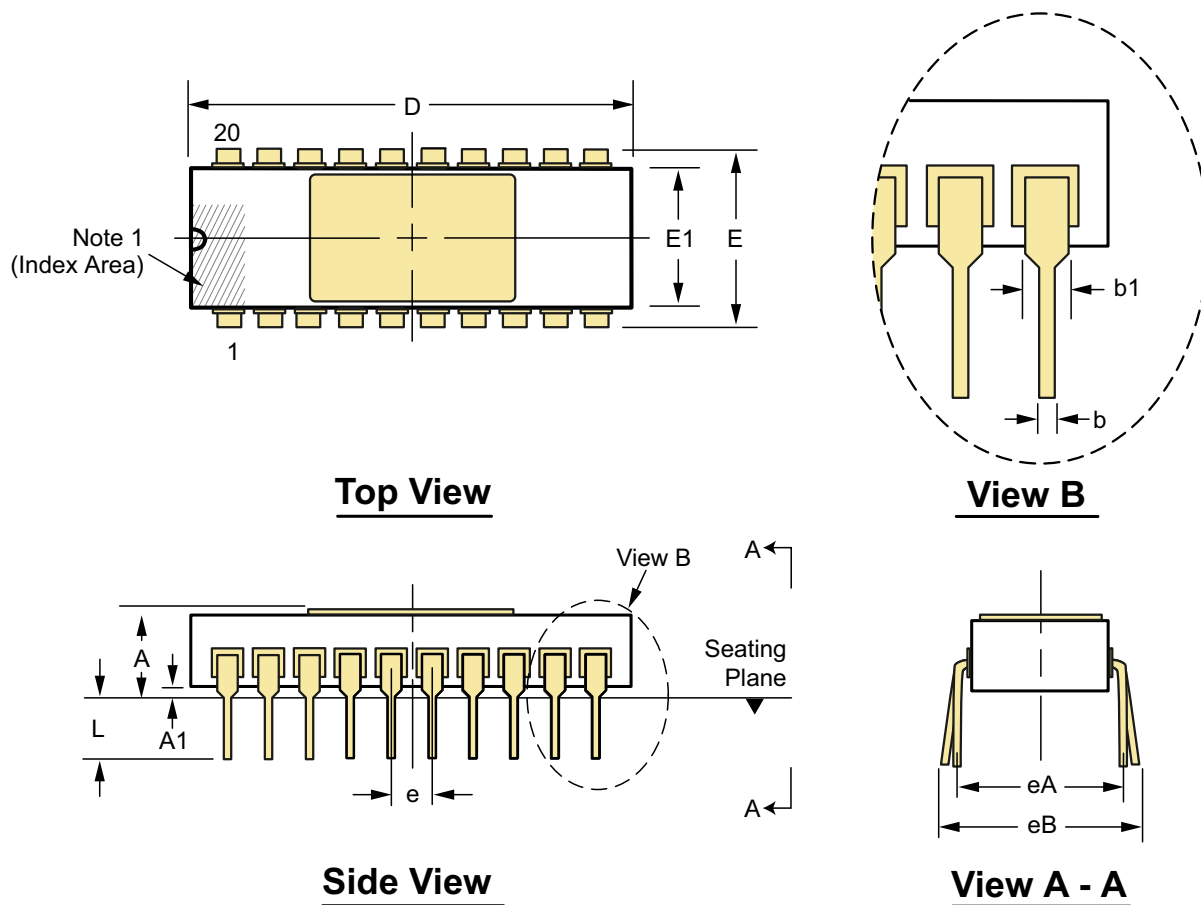
Pin Description - 28-Lead PLCC (PJ)

Pin #	Function
1	D1
2	D2
3	D3
4	NC
5	VLL
6	GND
7	NC
8	DRV3
9	DRV2
10	NC
11	PD3
12	NC
13	PD2
14	NC

Pin #	Function
15	PD1
16	PD0
17	NC
18	DRV1
19	DRV0
20	NC
21	VPP
22	NC
23	VCC
24	$\overline{\text{ENA}}$
25	$\overline{\text{OE}}$
26	$\overline{\text{CS}}$
27	$\overline{\text{FAULT}}$
28	D0

20-Lead Ceramic Side-Brazed Package Outline (C)

.980x.280in. body, .200in. height (max), .100in. pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	b	b1	D	E	E1	eA	eB	e	L	
Dimension (inches)	MIN	.085	.025	.015	.045	.980	.300	.280	.300 REF	.100 BSC	.125	
	NOM	-	-	-	-	-	-	-			.300 [†]	-
	MAX	.200	.070	.022	.065	1.020	.325	.310			.400	.200

JEDEC Registration MS-015, Variation AE, Issue A, July, 1990.

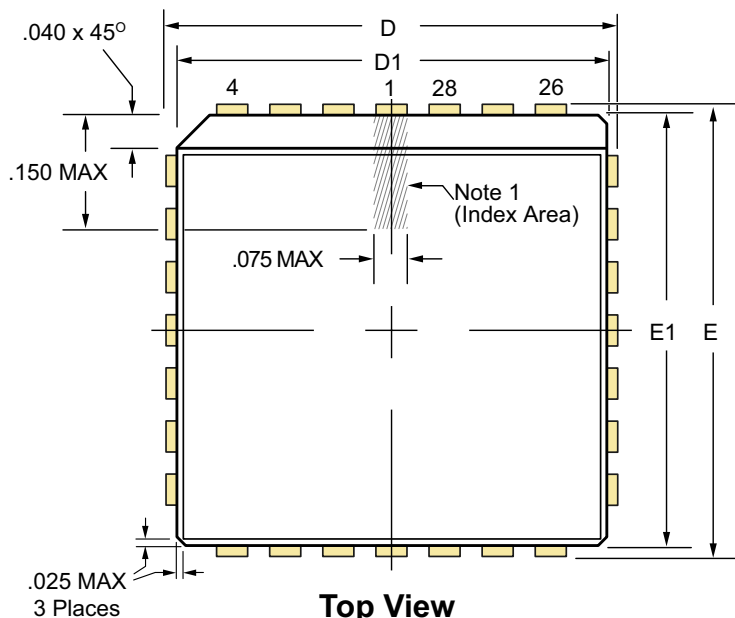
[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

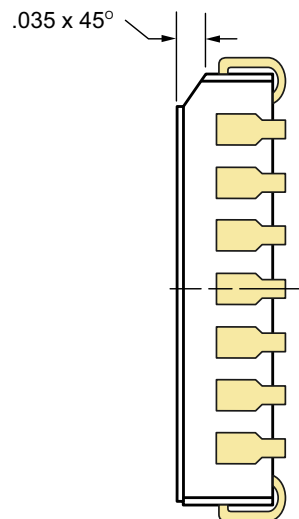
Supertex Doc.#: DSPD-20CDIPCNC, Version D041309.

28-Lead Quad Cerpac Package Outline (DJ)

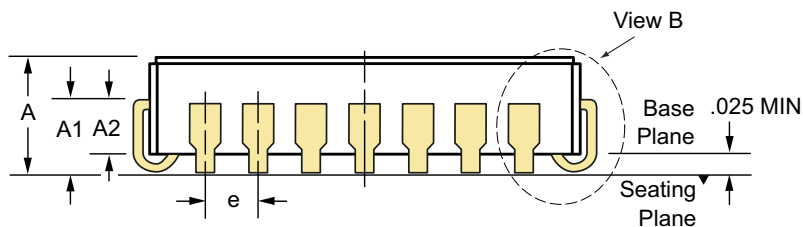
.450x.450in. body, .190in. height (max), .050in. pitch



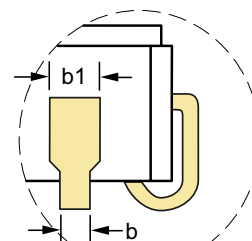
Top View



Vertical Side View



Horizontal Side View



View B

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.155	.090	.060 REF	.017	.026	.485	.430	.485	.430	.050 BSC
	NOM	.172	.100		.019	.029	.490	.450	.490	.450	
	MAX	.190	.120		.021	.032	.495	.465	.495	.465	

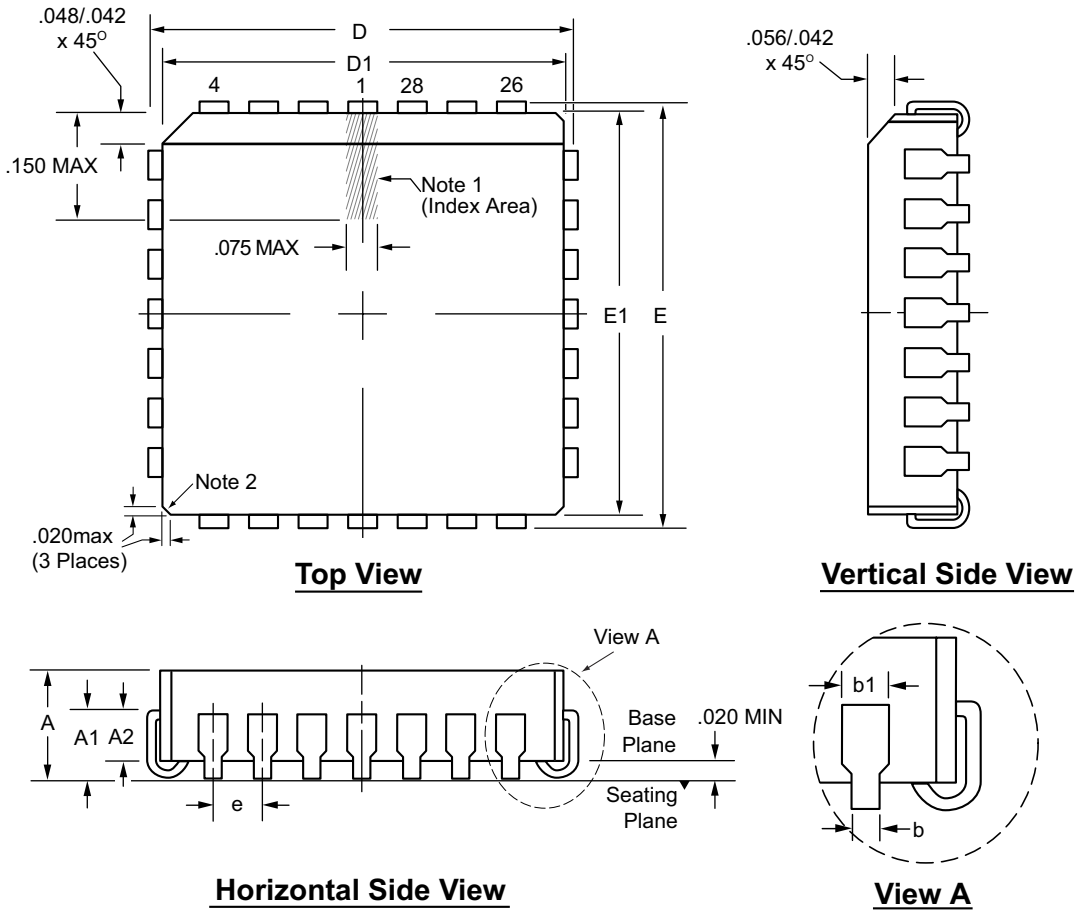
JEDEC Registration MO-087, Variation AA, Issue B, August, 1991.

Drawings not to scale.

Supertex Doc.#: DSPD-28CERPACDJ, Version B090808.

28-Lead PLCC Package Outline (PJ)

.453x.453in. body, .180in. height (max), .050in. pitch



Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC
	NOM	.172	.105	-	-	-	.490	.453	.490	.453	
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456	

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

Supertex Doc. #: DSPD-28PLCCPJ, Version A092408.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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