MRF24J40

IEEE 802.15.4™ 2.4 GHz RF Transceiver

Devices Included:

- MRF24J40

Features:

- Complete IEEE 802.15.4 Specification Compliant
- Supports MiWi™, ZigBee™ and Proprietary Protocols
- Simple, 4-Wire SPI Interface
- Integrated 20 MHz and 32.768 kHz Oscillator Drive
- 20 MHz Reference Clock Output:
  - Available to drive microcontroller oscillator
- Supports Power-Saving mode
- Low-Current Consumption, Typical 18 mA in RX mode and 22 mA in TX mode
- Typical 2 μA Sleep mode
- Small, 40-Pin Leadless QFN 6x6 mm^2 Package

RF/Analog Features:

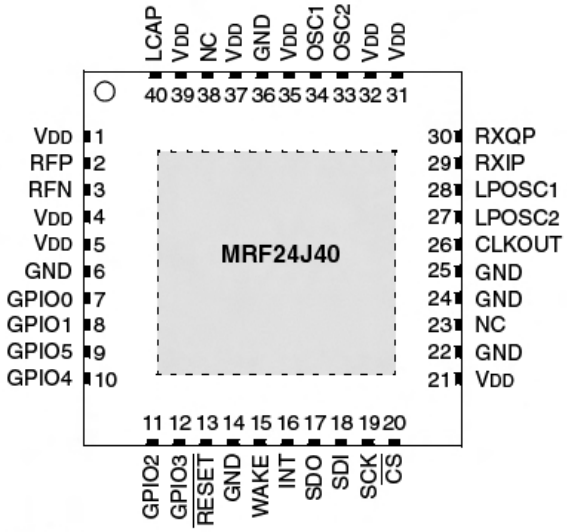
- ISM Band 2.405-2.48 GHz Operation
- -91 dBm Typical Sensitivity and +5 dBm Maximum Input Level
- +0 dBm Typical Output Power and 38.75 dB TX Power Control Range
- Differential RF Input/Output and Integrated TX/RX Switch
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver and RSSI Dynamic Range

MAC/Baseband Features:

- Hardware CSMA-CA Mechanism, Automatic ACK Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports all CCA modes and RSS/LQI
- Automatic Packet Retransmit Capability
- Supports In-Line or Stand-Alone modes for both Encryption and Decryption

Pin Diagram:

40-Pin QFN



Note: Backside center pad is GND.

1.0 OVERVIEW

The MRF24J40 is an IEEE 802.15.4-2003 compliant transceiver supporting MiWi™, ZigBee™ and other proprietary protocols. The MRF24J40 integrates wireless RF, PHY layer baseband and MAC layer architectures that can be combined with a simple microprocessor to apply low data rate to a multitude of applications that include home automation, consumer electronics, PC peripherals, toys, industrial automation and more. The MRF24J40 device integrates a receiver, transmitter, VCO and PLL into a single integrated circuit. It uses advanced radio architecture to minimize external part count and power consumption. The MRF24J40 MAC/baseband provides hardware architecture for both IEEE 802.15.4 MAC and PHY layers. It mainly consists of TX/RX FIFOs, a CSMA-CA controller, superframe constructor, receive frame filter, security engine and digital signal processing module. The MRF24J40 is fabricated by advanced 0.18 μm CMOS process and is offered in a 40-pin QFN 6x6 mm^2 package.

Features are summarized in Table 1-1 and the pinout for this device is listed in Table 1-2.

The MRF24J40 consists of four major functional blocks:

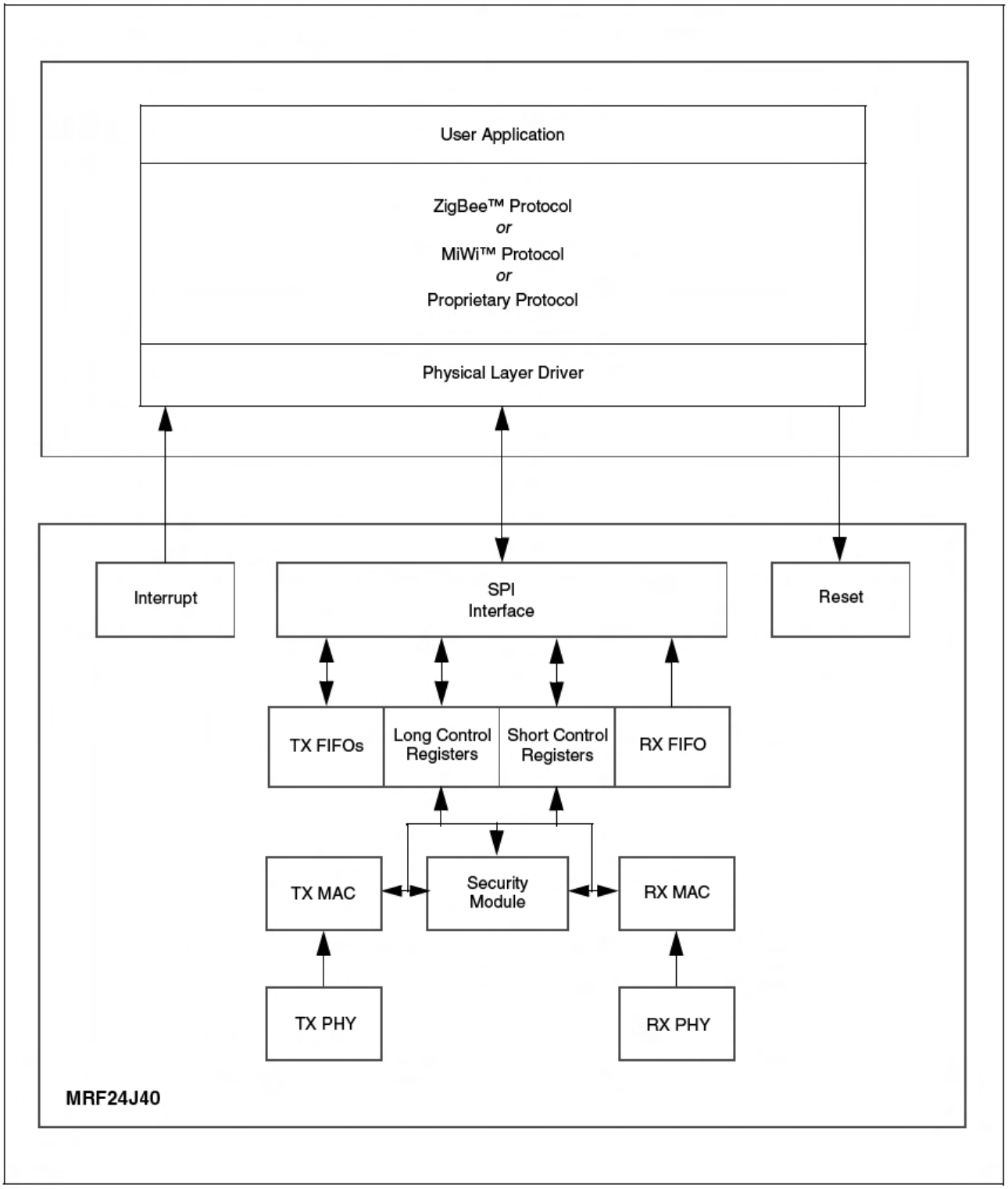
1. An SPI interface that serves as a communication channel between the host controller and the MRF24J40.
2. Control registers which are used to control and monitor the MRF24J40.
3. The MAC (Medium Access Control) module that implements IEEE 802.3™ compliant MAC logic.
4. The PHY (Physical Layer) driver that encodes and decodes the analog data.

The device also contains other support blocks, such as the on-chip voltage regulator, security module and system control logic.

TABLE 1-1: DEVICE FEATURES FOR THE MRF24J40 (40-PIN DEVICE)

Features	MRF24J40
IEEE 802.15.4™ Specification Compliant	Yes
Integrated Oscillator Drive	20 MHz and 32.768 kHz
Reference Clock Output	20 MHz
Power-Saving Mode Support	Yes
Current Consumption	Typical 18 mA in RX and 22 mA in TX
Sleep Mode	2 μA Typical
Serial Communications	SPI (4-wire)
Packages	40-Pin Leadless QFN 6x6 mm^2

FIGURE 1-1: MRF24J40 ARCHITECTURE BLOCK DIAGRAM



1.1 Pin Descriptions

TABLE 1-2: MRF24J40 PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
2	RFP	AIO	Differential RF input/output (+).
3	RFN	AIO	Differential RF input/output (-).
4	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
5	VDD	Power	Guard ring power supply. Bypass with a capacitor as close to the pin as possible.
6	GND	Ground	Guard ring ground.
7	GPIO0	DIO	General purpose digital I/O, also used as external PA enable.
8	GPIO1	DIO	General purpose digital I/O, also used as external TX/RX switch control.
9	GPIO5	DIO	General purpose digital I/O.
10	GPIO4	DIO	General purpose digital I/O.
11	GPIO2	DIO	General purpose digital I/O, also used as external TX/RX switch control.
12	GPIO3	DIO	General purpose digital I/O.
13	$\overline{\text{RESET}}$	DI	Global hardware Reset pin active-low.
14	GND	Ground	Ground for digital circuit.
15	WAKE	DI	External wake-up trigger.
16	INT	DO	Interrupt pin to microcontroller.
17	SDO	DIO	Serial interface data output from MRF24J40.
18	SDI	DIO	Serial interface data input to MRF24J40.
19	SCK	DI	Serial interface clock.
20	$\overline{\text{CS}}$	DI	Serial interface enable.
21	VDD	Power	Digital circuit power supply. Bypass with a capacitor as close to the pin as possible.
22	GND	Ground	Ground for digital circuit.
23	NC	—	No Connection, do not connect anything to this pin.
24	GND	Ground	Ground for digital circuit.
25	GND	Ground	Ground for digital circuit.
26	CLKOUT	DIO	20/10/5/2.5 MHz clock output.
27	LPOSC2	AI	32 kHz crystal input (-).
28	LPOSC1	AI	32 kHz crystal input (+).
29	RXIP	AO	Analog RX I channel output (+).
30	RXQP	AO	Analog RX Q channel output (+).
31	VDD	Power	Power supply for band gap reference circuit. Bypass with a capacitor as close to the pin as possible.
32	VDD	Power	Power supply for analog circuit. Bypass with a capacitor as close to the pin as possible.
33	OSC2	AI	20 MHz crystal input (-).
34	OSC1	AI	20 MHz crystal input (+).
35	VDD	Power	PLL power supply. Bypass with a capacitor as close to the pin as possible.
36	GND	Ground	Ground for PLL.
37	VDD	Power	Charge pump power supply. Bypass with a capacitor as close to the pin as possible.
38	NC	—	No Connection.
39	VDD	Power	VCO supply. Bypass with a capacitor as close to the pin as possible.
40	LCAP	—	PLL loop filter external capacitor. Connected to external 180 pF capacitor.

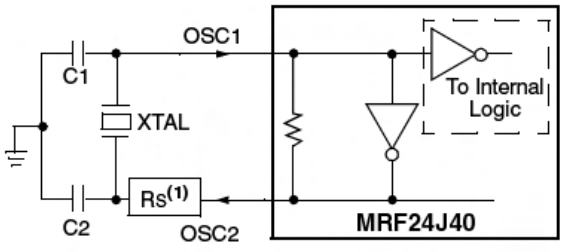
Legend: A = Analog, D = Digital, I = Input, O = Output

2.0 EXTERNAL CONNECTIONS

2.1 Oscillator

The MRF24J40 is designed to operate at 20 MHz with a crystal connected to the OSC1 and OSC2 pins. A typical oscillator circuit is shown in Figure 2-1.

FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION



Note 1: A series resistor (Rs) may be required for AT strip cut crystals.

2.2 Oscillator Start-up

The MRF24J40 PHY has an internal PLL that must lock before the device is capable of transmitting or receiving packets. After a full Power-on Reset, the device requires 2 ms to lock. During this delay, all registers and buffer memory may still be read and written to through the SPI bus. However, software should not attempt to transmit any packets (set the TXRTS (TXNMTRIG<0>)), or access any MAC or PHY registers during this period.

2.3 CLKOUT Pin

The clock out pin is provided to the system designer for use as the host controller clock or as a clock source for other devices in the system. The CLKOUT has an internal prescaler which can divide the output by 1, 2, 4 or 8. The CLKOUT function is enabled via the CLKCTRL register (Register 2-1) and the prescaler is selected via the RFCTRL7 register (Register 2-2).

REGISTER 2-1: CLKCTRL: DIVIDED SLEEP CLOCK (50 kHz) SELECTION REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	—	$\overline{\text{CLKOEN}}$	SCLKDIV<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Maintain as '0'

bit 6 **Unimplemented:** Read as '0'

bit 5 **$\overline{\text{CLKOEN}}$:** 20 MHz Clock Output Enable bit
1 = Disable
0 = Enable

bit 4-0 **SCLKDIV4:SCLKDIV0:** Divided SLPCLK Selection bits
Divided by 2^n.

REGISTER 2-2: RFCTRL7: RF CONTROL REGISTER 7

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
SLPCLK<7:6>		—	—	—	—	CLKDIV<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SLPCLK7:SLPCLK6:** Sleep Clock Selection bits
00 = None
01 = External crystal
10 = Internal ring oscillator
11 = Reserved

bit 5-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKDIV1:CLKDIV0:** MRF24J40 Clock Output Frequency bits
00 = 2.5 MHz
01 = 5 MHz
10 = 10 MHz
11 = 20 MHz

To create a clean clock signal, the CLKOUT pin is held low for a period when power is first applied. After the Power-on Reset ends, the Oscillator Start-up Timer (OST) will begin counting. When the OST expires, the CLKOUT pin will begin outputting its default frequency of 2.5 MHz (main clock divided by 8).

2.4 RF Output

RFP and RFN are the differential RF input/output pins. These pins are connected to the antenna of the system, as seen in the example circuit diagram in Figure A-1. L5 is an RF choke. This inductor filters out non 2.4 GHz voltages. L3, L4, C37 and C43 act as a balun. The balun converts a differential unbalanced input and converts it to a balanced singled-ended output and visa versa. L1, C23 and C38 form a pi-type matching circuit to match the impedance of the balun to the impedance of the antenna. This circuit is not required if the impedance of the balun matches the antenna impedance. Refer to **Appendix A.1 "Layout Considerations and RF Measurements"** for more details about board layout and part selection concerning the RF output pins.

3.0 MEMORY ORGANIZATION

All memory in the MRF24J40 is implemented as static RAM. There are five types of memory in the MRF24J40:

- Short Address Control Registers
- Long Address Control Registers
- Transmit Buffers
- Receive Buffers
- Security Buffer

The control registers, both long and short, are used for configuration, control, and status retrieval of the MRF24J40. The control registers are directly read and written to by the SPI interface. The transmit and receive buffers contain transmit and receive memory used by the controller to transmit and receive data.

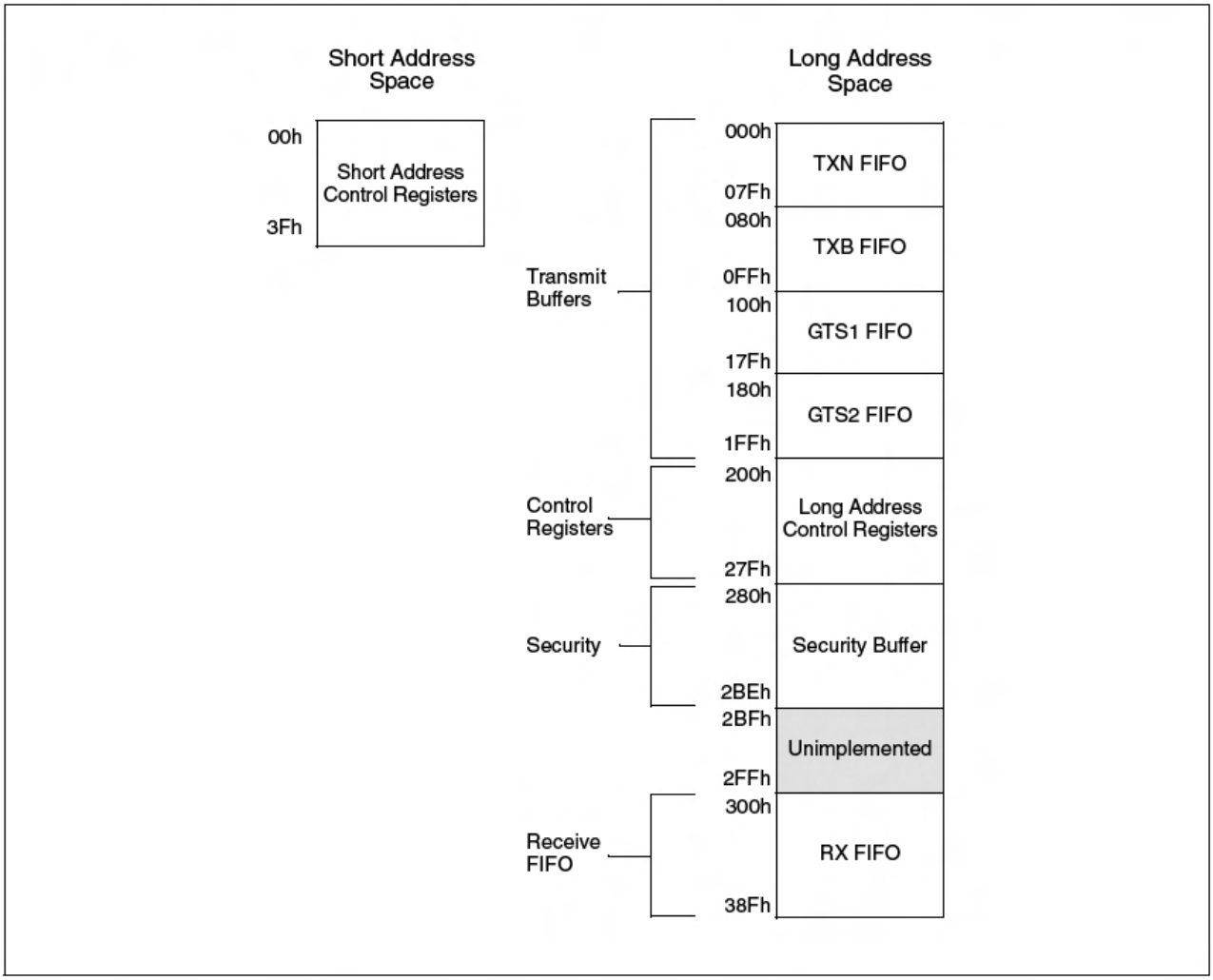
The security buffer provides an engine for the MRF24J40 MAC, which is compatible with the IEEE 802.15.4 LR-WPAN (ZigBee). The security buffer contains the following features:

- Transmit encryption and receive decryption.
- Seven-mode security suite.
- 64 x 8-bit security RAM for security suite storing; one receive key and three transmit keys for TX FIFOs. Beacon FIFO and GTS2 FIFO share the same key space since they will not conflict with each other. Normal FIFO and GTS1 FIFO both have their own transmit key.
- Security of APL and NWK layers can be achieved using the same engine. The upper layer security function is compliant to the ZigBee V1.0 and ZigBee 2006 specifications.

The SPI interface used to write and read these registers is described in **Section 4.0 "Serial Peripheral Interface (SPI)"**.

Figure 3-1 shows the data memory organization for the MRF24J40.

FIGURE 3-1: MRF24J40 MEMORY SPACE



3.1 Control Registers

The control registers provide the main interface between the host controller and the on-chip RF controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

The control register memory is partitioned into the short address control register section and the long address control register section.

All reserved registers may be read but their contents must not be changed. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

FIGURE 3-2: MRF24J40 SHORT ADDRESS CONTROL REGISTER MAPPING

00h	RXMCR	10h	—	20h	—	30h	—
01h	PANIDL	11h	—	21h	—	31h	ISRSTS
02h	PANIDH	12h	—	22h	—	32h	INTMSK
03h	SADRL	13h	—	23h	—	33h	GPIO
04h	SADRH	14h	—	24h	TXSR	34h	TRISGPIO
05h	EADR0	15h	—	25h	—	35h	—
06h	EADR1	16h	—	26h	—	36h	RFCTL
07h	EADR2	17h	—	27h	—	37h	—
08h	EADR3	18h	—	28h	—	38h	—
09h	EADR4	19h	—	29h	—	39h	—
0Ah	EADR5	1Ah	—	2Ah	—	3Ah	BBREG2
0Bh	EADR6	1Bh	TXNMTRIG	2Bh	—	3Bh	—
0Ch	EADR7	1Ch	—	2Ch	—	3Ch	—
0Dh	RXFLUSH	1Dh	—	2Dh	—	3Dh	—
0Eh	—	1Eh	—	2Eh	—	3Eh	BBREG6
0Fh	—	1Fh	—	2Fh	—	3Fh	RSSITHCCA

FIGURE 3-3: MRF24J40 LONG ADDRESS CONTROL REGISTER MAPPING

200h	RFCTRL0	210h	—	220h	CLKCTRL	230h	—	240h	—
201h	—	211h	CLKINTCR	221h	—	231h	—	241h	—
202h	RFCTRL2	212h	—	222h	—	232h	—	242h	—
203h	RFCTRL3	213h	—	223h	—	233h	—	243h	—
204h	—	214h	—	224h	—	234h	—	244h	—
205h	—	215h	—	225h	—	235h	—	245h	—
206h	RFCTRL6	216h	—	226h	—	236h	—	246h	—
207h	RFCTRL7	217h	—	227h	—	237h	—	247h	—
208h	RFCTRL8	218h	—	228h	—	238h	—	248h	—
209h	—	219h	—	229h	—	239h	—	249h	—
20Ah	—	21Ah	—	22Ah	—	23Ah	—	24Ah	—
20Bh	—	21Bh	—	22Bh	—	23Bh	—	24Bh	—
20Ch	—	21Ch	—	22Ch	—	23Ch	—	24Ch	—
20Dh	—	21Dh	—	22Dh	—	23Dh	—		
20Eh	—	21Eh	—	22Eh	—	23Eh	—		
20Fh	—	21Fh	—	22Fh	—	23Fh	—		

3.2 MRF24J40 Address Summary

TABLE 3-1: REGISTER FILE SHORT ADDRESS SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on page:
RXMCR	$\overline{\text{TXCRCEN}}$	BBLPBK	$\overline{\text{ACKEN}}$	MACLPBK	PANCOORD	COORD	$\overline{\text{RXCRCEN}}$	PROMI	0000 0000	21
PANIDL	MAC PAN Low Byte (PANL<7:0>)								0000 0000	26
PANIDH	MAC PAN High Byte (PANH<15:8>)								0000 0000	26
SADRL	MAC Short Address Low Byte (SADDRL<7:0>)								0000 0000	27
SADRH	MAC Short Address High Byte (SADDRH<15:8>)								0000 0000	27
EADR0	LSB of EUI (EADR0<7:0>)								0000 0000	26
EADR1	Byte 2 of EUI (EADR1<15:8>)								0000 0000	26
EADR2	Byte 3 of EUI (EADR2<23:16>)								0000 0000	26
EADR3	Byte 4 of EUI (EADR3<31:24>)								0000 0000	26
EADR4	Byte 5 of EUI (EADR4<39:32>)								0000 0000	26
EADR5	Byte 6 of EUI (EADR5<47:40>)								0000 0000	26
EADR6	Byte 7 of EUI (EADR6<55:48>)								0000 0000	26
EADR7	MSB of EUI (EADR7<63:56>)								0000 0000	26
RXFLUSH	—	r	r	$\overline{\text{RXWRTBLK}}$	CMDONLY	DATAONLY	BCNONLY	RXFLUSH	-000 0000	34
TXNMTRIG	—	—	—	PENDACK	INDIRECT	ACKREQ	SECEN	TXRTS	---0 0000	30
TXSR	TXRETRY<7:6>		CCAFAIL	r	r	r	r	r	0000 0000	31
ISRSTS	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	GTS2TXIF	GTS1TXIF	TXIF	0000 0000	36
INTMSK	SLPMSK	WAKEMSK	HSYMTMRMSK	SECMSK	RXMSK	GTS2TXMSK	GTS1TXMSK	TXMSK	1111 1111	37
GPIO	—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	--00 0000	39
TRISGPIO	—	—	TRISGP5	TRISGP4	TRISGP3	TRISGP2	TRISGP1	TRISGP0	--00 0000	40
RFCTL	r	—	—	r	r	RFRST	r	r	0--0 0000	24
BBREG2	CCAMODE<7:6>		CCATHRES<5:2>				—	—	0000 00--	25
BBREG6	RSSIREQ	RXRSSI	r	r	r	r	r	RSSIRDY	0000 0001	25
RSSITHCCA	RSSITHRES<7:0>								0000 0000	23

Legend: - = unimplemented, r = reserved. Shaded cells are unimplemented, read as '0'.

TABLE 3-2: REGISTER FILE LONG ADDRESS SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on page:
RFCTRL0	CHANNEL<7:4>				—	—	—	—	0000 ----	24
RFCTRL2	RFPLL	r	r	r	r	—	—	—	0000 0---	22
RFCTRL3	TXPOWER<7:3>					—	—	—	0000 0---	22
RFCTRL6	TXFIL	—	r	r	BATMONEN	—	—	—	0-00 0---	23
RFCTRL7	SLPCLK<7:6>		—	—	—	—	CLKDIV<1:0>		00-- --00	8
RFCTRL8	—	—	—	RF_VCO	—	—	—	SLPCLKOUT	---0 ---0	23
CLKINTCR	—	—	—	—	—	—	INTEDGE	$\overline{\text{SLPCLKEN}}$	---- --00	38
CLKCTRL	r	—	$\overline{\text{CLKOEN}}$	SCLKDIV<4:0>					0-00 0000	7

Legend: - = unimplemented, r = reserved. Shaded cells are unimplemented, read as '0'.

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The control registers provide the main interface between the host controller and the on-chip RF controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

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03h	SADRL	13h	—	23h	—	33h	GPIO
04h	SADRH	14h	—	24h	TXSR	34h	TRISGPIO
05h	EADR0	15h	—	25h	—	35h	—
06h	EADR1	16h	—	26h	—	36h	RFCTL
07h	EADR2	17h	—	27h	—	37h	—
08h	EADR3	18h	—	28h	—	38h	—
09h	EADR4	19h	—	29h	—	39h	—
0Ah	EADR5	1Ah	—	2Ah	—	3Ah	BBREG2
0Bh	EADR6	1Bh	TXNMTRIG	2Bh	—	3Bh	—
0Ch	EADR7	1Ch	—	2Ch	—	3Ch	—
0Dh	RXFLUSH	1Dh	—	2Dh	—	3Dh	—
0Eh	—	1Eh	—	2Eh	—	3Eh	BBREG6
0Fh	—	1Fh	—	2Fh	—	3Fh	RSSITHCCA

FIGURE 3-3: MRF24J40 LONG ADDRESS CONTROL REGISTER MAPPING

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201h	—	211h	CLKINTCR	221h	—	231h	—	241h	—
202h	RFCTRL2	212h	—	222h	—	232h	—	242h	—
203h	RFCTRL3	213h	—	223h	—	233h	—	243h	—
204h	—	214h	—	224h	—	234h	—	244h	—
205h	—	215h	—	225h	—	235h	—	245h	—
206h	RFCTRL6	216h	—	226h	—	236h	—	246h	—
207h	RFCTRL7	217h	—	227h	—	237h	—	247h	—
208h	RFCTRL8	218h	—	228h	—	238h	—	248h	—
209h	—	219h	—	229h	—	239h	—	249h	—
20Ah	—	21Ah	—	22Ah	—	23Ah	—	24Ah	—
20Bh	—	21Bh	—	22Bh	—	23Bh	—	24Bh	—
20Ch	—	21Ch	—	22Ch	—	23Ch	—	24Ch	—
20Dh	—	21Dh	—	22Dh	—	23Dh	—		
20Eh	—	21Eh	—	22Eh	—	23Eh	—		
20Fh	—	21Fh	—	22Fh	—	23Fh	—		