74LVC14A

Hex inverting Schmitt trigger with 5 V tolerant input

Product data sheet

1. General description

The 74LVC14A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as a translator in a mixed 3.3 V and 5 V environment.

The 74LVC14A provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

2. Features

- Wide supply voltage range from 1.2 V to 3.6 V
- 5 V tolerant input for interfacing with 5 V logic
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Unlimited input rise and fall times
- Complies with JEDEC standard:
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

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4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay nA to nY	V_{CC} = 3.3 V; C_L = 50 pF		-	3.2	-	ns
C_I	input capacitance			-	4.0	-	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V	[1] [2]	-	10	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC14AD	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC14ADB	–40 °C to +125 °C	SSOP14	plastic thin shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC14APW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC14ABQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

8. Functional description

8.1 Function table

Table 4: Function table [1]

Input	Output
nA	**nY**
L	H
H	L

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+6.5	V
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_{IK}	input diode current	V_I < 0 V		-	–50	mA
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 3.6 V in normal operation.

[3] For SO14 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C

11. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.2	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V to 2.7 V	V_{CC} – 0.5	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.5	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.6	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 0.8	-	-	V
V_{OL}	LOW-level voltage output	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.2	V
		I_O = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	-	0.6	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0 A	-	5	500	µA
C_I	input capacitance		-	4.0	-	pF
T_{amb} = –40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.3	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V to 2.7 V	V_{CC} – 0.65	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.65	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.75	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 1	-	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level voltage output	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.3	V
		I_O = 8 mA; V_{CC} = 2.3 V to 2.7 V	-	-	0.75	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	-	±20	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	40	µA
ΔI_{CC}	additional quiescent supply current per input pin	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	-	5	mA

[1] All typical values are measured at T_{amb} = 25 °C.

12. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 6					
		V_{CC} = 1.2 V		-	16	-	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	4.0	7.8	ns
		V_{CC} = 2.7 V		1.5	3.6	7.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	3.2	6.4	ns
$t_{sk(0)}$	skew		[2]	-	-	1.0	ns
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V	[3] [4]	-	10	-	pF
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay nA to nY	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	-	10.0	ns
		V_{CC} = 2.7 V		1.5	-	9.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	8.0	ns
$t_{sk(0)}$	skew		[2]	-	-	1.5	ns

[1] All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[4] The condition is V_I = GND to V_{CC}.

14. Transfer characteristics

Table 11: Transfer characteristics

The V_{IH} and V_{IL} from the family static characteristics are superseded by the V_{T+} and V_{T-}. Voltages are referenced to GND (ground = 0 V); see Figure 8.

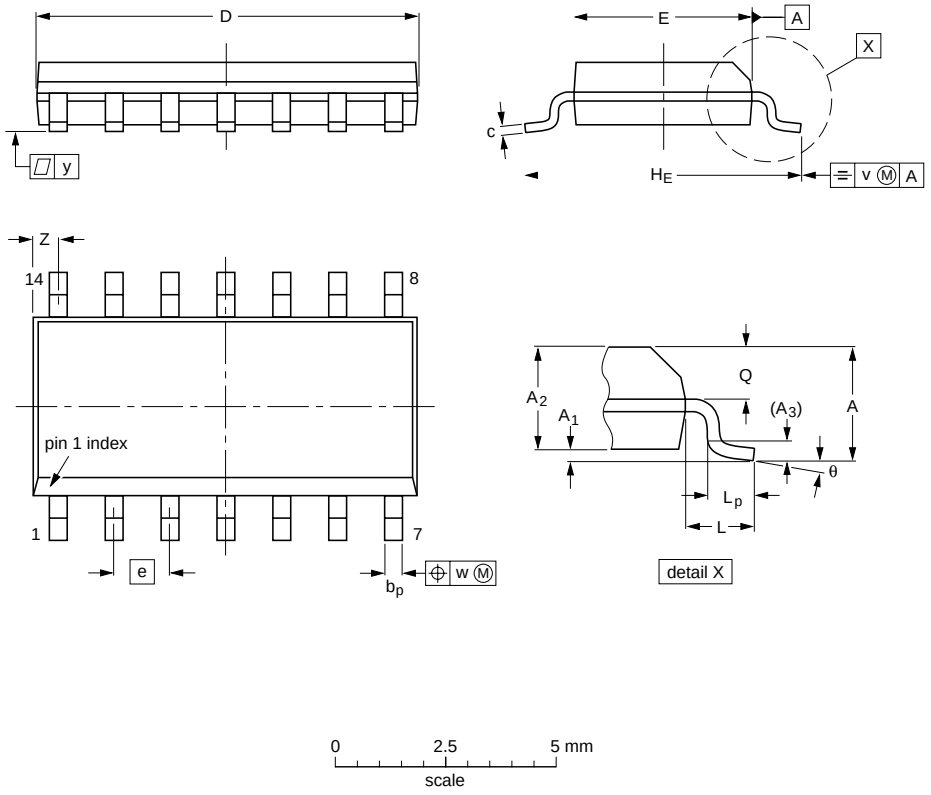
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
V_{T+}	positive-going threshold	V_{CC} = 1.2 V		-	-	1.2	V
		V_{CC} = 2.5 V		0.9	-	1.7	V
		V_{CC} = 2.7 V		1.1	-	2.0	V
		V_{CC} = 2.7 V to 3.6 V		1.1	-	2.0	V
V_{T-}	negative-going threshold	V_{CC} = 1.2 V		0	-	-	V
		V_{CC} = 2.5 V		0.4	-	1.2	V
		V_{CC} = 2.7 V		0.8	-	1.5	V
		V_{CC} = 2.7 V to 3.6 V		0.8	-	1.5	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 1.2 V		-	-	-	V
		V_{CC} = 2.5 V		0.3	-	-	V
		V_{CC} = 2.7 V		0.3	0.4	-	V
		V_{CC} = 2.7 V to 3.6 V	[2]	0.3	0.45	-	V
T_{amb} = −40 °C to +125 °C							
V_{T+}	positive-going threshold	V_{CC} = 1.2 V		-	-	1.2	V
		V_{CC} = 2.5 V		0.9	-	1.7	V
		V_{CC} = 2.7 V		1.1	-	2.0	V
		V_{CC} = 2.7 V to 3.6 V		1.1	-	2.0	V
V_{T-}	negative-going threshold	V_{CC} = 1.2 V		0	-	-	V
		V_{CC} = 2.5 V		0.4	-	1.2	V
		V_{CC} = 2.7 V		0.8	-	1.5	V
		V_{CC} = 2.7 V to 3.6 V		0.8	-	1.5	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 1.2 V		-	-	-	V
		V_{CC} = 2.5 V		0.2	-	-	V
		V_{CC} = 2.7 V		0.3	-	-	V
		V_{CC} = 2.7 V to 3.6 V		0.3	-	-	V

[1] All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] Typical transfer characteristic is displayed in Figure 9.

17. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

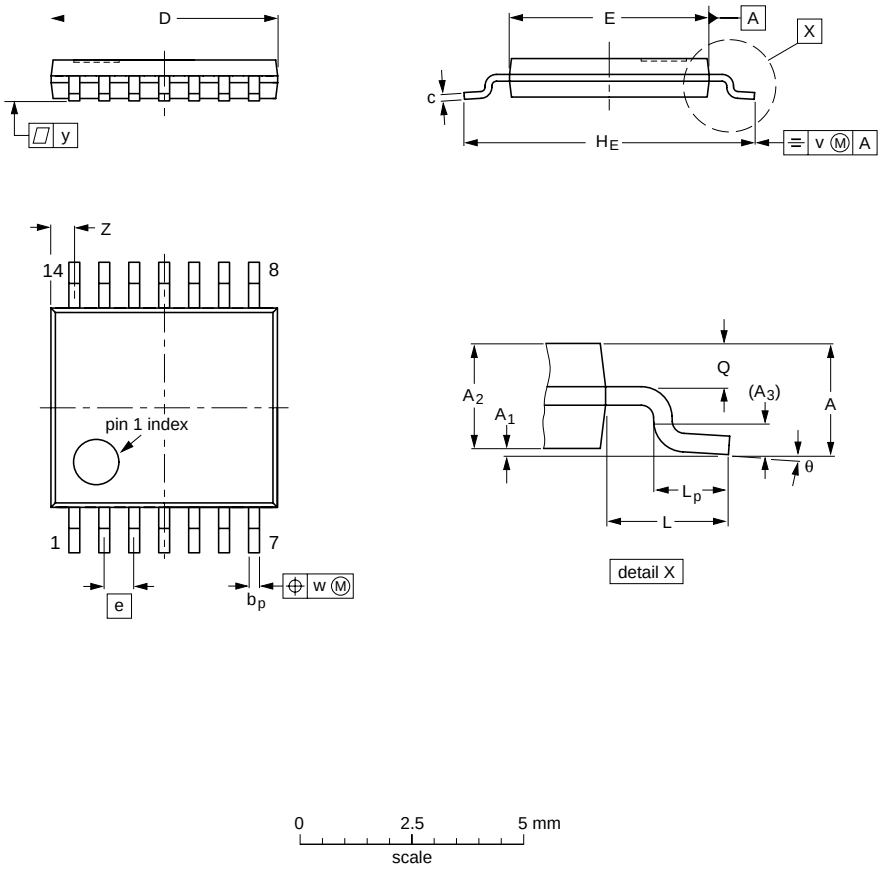
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				

Fig 12. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				

Fig 14. Package outline SOT402-1 (TSSOP14)