74HC393; 74HCT393

Dual 4-bit binary ripple counter

Product data sheet

1. General description

The 74HC393; HCT393 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC393; 74HCT393 contains 4-bit binary ripple counters with separate clocks (1$\overline{CP}$ and 2 $\overline{CP}$) and master reset (1MR and 2MR) inputs to each counter.

The operation of each half of the 74HC393; 74HCT393 is the same as the 74HC93; 74HCT93, except no external clock connections are required.

The counters are triggered by a HIGH-to-LOW transition of the clock inputs.
The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets (1MR and 2MR) are active-HIGH asynchronous inputs to each 4-bit counter. A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

2. Features

- Two 4-bit binary counters with individual clocks
- Divide by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC393						
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V				
	n$\overline{CP}$ to nQ0		-	12	-	ns
	nQx to nQ(x+1)		-	5	-	ns
	nMR to nQx		-	11	-	ns
$f_{clk(max)}$	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	99	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance (per gate)	[1] [2]	-	23	-	pF

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HCT393						
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V				
	$n\overline{CP}$ to nQ0		-	20	-	ns
	nQx to nQ(x+1)		-	6	-	ns
	nMR to nQx		-	15	-	ns
$f_{clk(max)}$	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	53	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance (per gate)	[1] [3]	-	25	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] V_I = GND to V_{CC}

[3] V_I = GND to V_{CC} – 1.5 V

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC393N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HC393D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC393DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC393PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC393BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT393N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT393D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT393DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT393PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT393BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	quiescent supply current			-	±50	mA
I_{GND}	ground current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation					
	DIP14 package		[1]	-	750	mW
	SO14 package		[2]	-	500	mW
	(T)SSOP14 package		[3]	-	500	mW
	DHVQFN14 package		[4]	-	500	mW

[1] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC393						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 2.0$ V	-	-	1000	ns
		$V_{CC} = 4.5$ V	-	6.0	500	ns
		$V_{CC} = 6.0$ V	-	-	400	ns
74HCT393						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 4.5$ V	-	6.0	500	ns

Table 7: Static characteristics type 74HC393 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = –4 mA	3.98	-	-	V
		V_{CC} = 6 V; I_O = –5.2 mA	5.48	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = 4 mA	-	-	0.33	V
		V_{CC} = 6 V; I_O = 5.2 mA	-	-	0.33	V
I_{LI}	input leakage current	V_{CC} = 6 V	-	-	0.1	µA
I_{CC}	quiescent supply current	V_{CC} = 6.0 V; I_O = 0 A; V_I = V_{CC} or GND	-	-	160	µA

Table 8: Static characteristics type 74HCT393

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	4.5	-	V
		I_O = –6 mA	3.98	4.32	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	0	0.1	V
		I_O = 6.0 mA	-	0.15	0.26	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current (per input pin)	V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	$1\overline{CP}$, $2\overline{CP}$		-	40	144	µA
	1MR, 2MR		-	100	360	µA
C_i	input capacitance		-	3.5	-	pF

Table 8: Static characteristics type 74HCT393 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −6 mA	3.84	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	μA
ΔI_{CC}	additional quiescent supply current (per input pin)	V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	$1\overline{CP}$, $2\overline{CP}$		-	-	180	μA
	1MR, 2MR		-	-	450	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = −20 μA	4.4	-	-	V
		I_O = −6 mA	3.7	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 μA	-	-	0.1	V
		I_O = 6.0 mA	-	-	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current (per input pin)	V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A				
	$1\overline{CP}$, $2\overline{CP}$		-	-	196	μA
	1MR, 2MR		-	-	490	μA

Table 9: Dynamic characteristics type 74HC393 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 2.0 V	4	-	-	MHz
		V_{CC} = 4.5 V	20	-	-	MHz
		V_{CC} = 6.0 V	24	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] V_I = GND to V_{CC}

Table 10: Dynamic characteristics type 74HCT393

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = +25 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 4.5 V	-	15	25	ns
		V_{CC} = 5 V; C_L = 15 pF	-	20	-	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 4.5 V	-	6	10	ns
		V_{CC} = 5 V; C_L = 15 pF	-	6	-	ns
t_{PHL}	propagation delay					
	nMR to nQn	see Figure 9				
		V_{CC} = 4.5 V	-	18	32	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 4.5 V	-	7	15	ns
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 4.5 V	19	11	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 4.5 V	16	6	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9				
		V_{CC} = 4.5 V	5	0	-	ns

Table 10: Dynamic characteristics type 74HCT393 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 4.5 V	27	48	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	53	-	MHz
C_{PD}	power dissipation capacitance (per gate)	[1] [2]	-	25	-	pF
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 4.5 V	-	-	31	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 4.5 V	-	-	13	ns
t_{PHL}	propagation delay					
	nMR to nQx	see Figure 9				
		V_{CC} = 4.5 V	-	-	40	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 4.5 V	-	-	19	ns
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 4.5 V	24	-	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 4.5 V	20	-	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9	5	-	-	ns
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 4.5 V	22	-	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	$n\overline{CP}$ to nQ0	see Figure 8				
		V_{CC} = 4.5 V	-	-	38	ns
	nQx to nQ(x+1)	see Figure 8				
		V_{CC} = 4.5 V	-	-	15	ns
t_{PHL}	propagation delay					
	nMR to nQx	see Figure 9				
		V_{CC} = 4.5 V	-	-	48	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 4.5 V	-	-	22	ns

Table 10: Dynamic characteristics type 74HCT393 *…continued*

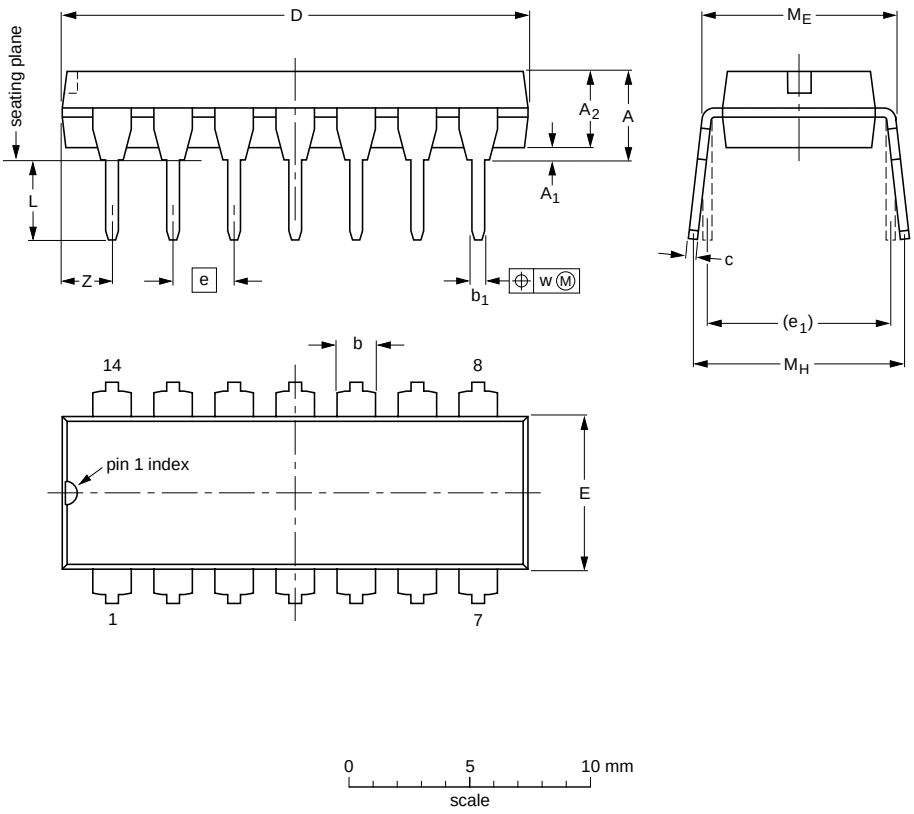
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF, unless otherwise specified. For test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width					
	$n\overline{CP}$ HIGH or LOW	see Figure 8				
		V_{CC} = 4.5 V	29	-	-	ns
	nMR HIGH	see Figure 9				
		V_{CC} = 4.5 V	24	-	-	ns
t_{rec}	recovery time					
	nMR to $n\overline{CP}$	see Figure 9	5	0	-	ns
$f_{clk(max)}$	maximum clock frequency	see Figure 8				
		V_{CC} = 4.5 V	18	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] V_I = GND to V_{CC} − 1.5 V.

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			

Fig 12. Package outline SOT27-1 (DIP14)