

## Single-Ended, Rail-to-Rail I/O, Low Gain PGA

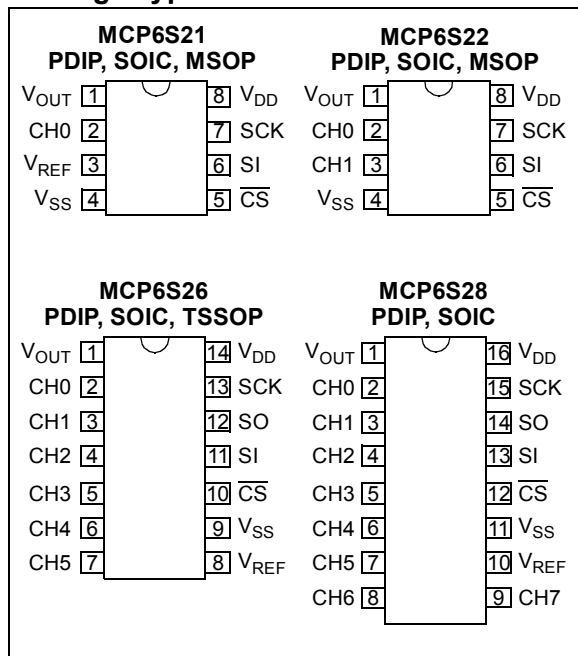
### Features

- Multiplexed Inputs: 1, 2, 6 or 8 channels
- 8 Gain Selections:
  - +1, +2, +4, +5, +8, +10, +16 or +32 V/V
- Serial Peripheral Interface (SPI™)
- Rail-to-Rail Input and Output
- Low Gain Error:  $\pm 1\%$  (max)
- Low Offset:  $\pm 275 \mu\text{V}$  (max)
- High Bandwidth: 2 to 12 MHz (typ)
- Low Noise: 10 nV/√Hz @ 10 kHz (typ)
- Low Supply Current: 1.0 mA (typ)
- Single Supply: 2.5V to 5.5V

### Typical Applications

- A/D Converter Driver
- Multiplexed Analog Applications
- Data Acquisition
- Industrial Instrumentation
- Test Equipment
- Medical Instrumentation

### Package Types

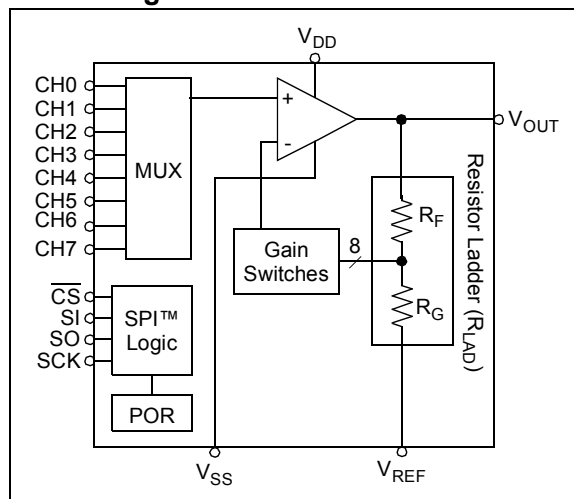


### Description

The Microchip Technology Inc. MCP6S21/2/6/8 are analog Programmable Gain Amplifiers (PGA). They can be configured for gains from +1 V/V to +32 V/V and the input multiplexer can select one of up to eight channels through an SPI port. The serial interface can also put the PGA into shutdown to conserve power. These PGAs are optimized for high speed, low offset voltage and single-supply operation with rail-to-rail input and output capability. These specifications support single supply applications needing flexible performance or multiple inputs.

The one channel MCP6S21 and the two channel MCP6S22 are available in 8-pin PDIP, SOIC and MSOP packages. The six channel MCP6S26 is available in 14-pin PDIP, SOIC and TSSOP packages. The eight channel MCP6S28 is available in 16-pin PDIP and SOIC packages. All parts are fully specified from -40°C to +85°C.

### Block Diagram



# MCP6S21/2/6/8

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
All inputs and outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input voltage .....	$ V_{DD} - V_{SS} $
Output Short Circuit Current.....	continuous
Current at Input Pin .....	$\pm 2$ mA
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage temperature .....	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Junction temperature .....	$+150^{\circ}\text{C}$
ESD protection on all pins (HBM;MM).....	$\geq 2$ kV; 200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $T_A = +25^{\circ}\text{C}$ ,  $V_{DD} = +2.5V$  to  $+5.5V$ ,  $V_{SS} = \text{GND}$ ,  $V_{REF} = V_{SS}$ ,  $G = +1$  V/V, Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V,  $R_L = 10$  k $\Omega$  to  $V_{DD}/2$ , SI and SCK are tied low and  $\overline{\text{CS}}$  is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions	
<b>Amplifier Input</b>							
Input Offset Voltage	$V_{OS}$	-275	—	+275	$\mu\text{V}$	$G = +1$ , $V_{DD} = 4.0V$	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T_A$	—	$\pm 4$	—	$\mu\text{V}/^{\circ}\text{C}$	$T_A = -40$ to $+85^{\circ}\text{C}$	
Power Supply Rejection Ratio	PSRR	70	85	—	dB	$G = +1$ ( <b>Note 1</b> )	
Input Bias Current	$I_B$	—	$\pm 1$	—	pA	$\text{CHx} = V_{DD}/2$	
Input Bias Current over Temperature	$I_B$	—	—	250	pA	$T_A = -40$ to $+85^{\circ}\text{C}$ , $\text{CHx} = V_{DD}/2$	
Input Impedance	$Z_{IN}$	—	$10^{13}  15$	—	$\Omega  \text{pF}$		
Input Voltage Range	$V_{IVR}$	$V_{SS}-0.3$	—	$V_{DD}+0.3$	V		
<b>Amplifier Gain</b>							
Nominal Gains	G	—	1 to 32	—	V/V	+1, +2, +4, +5, +8, +10, +16 or +32	
DC Gain Error	$G = +1$	$g_E$	-0.1	—	+0.1	%	$V_{OUT} \approx 0.3V$ to $V_{DD} - 0.3V$
	$G \geq +2$	$g_E$	-1.0	—	+1.0	%	$V_{OUT} \approx 0.3V$ to $V_{DD} - 0.3V$
DC Gain Drift	$G = +1$	$\Delta G/\Delta T_A$	—	$\pm 0.0002$	—	$\%/^{\circ}\text{C}$	$T_A = -40$ to $+85^{\circ}\text{C}$
	$G \geq +2$	$\Delta G/\Delta T_A$	—	$\pm 0.0004$	—	$\%/^{\circ}\text{C}$	$T_A = -40$ to $+85^{\circ}\text{C}$
Internal Resistance	$R_{LAD}$	3.4	4.9	6.4	k $\Omega$	( <b>Note 1</b> )	
Internal Resistance over Temperature	$\Delta R_{LAD}/\Delta T_A$	—	+0.028	—	$\%/^{\circ}\text{C}$	( <b>Note 1</b> ) $T_A = -40$ to $+85^{\circ}\text{C}$	
<b>Amplifier Output</b>							
DC Output Non-linearity	$G = +1$	$V_{ONL}$	—	$\pm 0.003$	—	% of FSR	$V_{OUT} = 0.3V$ to $V_{DD} - 0.3V$ , $V_{DD} = 5.0V$
	$G \geq +2$	$V_{ONL}$	—	$\pm 0.001$	—	% of FSR	$V_{OUT} = 0.3V$ to $V_{DD} - 0.3V$ , $V_{DD} = 5.0V$
Maximum Output Voltage Swing	$V_{OH}, V_{OL}$	$V_{SS}+20$	—	$V_{DD}-100$	mV		$G \geq +2$ ; 0.5V output overdrive
		$V_{SS}+60$	—	$V_{DD}-60$			$G \geq +2$ ; 0.5V output overdrive, $V_{REF} = V_{DD}/2$
Short-Circuit Current	$I_{O(SC)}$	—	$\pm 30$	—	mA		

**Note 1:**  $R_{LAD}$  ( $R_F + R_G$  in Figure 4-1) connects  $V_{REF}$ ,  $V_{OUT}$  and the inverting input of the internal amplifier. The MCP6S22 has  $V_{REF}$  tied internally to  $V_{SS}$ , so  $V_{SS}$  is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. We recommend the MCP6S22's  $V_{SS}$  pin be tied directly to ground to avoid noise problems.

**2:**  $I_Q$  includes current in  $R_{LAD}$  (typically 60  $\mu\text{A}$  at  $V_{OUT} = 0.3V$ ). Both  $I_Q$  and  $I_{Q\_SHDN}$  exclude digital switching currents.

**3:** The output goes Hi-Z and the registers reset to their defaults; see Section 5.4, "Power-On Reset".

### PIN FUNCTION TABLE

Name	Function
$V_{OUT}$	Analog Output
CH0-CH7	Analog Inputs
$V_{SS}$	Negative Power Supply
$V_{DD}$	Positive Power Supply
SCK	SPI Clock Input
SI	SPI Serial Data Input
SO	SPI Serial Data Output
$\overline{\text{CS}}$	SPI Chip Select
$V_{REF}$	External Reference Pin

## DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.5\text{V to } +5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{REF} = V_{SS}$ ,  $G = +1\text{ V/V}$ , Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ , SI and SCK are tied low and CS is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	2.5	—	5.5	V	
Quiescent Current	$I_Q$	0.5	1.0	1.35	mA	$I_O = 0$ (Note 2)
Quiescent Current, Shutdown mode	$I_{Q\_SHDN}$	—	0.5	1.0	$\mu\text{A}$	$I_O = 0$ (Note 2)
<b>Power-On Reset</b>						
POR Trip Voltage	$V_{POR}$	1.2	1.7	2.2	V	(Note 3)
POR Trip Voltage Drift	$\Delta V_{POR}/\Delta T$	—	-3.0	—	$\text{mV}/^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$

- Note 1:**  $R_{LAD}$  ( $R_F + R_G$  in Figure 4-1) connects  $V_{REF}$ ,  $V_{OUT}$  and the inverting input of the internal amplifier. The MCP6S22 has  $V_{REF}$  tied internally to  $V_{SS}$ , so  $V_{SS}$  is coupled to the internal amplifier and the PSRR spec describes PSRR+ only. We recommend the MCP6S22's  $V_{SS}$  pin be tied directly to ground to avoid noise problems.
- Note 2:**  $I_Q$  includes current in  $R_{LAD}$  (typically 60  $\mu\text{A}$  at  $V_{OUT} = 0.3\text{V}$ ). Both  $I_Q$  and  $I_{Q\_SHDN}$  exclude digital switching currents.
- Note 3:** The output goes Hi-Z and the registers reset to their defaults; see Section 5.4, "Power-On Reset".

## AC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.5\text{V to } +5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{REF} = V_{SS}$ ,  $G = +1\text{ V/V}$ , Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , SI and SCK are tied low, and CS is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Frequency Response</b>						
-3 dB Bandwidth	BW	—	2 to 12	—	MHz	All gains; $V_{OUT} < 100\text{ mV}_{P-P}$ (Note 1)
Gain Peaking	GPK	—	0	—	dB	All gains; $V_{OUT} < 100\text{ mV}_{P-P}$
<b>Total Harmonic Distortion plus Noise</b>						
$f = 1\text{ kHz}$ , $G = +1\text{ V/V}$	THD+N	—	0.0015	—	%	$V_{OUT} = 1.5\text{V} \pm 1.0\text{V}_{P-K}$ , $V_{DD} = 5.0\text{V}$ , BW = 22 kHz
$f = 1\text{ kHz}$ , $G = +4\text{ V/V}$	THD+N	—	0.0058	—	%	$V_{OUT} = 1.5\text{V} \pm 1.0\text{V}_{P-K}$ , $V_{DD} = 5.0\text{V}$ , BW = 22 kHz
$f = 1\text{ kHz}$ , $G = +16\text{ V/V}$	THD+N	—	0.023	—	%	$V_{OUT} = 1.5\text{V} \pm 1.0\text{V}_{P-K}$ , $V_{DD} = 5.0\text{V}$ , BW = 22 kHz
$f = 20\text{ kHz}$ , $G = +1\text{ V/V}$	THD+N	—	0.0035	—	%	$V_{OUT} = 1.5\text{V} \pm 1.0\text{V}_{P-K}$ , $V_{DD} = 5.0\text{V}$ , BW = 80 kHz
$f = 20\text{ kHz}$ , $G = +4\text{ V/V}$	THD+N	—	0.0093	—	%	$V_{OUT} = 1.5\text{V} \pm 1.0\text{V}_{P-K}$ , $V_{DD} = 5.0\text{V}$ , BW = 80 kHz
$f = 20\text{ kHz}$ , $G = +16\text{ V/V}$	THD+N	—	0.036	—	%	$V_{OUT} = 1.5\text{V} \pm 1.0\text{V}_{P-K}$ , $V_{DD} = 5.0\text{V}$ , BW = 80 kHz
<b>Step Response</b>						
Slew Rate	SR	—	4.0	—	$\text{V}/\mu\text{s}$	$G = 1, 2$
		—	11	—	$\text{V}/\mu\text{s}$	$G = 4, 5, 8, 10$
		—	22	—	$\text{V}/\mu\text{s}$	$G = 16, 32$
<b>Noise</b>						
Input Noise Voltage	$E_{ni}$	—	3.2	—	$\mu\text{V}_{P-P}$	$f = 0.1\text{ Hz to } 10\text{ kHz}$ (Note 2)
		—	26	—		$f = 0.1\text{ Hz to } 200\text{ kHz}$ (Note 2)
Input Noise Voltage Density	$e_{ni}$	—	10	—	$\text{nV}/\sqrt{\text{Hz}}$	$f = 10\text{ kHz}$ (Note 2)
Input Noise Current Density	$i_{ni}$	—	4	—	$\text{fA}/\sqrt{\text{Hz}}$	$f = 10\text{ kHz}$

- Note 1:** See Table 4-1 for a list of typical numbers.
- Note 2:**  $E_{ni}$  and  $e_{ni}$  include ladder resistance noise. See Figure 2-33 for  $e_{ni}$  vs. G data.

# MCP6S21/2/6/8

## DIGITAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +2.5\text{V}$  to  $+5.5\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{REF} = V_{SS}$ ,  $G = +1\text{V/V}$ , Input = CH0 = (0.3V)/G, CH1 to CH7 = 0.3V,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}/2$ ,  $C_L = 60\text{ pF}$ , SI and SCK are tied low, and  $\overline{\text{CS}}$  is tied high.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>SPI Inputs (<math>\overline{\text{CS}}</math>, SI, SCK)</b>						
Logic Threshold, Low	$V_{IL}$	0	—	$0.3V_{DD}$	V	
Input Leakage Current	$I_{IL}$	-1.0	—	+1.0	$\mu\text{A}$	
Logic Threshold, High	$V_{IH}$	$0.7V_{DD}$	—	$V_{DD}$	V	
Amplifier Output Leakage Current	—	-1.0	—	+1.0	$\mu\text{A}$	In Shutdown mode
<b>SPI Output (SO, for MCP6S26 and MCP6S28)</b>						
Logic Threshold, Low	$V_{OL}$	$V_{SS}$	—	$V_{SS}+0.4$	V	$I_{OL} = 2.1\text{ mA}$ , $V_{DD} = 5\text{V}$
Logic Threshold, High	$V_{OH}$	$V_{DD}-0.5$	—	$V_{DD}$	V	$I_{OH} = -400\text{ }\mu\text{A}$
<b>SPI Timing</b>						
Pin Capacitance	$C_{PIN}$	—	10	—	pF	All digital I/O pins
Input Rise/Fall Times ( $\overline{\text{CS}}$ , SI, SCK)	$t_{RFI}$	—	—	2	$\mu\text{s}$	<b>Note 1</b>
Output Rise/Fall Times (SO)	$t_{RFO}$	—	5	—	ns	MCP6S26 and MCP6S28
$\overline{\text{CS}}$ high time	$t_{CSH}$	40	—	—	ns	
SCK edge to $\overline{\text{CS}}$ fall setup time	$t_{CS0}$	10	—	—	ns	SCK edge when $\overline{\text{CS}}$ is high
$\overline{\text{CS}}$ fall to first SCK edge setup time	$t_{CSSC}$	40	—	—	ns	
SCK Frequency	$f_{SCK}$	—	—	10	MHz	$V_{DD} = 5\text{V}$ ( <b>Note 2</b> )
SCK high time	$t_{HI}$	40	—	—	ns	
SCK low time	$t_{LO}$	40	—	—	ns	
SCK last edge to $\overline{\text{CS}}$ rise setup time	$t_{SCCS}$	30	—	—	ns	
$\overline{\text{CS}}$ rise to SCK edge setup time	$t_{CS1}$	100	—	—	ns	SCK edge when $\overline{\text{CS}}$ is high
SI set-up time	$t_{SU}$	40	—	—	ns	
SI hold time	$t_{HD}$	10	—	—	ns	
SCK to SO valid propagation delay	$t_{DO}$	—	—	80	ns	MCP6S26 and MCP6S28
$\overline{\text{CS}}$ rise to SO forced to zero	$t_{SOZ}$	—	—	80	ns	MCP6S26 and MCP6S28
<b>Channel and Gain Select Timing</b>						
Channel Select Time	$t_{CH}$	—	1.5	—	$\mu\text{s}$	CHx = 0.6V, CHy = 0.3V, G = 1, CHx to CHy select $\overline{\text{CS}} = 0.7V_{DD}$ to $V_{OUT}$ 90% point
Gain Select Time	$t_G$	—	1	—	$\mu\text{s}$	CHx = 0.3V, G = 5 to G = 1 select, $\overline{\text{CS}} = 0.7V_{DD}$ to $V_{OUT}$ 90% point
<b>Shutdown Mode Timing</b>						
Out of Shutdown mode ( $\overline{\text{CS}}$ goes high) to Amplifier Output Turn-on Time	$t_{ON}$	—	3.5	10	$\mu\text{s}$	$\overline{\text{CS}} = 0.7V_{DD}$ to $V_{OUT}$ 90% point
Into Shutdown mode ( $\overline{\text{CS}}$ goes high) to Amplifier Output High-Z Turn-off Time	$t_{OFF}$	—	1.5	—	$\mu\text{s}$	$\overline{\text{CS}} = 0.7V_{DD}$ to $V_{OUT}$ 90% point
<b>POR Timing</b>						
Power-On Reset power-up time	$t_{RPU}$	—	30	—	$\mu\text{s}$	$V_{DD} = V_{POR} - 0.1\text{V}$ to $V_{POR} + 0.1\text{V}$ , 50% $V_{DD}$ to 90% $V_{OUT}$ point
Power-On Reset power-down time	$t_{RPD}$	—	10	—	$\mu\text{s}$	$V_{DD} = V_{POR} + 0.1\text{V}$ to $V_{POR} - 0.1\text{V}$ , 50% $V_{DD}$ to 90% $V_{OUT}$ point

**Note 1:** Not tested in production. Set by design and characterization.

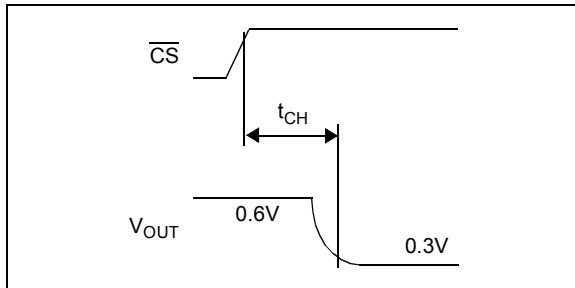
**Note 2:** When using the device in the daisy chain configuration, maximum clock frequency is determined by a combination of propagation delay time ( $t_{DO} \leq 80\text{ ns}$ ), data input setup time ( $t_{SU} \geq 40\text{ ns}$ ), SCK high time ( $t_{HI} \geq 40\text{ ns}$ ), and SCK rise and fall times of 5 ns. Maximum  $f_{SCK}$  is, therefore,  $\approx 5.8\text{ MHz}$ .

## TEMPERATURE CHARACTERISTICS

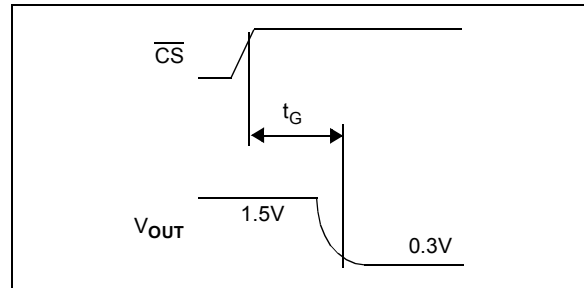
**Electrical Specifications:** Unless otherwise indicated,  $V_{DD} = +2.5V$  to  $+5.5V$ ,  $V_{SS} = GND$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+85	°C	
Operating Temperature Range	$T_A$	-40	—	+125	°C	(Note Note:)
Storage Temperature Range	$T_A$	-65	—	+150	°C	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 8L-PDIP	$\theta_{JA}$	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	$\theta_{JA}$	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	°C/W	
Thermal Resistance, 16L-PDIP	$\theta_{JA}$	—	70	—	°C/W	
Thermal Resistance, 16L-SOIC	$\theta_{JA}$	—	90	—	°C/W	

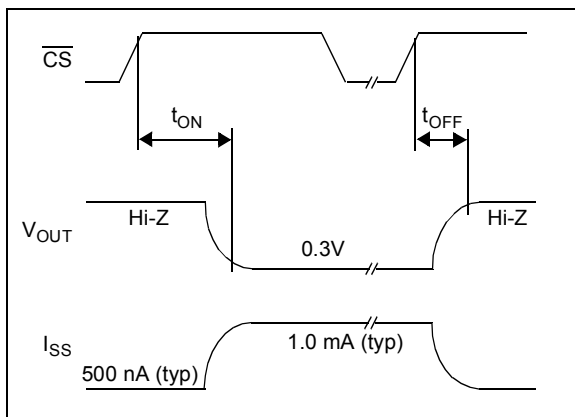
**Note 1:** The MCP6S21/2/6/8 family of PGAs operates over this extended temperature range, but with reduced performance. Operation in this range must not cause  $T_J$  to exceed the Maximum Junction Temperature (150°C).



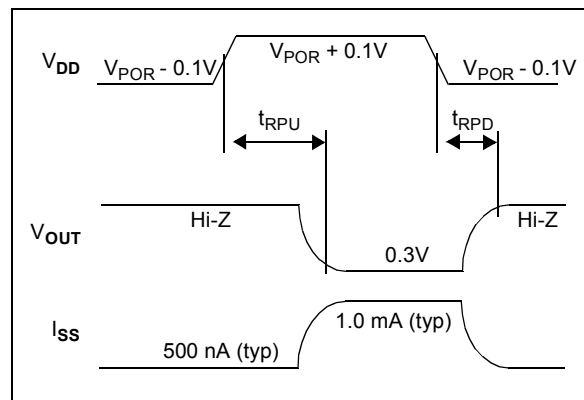
**FIGURE 1-1:** Channel Select Timing Diagram.



**FIGURE 1-3:** Gain Select Timing Diagram.

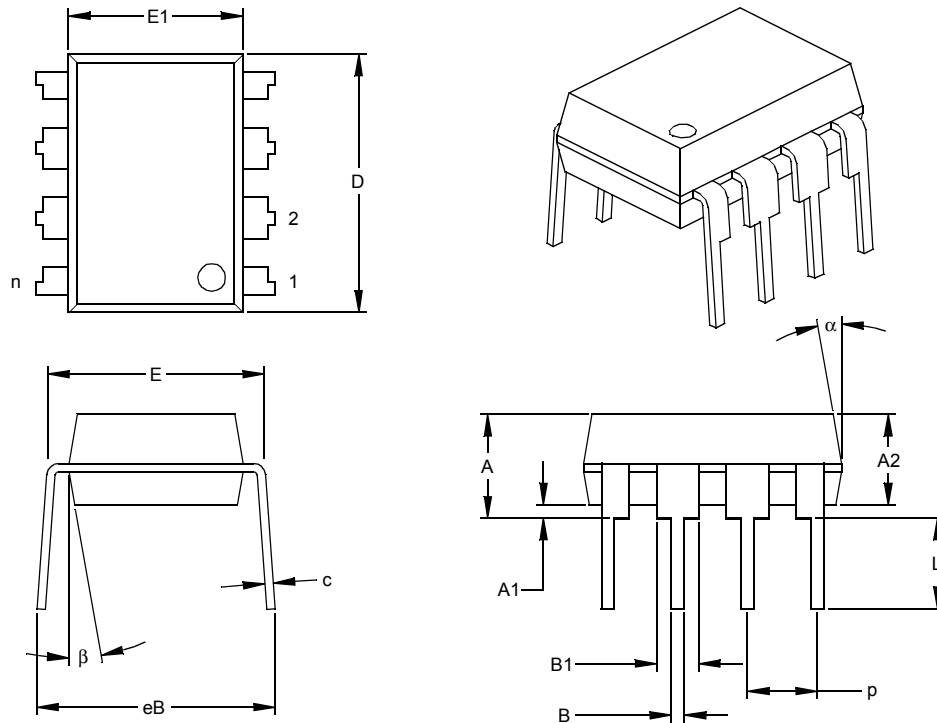


**FIGURE 1-2:** PGA Shutdown timing diagram (must enter correct commands before CS goes high).



**FIGURE 1-4:** POR power-up and power-down timing diagram.

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter  
 § Significant Characteristic

Notes:  
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.  
 JEDEC Equivalent: MS-001  
 Drawing No. C04-018

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-X</u>	<u>/XX</u>	
Device	Temperature Range	Package	
Device:	MCP6S21:	One Channel PGA	
	MCP6S21T:	One Channel PGA (Tape and Reel for SOIC and MSOP)	
	MCP6S22:	Two Channel PGA	
	MCP6S22T:	Two Channel PGA (Tape and Reel for SOIC and MSOP)	
	MCP6S26:	Six Channel PGA	
	MCP6S26T:	Six Channel PGA (Tape and Reel for SOIC and TSSOP)	
	MCP6S28:	Eight Channel PGA	
	MCP6S28T:	Eight Channel PGA (Tape and Reel for SOIC)	
Temperature Range:	I	= -40°C to +85°C	
Package:	MS	= Plastic Micro Small Outline (MSOP), 8-lead	
	P	= Plastic DIP (300 mil Body), 8, 14, and 16-lead	
	SN	= Plastic SOIC, (150 mil Body), 8-lead	
	SL	= Plastic SOIC (150 mil Body), 14, 16-lead	
	ST	= Plastic TSSOP (4.4mm Body), 14-lead	

**Examples:**

- a) MCP6S21-I/P: One Channel PGA, PDIP package.
- b) MCP6S21-I/SN: One Channel PGA, SOIC package.
- c) MCP6S21-I/MS: One Channel PGA, MSOP package.
- d) MCP6S22-I/MS: Two Channel PGA, MSOP package.
- e) MCP6S22T-I/MS: Two Channel PGA, MSOP package.
- f) MCP6S26-I/P: Six Channel PGA, PDIP package.
- g) MCP6S26-I/SN: Six Channel PGA, SOIC package.
- h) MCP6S26T-I/ST: Tape and Reel, Six Channel PGA, TSSOP package.
- i) MCP6S28T-I/SL: Tape and Reel, Eight Channel PGA, SOIC package.