DS2430A
256-Bit 1-Wire EEPROM

FEATURES

- 256-bit Electrically Erasable Programmable Read Only Memory (EEPROM) plus 64-bit one-time programmable application register
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute identity because no two parts are alike
- Built-in multidrop controller ensures compatibility with other MicroLAN products
- EEPROM organized as one page of 32 bytes for random access
- Reduces control, address, data, and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits per second
- 8-bit family code specifies DS2430A communication requirements to reader
- Presence detector acknowledges when reader first applies voltage
- Low cost TO-92 or 6-pin TSOC and Flip Chip surface mount package
- Reads and writes over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C

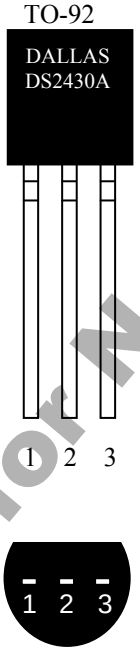
ORDERING INFORMATION

DS2430A	TO-92 Package
DS2430AP	6-pin TSOC Package
DS2430A/T&R	TO-92 Package, Tape & Reel
DS2430AP/T&R	TSOC Package, Tape & Reel
DS2430A+	TO-92 Package
DS2430AP+	6-pin TSOC Package
DS2430A+T&R	TO-92 Package, Tape & Reel
DS2430AP+T&R	TSOC Package, Tape & Reel
DS2430AX	Flip Chip, 10k Tape & Reel
DS2430AX-S	Flip Chip, 2.5k Tape & Reel

+ Indicates lead-free compliance.

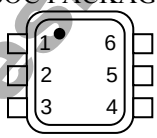
PIN ASSIGNMENT

TO-92

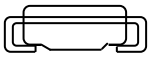


BOTTOM VIEW
See Mech.
Drawings Section

TSOC PACKAGE

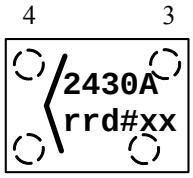


TOP VIEW
3.7mm x 4.0mm x 1.5mm



SIDE VIEW

See Mech.
Drawing Section



Flip Chip, Top View
with Laser Mark,
Contacts Not Visible.
"rrd" = Revision/Date
#xx = Lot Number
See 56-G7016-001 for
package outline.

NOTE: The leads of TO-92 packages on tape-and-reel are formed to approximately 100 mil (2.54 mm) spacing. For details refer to drawing 56-G0006-003.

PIN DESCRIPTION

	TO-92	**TSOC**	**Flip Chip**
Pin 1	Ground	Ground	Ground
Pin 2	Data	Data	Data
Pin 3	NC	NC	NC
Pin 4	——	NC	NC
Pin 5	——	NC	——
Pin 6	——	NC	——

DESCRIPTION

The DS2430A 256-bit 1-Wire EEPROM identifies and stores relevant information about the product to which it is associated. This lot or product specific information can be accessed with minimal interface, for example a single port pin of a microcontroller. The DS2430A consists of a factory-lasered registration number that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (14h) plus 256 bits of user-programmable EEPROM and a 64-bit one-time programmable application register. The power to read and write the DS2430A is derived entirely from the 1-Wire® communication line. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return. The 48-bit serial number that is factory-lasered into each DS2430A provides a guaranteed unique identity that allows for absolute traceability. The TO-92 and TSOC packages provide a compact enclosure that allows standard assembly equipment to handle the device easily for attachment to printed circuit boards or wiring. Typical applications include storage of calibration constants, board identification, and product revision status.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2430A. The DS2430A has four main data components: 1) 64-bit lasered ROM, 2) 256-bit EEPROM data memory with scratchpad, 3) 64-bit one-time programmable application register with scratchpad and 4) 8-bit status memory. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the four ROM Function Commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Skip ROM. The protocol required for these ROM Function Commands is described in Figure 8. After a ROM Function Command is successfully executed, the memory functions become accessible and the master can provide any one of the four memory function commands. The protocol for these memory function commands is described in Figure 6. All data is read and written least significant bit first.

64-BIT LASERED ROM

Each DS2430A contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code (14h). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in *Application Note 27*. The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, then the serial number is entered. After the 48^{th} bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all 0s.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP} = 2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2			V	1, 6
Logic 0	V_{IL}	-0.3		+0.8	V	1, 9
Output Logic Low @ 4mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1, 2
Input Load Current (DATA pin)	I_L	0.1	5	15	µA	3
Programming Current	I_P			500	µA	10

CAPACITANCE (t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance	C_D			800	pF	7

EEPROM (V_{PUP} = 5.0V; t_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Write/Erase Cycles	N_{CYCLE}	100k			-	
Data Retention (at 85°C)	t_{DR}	10			years	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{PUP}=2.8V to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	13
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	13
Read Data Valid	t_{RDV}		15		µs	11, 12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480		960	µs	8
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	
Programming Time	t_{PROG}			10	ms	

NOTES:

1) All voltages are referenced to ground.

2) V_{PUP} = external pullup voltage.

3) Input load is to ground.

4) An additional reset or communication sequence cannot begin until the reset high time has expired.

5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge.

6) V_{IH} is a function of the external pullup resistor and V_{PUP}.

7) Capacitance on the data pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied the parasite capacitance will not affect normal communications.

8) The Reset Low Time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling; otherwise it could mask or conceal interrupt pulses.

9) Under certain low voltage conditions V_{ILMAX} may have to be reduced to as much as 0.5V to always guarantee a Presence Pulse.

10) The Copy Scratchpad takes 10ms maximum, during which the voltage on the 1-Wire bus must not fall below 2.8V.

11) Depending on the 1-Wire communication speed and the bus load characteristics, the optimal pullup resistor value will be in the 1.5kΩ to 5kΩ range.

12) The optimal sampling point for the master is as close as possible to the end time of the 15µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.

13) The duration of the low pulse sent by the master should be a minimum of 1µs with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.