DS1217M
Nonvolatile Read/Write Cartridge

GENERAL DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 64k x 8 to 512k x 8. The cartridge is accessed in continuous 32k byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems that have JEDEC 28-pin bytewide memory sites.

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS1217M	0°C to +70°C	30 Cartridge

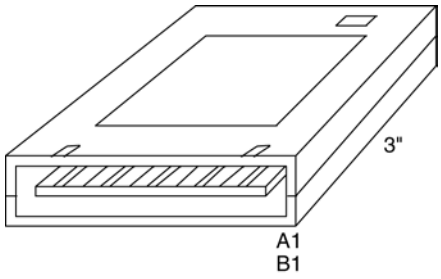
PIN CONFIGURATION

TOP VIEW

Ground	A1	B1	No Connect
+5V	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

FEATURES

- **User Insertable**
- **Data Retention Greater than 5 Years**
- **Capacity to 512k x 8**
- **Standard Bytewide Pinout Facilitates Connection to JEDEC 28-Pin DIP Through Ribbon Cable**
- **Software-Controlled Banks Maintain 32 x 8 JEDEC 28-Pin Compatibility**
- **Multiple Cartridges Can Reside on a Common Bus**
- **Automatic Write Protection Circuitry Safeguards Against Data Loss**
- **Manual Switch Unconditionally Protects Data**
- **Compact Size and Shape**
- **Rugged and Durable**
- **Operating Temperature Range: 0°C to +70°C**



Package Drawing appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Connection Relative to Ground	-0.3V to + 7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +70°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2		V_{CC}	V
Input Low Voltage	V_{IL}		0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}		-60		+60	µA
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}		-10		+10	µA
Output Current at 2.4V	I_{OH}		-1.0	-2.0		mA
Output Current at 0.4V	I_{OL}		+2.0	+3.0		mA
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}			15	25	mA
Operating Current	I_{CCO1}			50	100	mA

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}				100	pF
Input/Output Capacitance	C_{OUT}				100	pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

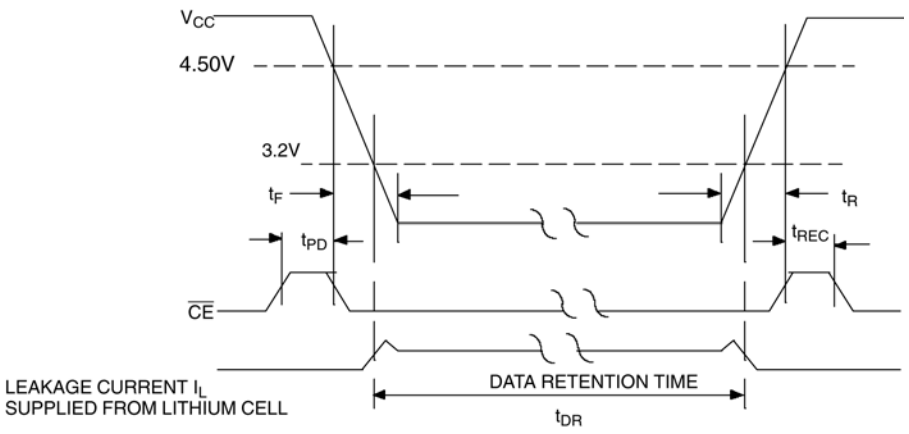
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle Time	t_{RC}		250			ns
Access Time	t_{ACC}				250	ns
$\overline{OE}$ to Output Valid	t_{OE}				125	ns
$\overline{CE}$ to Output Valid	t_{CO}				210	ns
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	(Note 1)	5			ns
Output High-Z from Deselection	t_{OD}	(Note 1)			125	ns
Output Hold from Address Change	t_{OH}		5			ns
Read Recovery Time	t_{RR}		40			ns
Write Cycle Time	t_{WC}		250			ns
Write Pulse Width	t_{WP}	(Note 2)	170			ns
Address Setup Time	t_{AW}		0			ns
Write Recovery Time	t_{WR}		20			ns
Output High-Z from $\overline{WE}$	t_{ODW}	(Note 1)			100	ns
Output Active from $\overline{WE}$	t_{OEW}	(Note 1)	5			ns
Data Setup Time	t_{DS}	(Note 3)	100			ns
Data Hold Time from $\overline{WE}$	t_{DH}	(Note 3)	20			ns

Note 1: These parameters are sampled with a 5pF load and are not 100% tested.

Note 2: t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$ t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

Note 3: t_{DH}, t_{DS} are measured form the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CE}$ at V_{IH} Before Power-Down	t_{PD}	(Note 9)	0			µs
V_{CC} Slew from 4.5V to 0 ($\overline{CE}$ at V_{IH})	t_F		100			µs
V_{CC} Slew from 0 to 4.5V ($\overline{CE}$ at V_{IH})	t_R		0			µs
$\overline{CE}$ at V_{IH} After Power-Up	t_{REC}	(Note 9)	2		125	ms

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Expected Data Retention Time	t_{DR}	(Note 10)	5			years

WARNING: Under no circumstances are negative undershoots of any amplitude allowed when the device is in battery-backup mode.

Note 4: $\overline{WE}$ is high for a read cycle.

Note 5: $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high-impedance state.

Note 6: If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ high transition in Write Cycle 1, that output buffers remain in a high-impedance state in this period.

Note 7: If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high-impedance state in this period.

Note 8: If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high-impedance state in this period.

Note 9: Removing and installing the cartridge with power applied may disturb data.

Note 10: Each DS1217M I smarked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture. This parameter is assured by component selection, process control, and design. It is not measured directly during production testing.