24LCS21A

1K 2.5V Dual Mode I²C™ Serial EEPROM

Features:

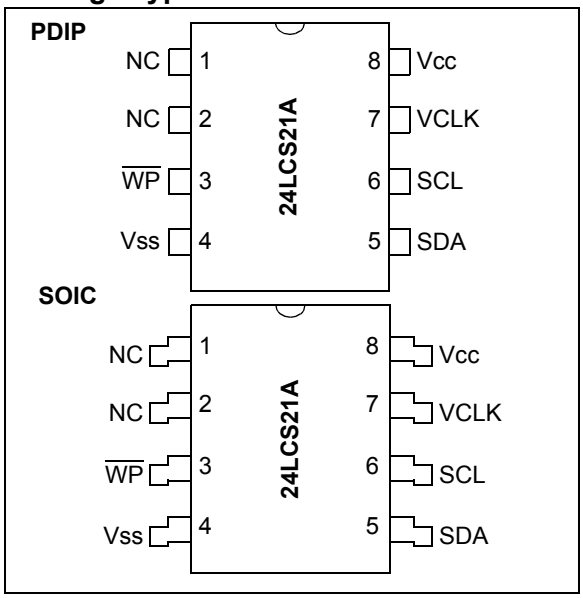
- Single Supply with Operation Down to 2.5V
- Completely Implements DDC1™/DDC2™ Interface for Monitor Identification, Including Recovery to DDC1
- Low-Power CMOS Technology:
  - 1 mA active current, typical
  - 10 μA standby current, typical at 5.5V
- 2-Wire Serial Interface Bus, I²C™ Compatible
- 100 kHz (2.5V) and 400 kHz (5V) Compatibility
- Self-Timed Write Cycle (including Auto-Erase)
- Hardware Write-Protect Pin
- Page Write Buffer for up to Eight Bytes
- 1,000,000 Erase/Write Cycles Ensured
- Data Retention > 200 years
- ESD Protection > 4000V
- 8-pin PDIP and SOIC Package
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +70°C
- Pb-Free and RoHS Compliant

Description:

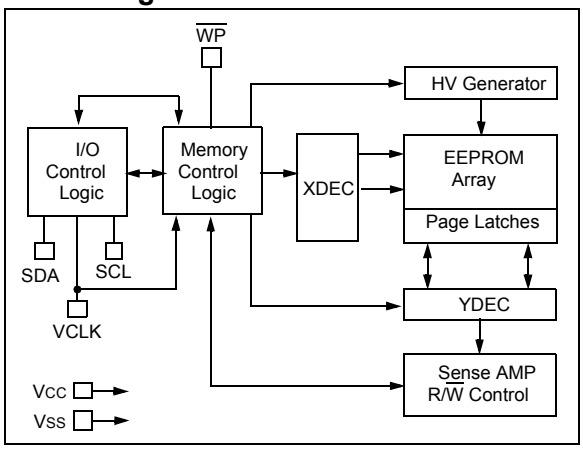
The Microchip Technology Inc. 24LCS21A is a 128 x 8-bit dual-mode Electrically Erasable PROM. This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: Transmit-Only mode and Bidirectional mode. Upon power-up, the device will be in the Transmit-Only mode, sending a serial bit stream of the memory array from 00h to 7Fh, clocked by the VCLK pin. A valid high-to-low transition on the SCL pin will cause the device to enter the Transition mode and look for a valid control byte on the I²C bus. If it detects a valid control byte from the master, it will switch into Bidirectional mode, with byte selectable read/write capability of the memory array using SCL. If no control byte is received, the device will revert to the Transmit-Only mode after it receives 128 consecutive VCLK pulses while the SCL pin is idle. The 24LCS21A also enables the user to write-protect the entire memory array using its write-protect pin. The 24LCS21A is available in a standard 8-pin PDIP and SOIC package in industrial temperature range.

DDC is a trademark of the Video Electronics Standards Assoc.
I²C is a trademark of Philips Corporation.

Package Types



Block Diagram



Pin Function Table

Name	Function
WP	Write-Protect (active low)
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock (Bidirectional mode)
VCLK	Serial Clock (Transmit-Only mode)
Vcc	+2.5V to 5.5V Power Supply
NC	No Connection

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS	VCC = +2.5V to 5.5V Industrial (I): TA = -40°C to +85°C				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
SCL and SDA pins:					
High-level input voltage	VIH	0.7 VCC	—	V	
Low-level input voltage	VIL	—	0.3 VCC	V	
Input levels on VCLK pin:					
High-level input voltage	VIH	2.0	—	V	VCC ≥ 2.7V **(Note)**
Low-level input voltage	VIL	—	0.2 VCC	V	VCC < 2.7V **(Note)**
Hysteresis of Schmitt Trigger inputs	VHYS	.05 VCC	—	V	**(Note)**
Low-level output voltage	VOL1	—	0.4	V	IOL = 3 mA, VCC = 2.5V **(Note)**
Low-level output voltage	VOL2	—	0.6	V	IOL = 6 mA, VCC = 2.5V
Input leakage current	ILI	—	±1	µA	VIN = VSS or VCC
Output leakage current	ILO	—	±1	µA	VOUT = VSS or VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V **(Note)** TA = 25°C, FCLK = 1 MHz
Operating current	ICC Write ICC Read	— —	3 1	mA mA	VCC = 5.5V VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	— —	30 100	µA µA	VCC = 3.0V, SDA = SCL = VCC VCC = 5.5V, SDA = SCL = VCC VCLK = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

Parameter	Symbol	Vcc = 2.5-4.5V Standard Mode		Vcc = 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	**(Note 1)**
SDA and SCL fall time	TF	—	300	—	300	ns	**(Note 1)**
Start condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
Start condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated Start condition
Data input hold time	THD:DAT	0	—	0	—	ns	**(Note 2)**
Data input setup time	TSU:DAT	250	—	100	—	ns	
Stop condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	**(Note 2)**
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 + 0.1 CB	250	ns	**(Note 1)**, CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	**(Note 3)**
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Transmit-Only Mode Parameters							
Output valid from VCLK	TVAA	—	2000	—	1000	ns	
VCLK high time	TVHIGH	4000	—	600	—	ns	
VCLK low time	TVLOW	4700	—	1300	—	ns	
VCLK setup time	TVHST	0	—	0	—	ns	
VCLK hold time	TSPVL	4000	—	600	—	ns	
Mode transition time	TVHZ	—	1000	—	500	ns	
Transmit-only power-up time	TVPU	0	—	0	—	ns	
Input filter spike suppression (VCLK pin)	TSPV	—	100	—	100	ns	
Endurance	—	1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block mode **(Note 4)**

Note 1: Not 100% tested. CB = Total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to Schmitt Trigger inputs which provide noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	24LCS21A Dual Mode I2C Serial EEPROM 24LCS21AT Dual Mode I2C Serial EEPROM (Tape and Reel)	
Temperature Range:	I	= -40°C to +85°C
Package:	P SN	= Plastic DIP (300 mil Body), 8-lead = Plastic SOIC (150 mil Body), 8-lead