Presettable synchronous 4-bit binary counter; asynchronous reset

74HC/HCT161

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Asynchronous reset
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT161 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT161 are synchronous presettable binary counters which feature an internal look-ahead carry and can be used for high-speed counting.
Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP).
The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET).

A LOW level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF;			
	CP to Q_n	V_{CC} = 5 V	19	20	ns
	CP to TC		21	24	ns
	$\overline{MR}$ to Q_n		20	25	ns
	$\overline{MR}$ to TC		20	26	ns
	CET to TC		10	14	ns
f_{max}	maximum clock frequency		44	45	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	33	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

   where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is
   V_I = GND to V_{CC}

   For HCT the condition is
   V_I = GND to V_{CC} – 1.5 V

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{MR}$	0.95
CP	1.10
CEP	0.25
D_n	0.25
CET	0.75
$\overline{PE}$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		23	43		54		65	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay CP to TC		28	48		60		72	ns	4.5	Fig.8
t_{PHL}	propagation delay $\overline{MR}$ to Q_n		29	46		58		69	ns	4.5	Fig.9
t_{PHL}	propagation delay $\overline{MR}$ to TC		30	51		64		77	ns	4.5	Fig.9
t_{PHL}/ t_{PLH}	propagation delay CET to TC		17	35		44		53	ns	4.5	Fig.10
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 8 and 10
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.8
t_W	master reset pulse width; LOW	20	10		25		30		ns	4.5	Fig.9
t_{rem}	removal time $\overline{MR}$ to CP	20	6		25		30		ns	4.5	Fig.9

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{su}	set-up time D_n to CP	18	8		23		27		ns	4.5	Fig.11
t_{su}	set-up time $\overline{PE}$ to CP	30	17		38		45		ns	4.5	Fig.11
t_{su}	set-up time CEP, CET to CP	40	17		50		60		ns	4.5	Fig.12
t_h	hold time D_n, $\overline{PE}$, CEP, CET to CP	0	−7		0		0		ns	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency	23	41		18		15		MHz	4.5	Fig.8