N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
100	0.062 at V_{GS} = 10 V	5.4
	0.084 at V_{GS} = 6 V	4.6

FEATURES

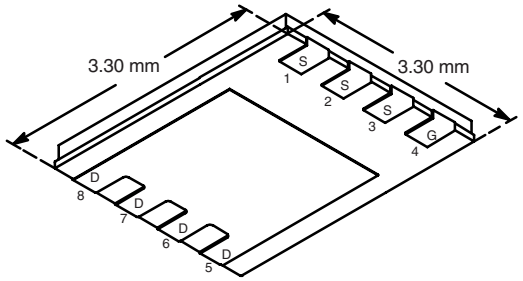
- **Halogen-free Option Available**
- TrenchFET® Power MOSFET
- New Low Thermal Resistance
- PowerPAK® 1212-8 Package with Low 1.07 mm Profile
- PWM Optimized

Pb-free
RoHS COMPLIANT

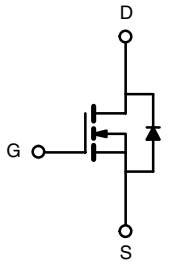
APPLICATIONS

- Primary Side Switch
- In-Rush Current Limiter

PowerPAK 1212-8



Bottom View



N-Channel MOSFET

Ordering Information: Si7810DN-T1-E3 (Lead (Pb)-free)
Si7810DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	5.4	3.4	A
	T_A = 70 °C		4.3	2.8	
Pulsed Drain Current		I_{DM}	20		
Continuous Source Current (Diode Conduction)[a]		I_S	3.2	1.3	A
Single Avalanche Current	L = 0.1 mH	I_{AS}	19		
Single Avalanche Energy (Duty Cycle 1 %)		E_{AS}	18		mJ
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	3.8	1.5	W
	T_A = 70 °C		2.0	0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	– 55 to 150		°C
Soldering Recommendations[b,c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	26	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

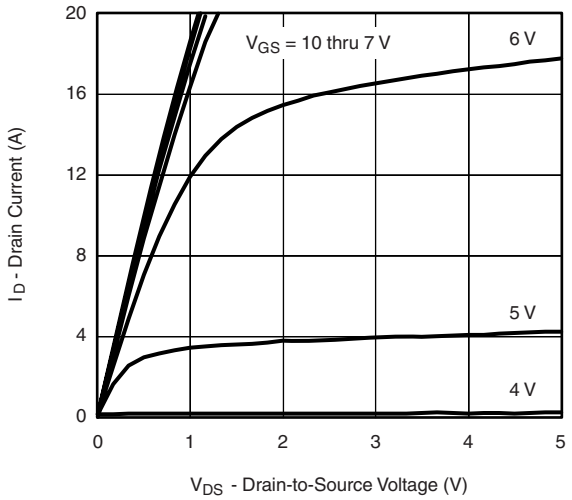
Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2		4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5.4 A		0.052	0.062	Ω
		V_{GS} = 6 V, I_D = 4.6 A		0.070	0.084	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 5.4 A		12		S
Diode Forward Voltage[a]	V_{SD}	I_S = 3.2 A, V_{GS} = 0 V		0.78	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 5.4 A		13.5	17	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			4.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 50 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		10	15	ns
Rise Time	t_r			15	25	
Turn-Off DelayTime	$t_{d(off)}$			20	30	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 3.2 A, dI/dt = 100 A/µs		45	90	

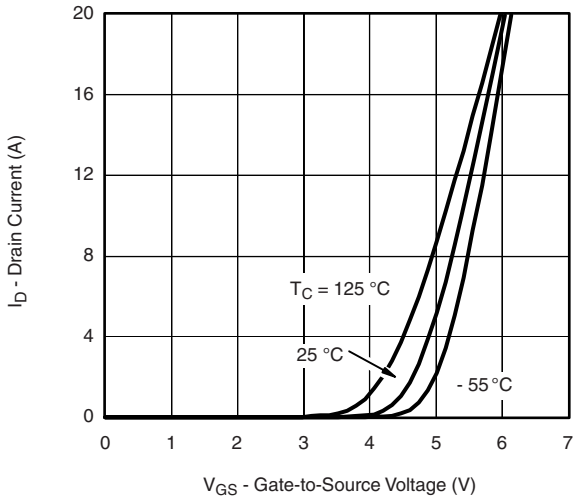
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



Output Characteristics



Transfer Characteristics