MICROCHIP PIC18F46J50 FAMILY

28/44-Pin, Low-Power, High-Performance USB Microcontrollers

Power Management Features with nanoWatt XLP™ for Extreme Low-Power:

- Deep Sleep mode: CPU off, Peripherals off, Currents Down to 13 nA and 850 nA with RTCC
  - Able to wake-up on external triggers, programmable WDT or RTCC alarm
  - Ultra Low-Power Wake-up (ULPWU)
- Sleep mode: CPU off, Peripherals off, SRAM on, Fast Wake-up, Currents Down to 105 nA Typical
- Idle: CPU off, Peripherals on, Currents Down to 2.3 µA Typical
- Run: CPU on, Peripherals on, Currents Down to 6.2 µA Typical
- Timer1 Oscillator w/RTCC: 1 µA, 32 kHz Typical
- Watchdog Timer: 1.3 µA Typical

Special Microcontroller Features:

- 5.5V Tolerant Inputs (digital only pins)
- Low-Power, High-Speed CMOS Flash Technology
- C Compiler Optimized Architecture for Re-Entrant Code
- Priority Levels for Interrupts
- Self-Programmable under Software Control
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Operating Voltage Range of 2.0V to 3.6V
- On-Chip 2.5V Regulator
- Flash Program Memory of 10,000 Erase/Write Cycles Minimum and 20-Year Data Retention

Universal Serial Bus (USB) Features

- USB V2.0 Compliant
- Full Speed (12 Mbps) and Low Speed (1.5 Mbps)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- USB module can use any RAM Location on the Device as USB Endpoint Buffers
- On-Chip USB Transceiver with Crystal-less operation

Flexible Oscillator Structure:

- High-Precision Internal Oscillator (±0.15% typ.) for USB
- Two External Clock modes, up to 48 MHz (12 MIPS)
- Internal 31 kHz Oscillator, Internal Oscillators Tunable at 31 kHz and 8 MHz or 48 MHz with PLL
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops
- Two-Speed Oscillator Start-up
- Programmable Reference Clock Output Generator

Peripheral Highlights:

- Peripheral Pin Select:
  - Allows independent I/O mapping of many peripherals
  - Continuous hardware integrity checking and safety interlocks prevent unintentional configuration changes
- Hardware Real-Time Clock and Calendar (RTCC):
  - Provides clock, calendar and alarm functions
- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Four Programmable External Interrupts
- Four Input Change Interrupts
- Two Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
  - Pulse steering control
- Two Master Synchronous Serial Port (MSSP) modules Supporting Three-Wire SPI (all four modes) and I^2C™ Master and Slave modes
- Full-Duplex Master/Slave SPI DMA Engine
- 8-Bit Parallel Master Port/Enhanced Parallel Slave Port
- Two-Rail – Rail Analog Comparators with Input Multiplexing
- 10-Bit, up to 13-Channel Analog-to-Digital (A/D) Converter module:
  - Auto-acquisition capability
  - Conversion available during Sleep
  - Self-calibration
- High/Low-Voltage Detect module
- Charge Time Measurement Unit (CTMU):
  - Supports capacitive touch sensing for touch screens and capacitive switches
  - Provides a precise resolution time measurement for both flow measurement and simple temperature sensing
- Two Enhanced USART modules:
  - Supports RS-485, RS-232 and LIN/J2602
  - Auto-Wake-up on Start bit
- Auto-Baud Detect

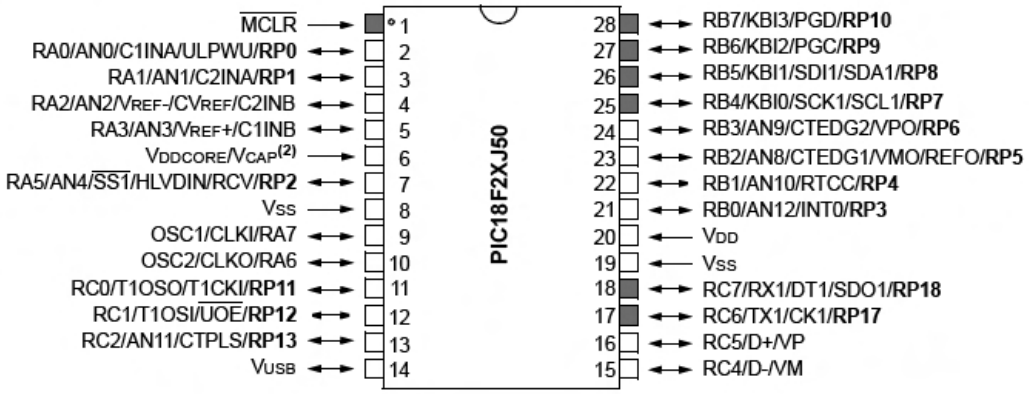
PIC18F/LF[1] Device	Pins	Program Memory (bytes)	SRAM (bytes)	Remappable Pins	Timers 8/16-Bit	ECCP/(PWM)	EUSART	MSSP			10-Bit A/D (ch)	Comparators	Deep Sleep	PMP/PSP	CTMU	RTCC	USB
									SPI w/DMA	I^2C™							
PIC18F24J50	28	16K	3776	16	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y	Y
PIC18F25J50	28	32K	3776	16	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y	Y
PIC18F26J50	28	64K	3776	16	2/3	2	2	2	Y	Y	10	2	Y	N	Y	Y	Y
PIC18F44J50	44	16K	3776	22	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y	Y
PIC18F45J50	44	32K	3776	22	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y	Y
PIC18F46J50	44	64K	3776	22	2/3	2	2	2	Y	Y	13	2	Y	Y	Y	Y	Y
PIC18LF24J50	28	16K	3776	16	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y	Y
PIC18LF25J50	28	32K	3776	16	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y	Y
PIC18LF26J50	28	64K	3776	16	2/3	2	2	2	Y	Y	10	2	N	N	Y	Y	Y
PIC18LF44J50	44	16K	3776	22	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y	Y
PIC18LF45J50	44	32K	3776	22	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y	Y
PIC18LF46J50	44	64K	3776	22	2/3	2	2	2	Y	Y	13	2	N	Y	Y	Y	Y

Note 1: See **Section 1.3 "Details on Individual Family Devices"**, **Section 3.6 "Deep Sleep Mode"** and **Section 26.3 "On-Chip Voltage Regulator"** for details describing the functional differences between PIC18F and PIC18LF variants in this device family.

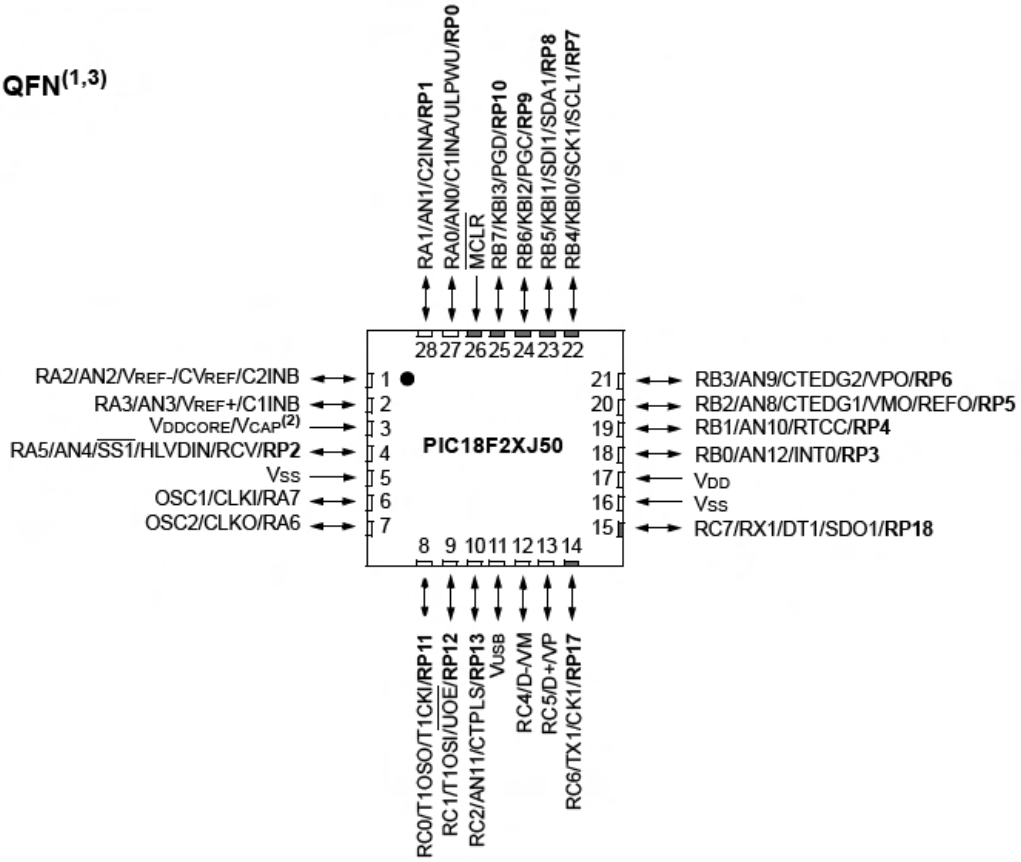
Pin Diagrams

28-Pin SPDIP/SOIC/SSOP(1)

■ = Pins are up to 5.5V tolerant



28-Pin QFN(1,3)



Legend: **RPn** represents remappable pins.

Note 1: Some input and output functions are routed through the Peripheral Pin Select (PPS) module and can be dynamically assigned to any of the RPn pins. For a list of the input and output functions, see Table 9-13 and Table 9-14, respectively. For details on configuring the PPS module, see **Section 9.7 "Peripheral Pin Select (PPS)"**.

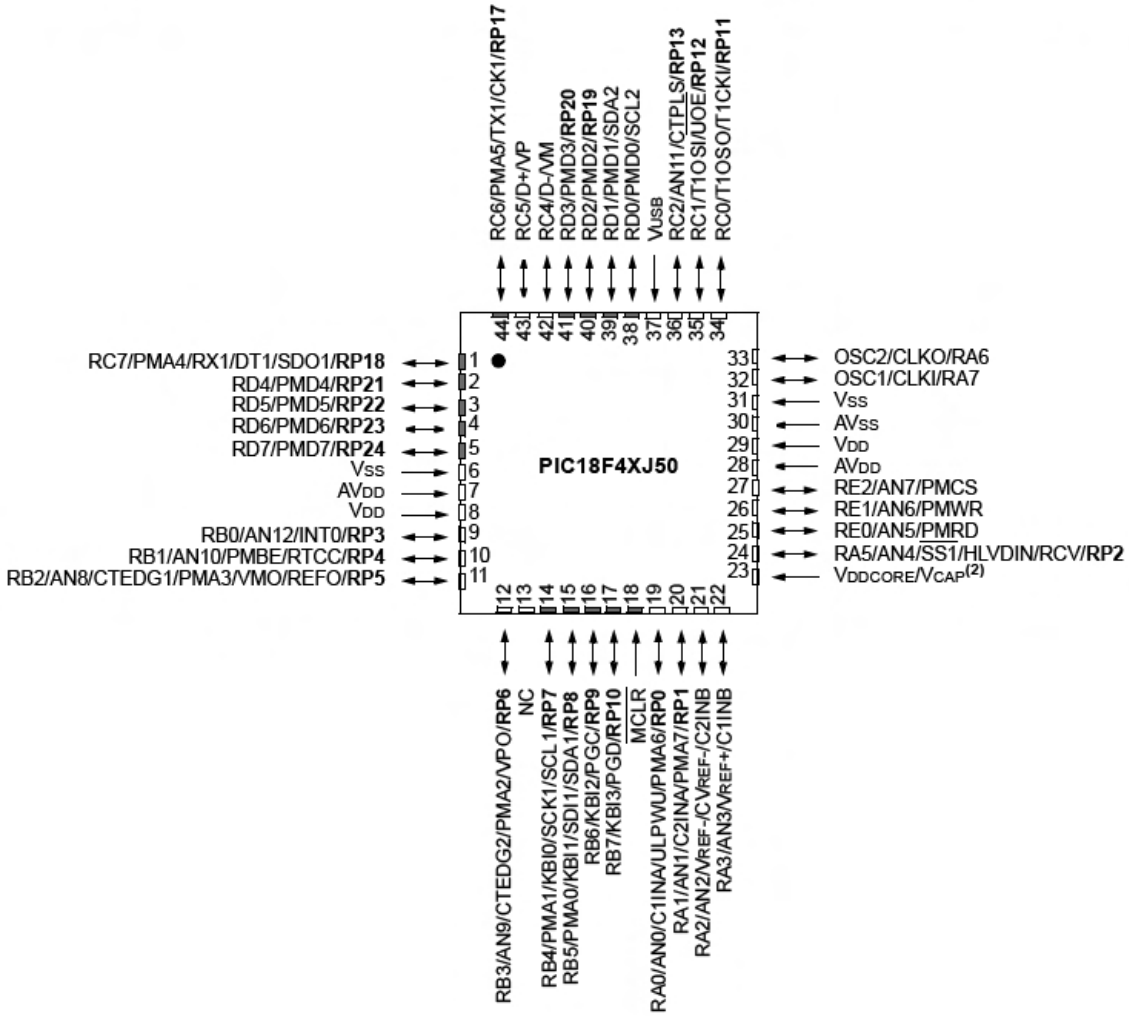
2: See **Section 26.3 "On-Chip Voltage Regulator"** for details on how to connect the VDDCORE/VCAP pin.

3: For the QFN package, it is recommended that the bottom pad be connected to VSS.

Pin Diagrams (Continued)

44-Pin QFN[1,3]

■ = Pins are up to 5.5V tolerant



Legend: **RPn** represents remappable pins.

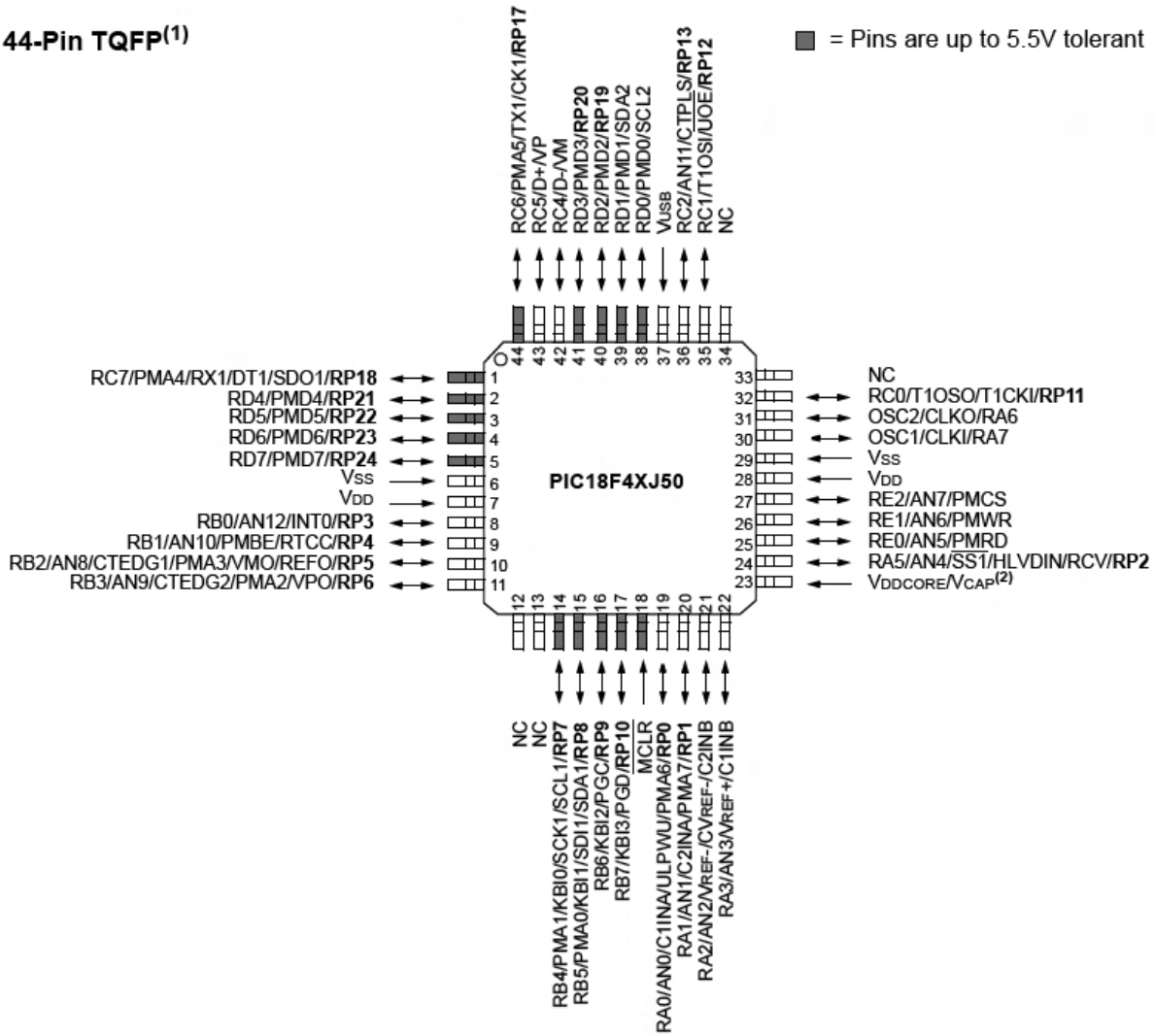
Note 1: Some input and output functions are routed through the Peripheral Pin Select (PPS) module and can be dynamically assigned to any of the RPn pins. For a list of the input and output functions, see Table 9-13 and Table 9-14, respectively. For details on configuring the PPS module, see **Section 9.7 "Peripheral Pin Select (PPS)"**.

2: See **Section 26.3 "On-Chip Voltage Regulator"** for details on how to connect the VDDCORE/VCAP pin.

3: For the QFN package, it is recommended that the bottom pad be connected to VSS.

Pin Diagrams (Continued)

44-Pin TQFP(1)



Legend: **RPn** represents remappable pins.

Note 1: Some input and output functions are routed through the Peripheral Pin Select (PPS) module and can be dynamically assigned to any of the RPn pins. For a list of the input and output functions, see Table 9-13 and Table 9-14, respectively. For details on configuring the PPS module, see **Section 9.7 "Peripheral Pin Select (PPS)"**.

2: See **Section 26.3 "On-Chip Voltage Regulator"** for details on how to connect the VDDCORE/VCAP pin.

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F24J50
- PIC18F25J50
- PIC18F26J50
- PIC18F44J50
- PIC18F45J50
- PIC18F46J50
- PIC18LF24J50
- PIC18LF25J50
- PIC18LF26J50
- PIC18LF44J50
- PIC18LF45J50
- PIC18LF46J50

This family introduces a new line of low-voltage Universal Serial Bus (USB) microcontrollers with the main traditional advantage of all PIC18 microcontrollers, namely, high computational performance and a rich feature set at an extremely competitive price point. These features make the PIC18F46J50 family a logical choice for many high-performance applications, where cost is a primary consideration.

1.1 Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F46J50 family incorporate a range of features that can significantly reduce power consumption during operation. Key features are:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operational requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the users to incorporate power-saving ideas into their application's software design.

1.1.2 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F46J50 family incorporate a fully-featured USB communications module with a built-in transceiver that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types.

1.1.3 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F46J50 family offer five different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-4 clock output.
- An internal oscillator block, which provides an 8 MHz clock and an INTRC source (approximately 31 kHz, stable over temperature and V_{DD}), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of eight clock frequencies. This option frees an oscillator pin for use as an additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to the high-speed crystal, and external and internal oscillators, providing a clock speed up to 48 MHz.
- Dual clock operation, allowing the USB module to run from a high-frequency oscillator while the rest of the microcontroller is clocked at a different frequency.

The internal oscillator block provides a stable reference source that gives the PIC18F46J50 family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset (POR), or wake-up from Sleep mode, until the primary clock source is available.

1.1.4 EXPANDED MEMORY

The PIC18F46J50 family provides ample room for application code, from 16 Kbytes to 64 Kbytes of code space. The Flash cells for program memory are rated to last in excess of 10000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The Flash program memory is readable and writable during normal operation. The PIC18F46J50 family also provides plenty of room for dynamic application data with up to 3.8 Kbytes of data RAM.

1.1.5 EXTENDED INSTRUCTION SET

The PIC18F46J50 family implements the optional extension to the PIC18 instruction set, adding eight new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.

1.1.6 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device.

The PIC18F46J50 family is also pin compatible with other PIC18 families, such as the PIC18F4550, PIC18F2450 and PIC18F45J10. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining the same feature set.

1.2 Other Special Features

- **Communications:** The PIC18F46J50 family incorporates a range of serial and parallel communication peripherals, including a fully featured USB communications module that is compliant with the USB Specification Revision 2.0. This device also includes two independent Enhanced USARTs and two Master Synchronous Serial Port (MSSP) modules, capable of both Serial Peripheral Interface (SPI) and I^2C™ (Master and Slave) modes of operation. The device also has a parallel port and can be configured to serve as either a Parallel Master Port (PMP) or as a Parallel Slave Port (PSP).
- **ECCP Modules:** All devices in the family incorporate three Enhanced Capture/Compare/PWM (ECCP) modules to maximize flexibility in control applications. Up to four different time bases may be used to perform several different operations at once. Each of the ECCPs offers up to four PWM outputs, allowing for a total of eight PWMs. The ECCPs also offer many beneficial features, including polarity selection, programmable dead time, auto-shutdown and restart and Half-Bridge and Full-Bridge Output modes.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 29.0 "Electrical Characteristics"** for time-out periods.

1.3 Details on Individual Family Devices

Devices in the PIC18F46J50 family are available in 28-pin and 44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2. The devices are differentiated from each other in two ways:

- Flash program memory (three sizes: 16 Kbytes for the PIC18FX4J50, 32 Kbytes for PIC18FX5J50 devices and 64 Kbytes for PIC18FX6J50)
- I/O ports (three bidirectional ports on 28-pin devices, five bidirectional ports on 44-pin devices)

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for the PIC18F2XJ50 devices are listed in Table 1-3. The pinouts for the PIC18F4XJ50 devices are shown in Table 1-4.

The PIC18F46J50 family of devices provides an on-chip voltage regulator to supply the correct voltage levels to the core. Parts designated with an "F" part number (such as PIC18**F**46J50) have the voltage regulator enabled.

These parts can run from 2.15V-3.6V on V_{DD}, but should have the V_{DDCORE} pin connected to V_{SS} through a low-ESR capacitor. Parts designated with an "LF" part number (such as PIC18**LF**46J50) do not enable the voltage regulator. For "LF" parts, an external supply of 2.0V-2.7V has to be supplied to the V_{DDCORE} pin while 2.0V-3.6V can be supplied to V_{DD} (V_{DDCORE} should never exceed V_{DD}).

For more details about the internal voltage regulator, see **Section 26.3 "On-Chip Voltage Regulator"**.

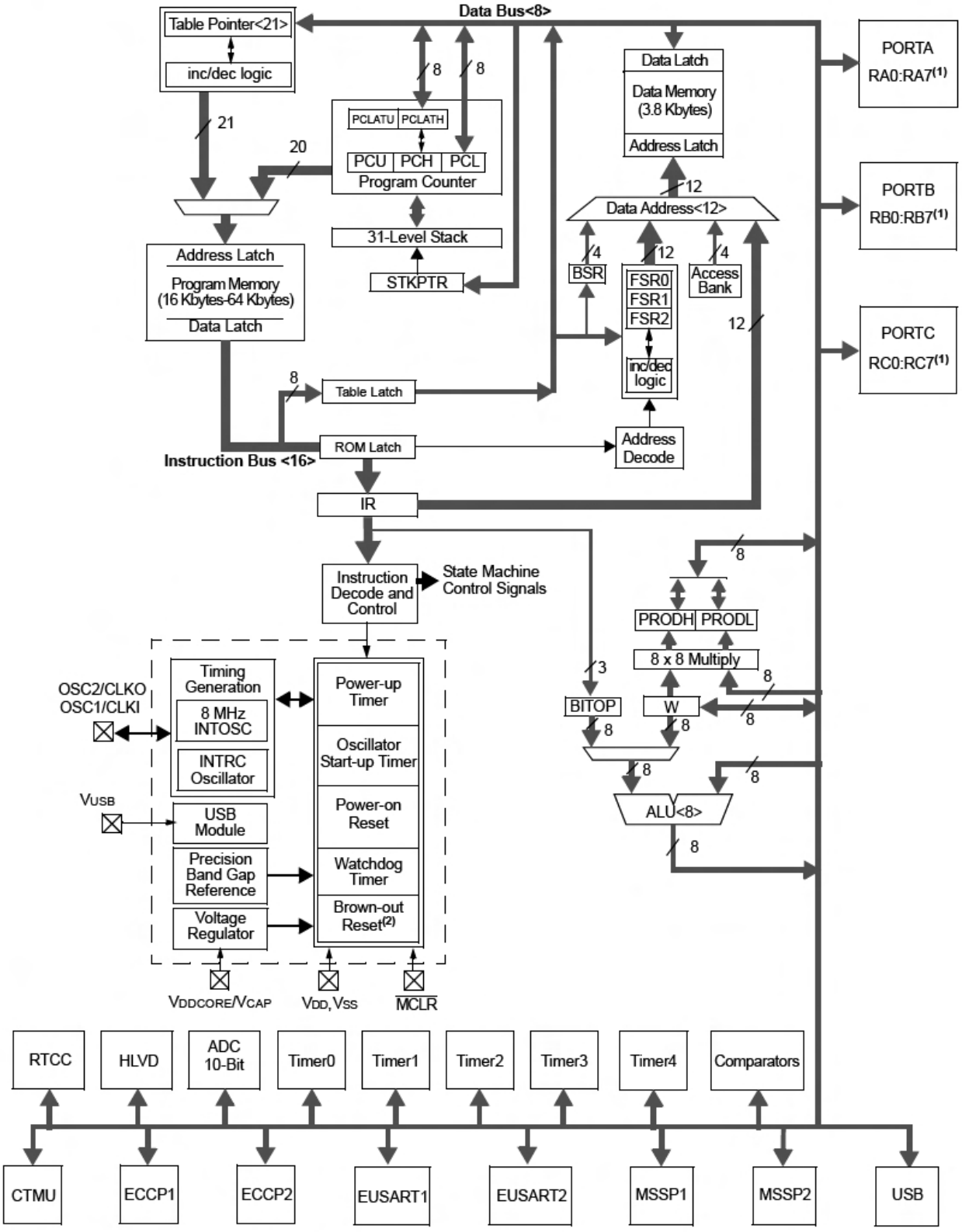
TABLE 1-1: DEVICE FEATURES FOR THE PIC18F2XJ50 (28-PIN DEVICES)

Features	PIC18F24J50	PIC18F25J50	PIC18F26J50
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2), USB		
Parallel Communications (PMP/PSP)	No		
10-Bit Analog-to-Digital Module	10 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	28-Pin QFN, SOIC, SSOP and SPDIP (300 mil)		

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F4XJ50 (44-PIN DEVICES)

Features	PIC18F44J50	PIC18F45J50	PIC18F46J50
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C, D, E		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2), USB		
Parallel Communications (PMP/PSP)	Yes		
10-Bit Analog-to-Digital Module	13 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	44-Pin QFN and TQFP		

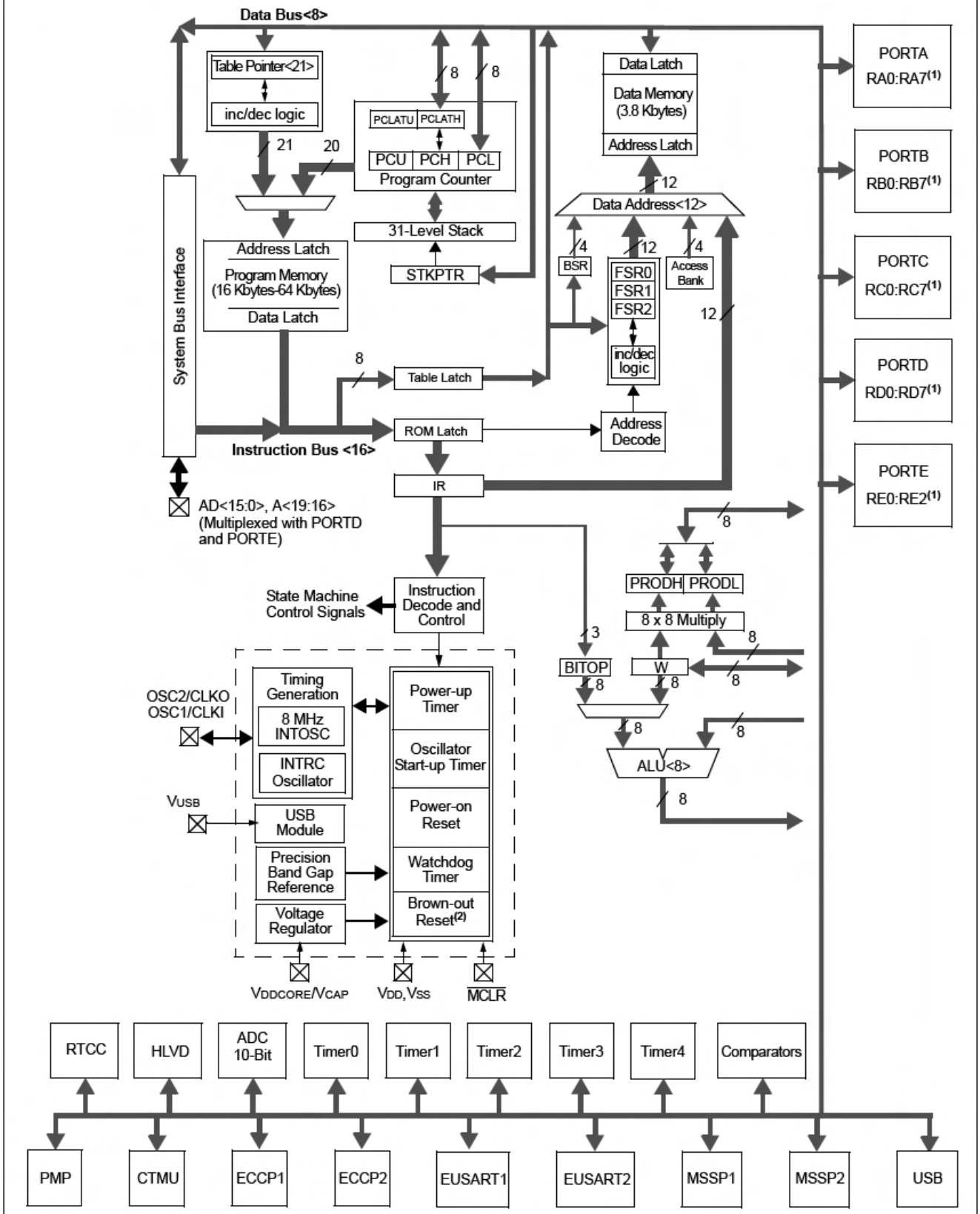
FIGURE 1-1: PIC18F2XJ50 (28-PIN) BLOCK DIAGRAM



Note 1: See Table 1-3 for I/O port pin descriptions.

2: BOR functionality is provided when the on-board voltage regulator is enabled.

FIGURE 1-2: PIC18F4XJ50 (44-PIN) BLOCK DIAGRAM



Note 1: See Table 1-3 for I/O port pin descriptions.

2: The on-chip voltage regulator is always enabled by default.

TABLE 1-3: PIC18F2XJ50 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
$\overline{MCLR}$	1	26	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OSC1/CLKI/RA7	9	6			Oscillator crystal or external clock input.
OSC1			I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. Main oscillator input connection.
CLKI			I	CMOS	External clock source input; always associated with pin function OSC1 (see related OSC1/CLKI pins).
RA7(1)			I/O	TTL	Digital I/O.
OSC2/CLKO/RA6	10	7			Oscillator crystal or clock output.
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	Main oscillator feedback output connection. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6(1)			I/O	TTL	Digital I/O.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); DIG = Digital output; I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F2XJ50 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
					PORTA is a bidirectional I/O port.
RA0/AN0/C1INA/ULPWU/RP0	2	27			
RA0			I/O	DIG	Digital I/O.
AN0			I	Analog	Analog input 0.
C1INA			I	Analog	Comparator 1 input A.
ULPWU			I	Analog	Ultra low-power wake-up input.
RP0			I/O	DIG	Remappable peripheral pin 0 input/output.
RA1/AN1/C2INA/RP1	3	28			
RA1			I	DIG	Digital I/O.
AN1			O	Analog	Analog input 1.
C2INA			I	Analog	Comparator 2 input A.
RP1			I/O	DIG	Remappable peripheral pin 1 input/output.
RA2/AN2/VREF-/CVREF/C2INB	4	1			
RA2			I/O	DIG	Digital I/O.
AN2			I	Analog	Analog input 2.
VREF-			O	Analog	A/D reference voltage (low) input.
CVREF			I	Analog	Comparator reference voltage output.
C2INB			I	Analog	Comparator 2 input B.
RA3/AN3/VREF+/C1INB	5	2			
RA3			I/O	DIG	Digital I/O.
AN3			I	Analog	Analog input 3.
VREF+			I	Analog	A/D reference voltage (high) input.
C1INB			I	Analog	Comparator 1 input B.
RA5/AN4/$\overline{SS1}$/HLVDIN/ RCV/RP2	7	4			
RA5			I/O	DIG	Digital I/O.
AN4			I	Analog	Analog input 4.
$\overline{SS1}$			I	TTL	SPI slave select input.
HLVDIN			I	Analog	Low-voltage detect input.
RCV			I	Analog	External USB transceiver RCV input.
RP2			I/O	DIG	Remappable peripheral pin 2 input/output.
RA6(1)					See the OSC2/CLKO/RA6 pin.
RA7(1)					See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; DIG = Digital output; CMOS = CMOS compatible input or output; Analog = Analog input; O = Output; OD = Open-Drain (no P diode to VDD); I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F2XJ50 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/RP3	21	18			
RB0			I/O	DIG	Digital I/O.
AN12			I	Analog	Analog input 12.
INT0			I	ST	External interrupt 0.
RP3			I/O	DIG	Remappable peripheral pin 3 input/output.
RB1/AN10/RTCC/RP4	22	19			
RB1			I/O	DIG	Digital I/O.
AN10			I	Analog	Analog input 10.
RTCC			O	DIG	Asynchronous serial transmit data output.
RP4			I/O	DIG	Remappable peripheral pin 4 input/output.
RB2/AN8/CTEDG1/VMO/ REFO/RP5	23	20			
RB2			I/O	DIG	Digital I/O.
AN8			I	Analog	Analog input 8.
CTEDG1			I	ST	CTMU edge 1 input.
VMO			O	DIG	External USB transceiver D- data output.
REFO			O	DIG	Reference output clock.
RP5			I/O	DIG	Remappable peripheral pin 5 input/output.
RB3/AN9/CTEDG2/VPO/RP6	24	21			
RB3			I/O	DIG	Digital I/O.
AN9			I	Analog	Analog input 9.
CTEDG2			I/O	ST	CTMU edge 2 input.
VPO			O	DIG	External USB transceiver D+ data output.
RP6			I	DIG	Remappable peripheral pin 6 input/output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); DIG = Digital output; I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F2XJ50 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
					PORTB (continued)
RB4/KBI0/SCK1/SCL1/RP7	25	22			
RB4			I/O	DIG	Digital I/O.
KBI0			I	TTL	Interrupt-on-change pin.
SCK1			I/O	DIG	Synchronous serial clock input/output.
SCL1			I/O	I^2C	I^2C clock input/output.
RP7			I/O	DIG	Remappable peripheral pin 7 input/output.
RB5/KBI1/SDI1/SDA1/RP8	26	23			
RB5			I/O	DIG	Digital I/O.
KBI1			I/O	DIG	Parallel Master Port address.
SDI1			I	ST	SPI data input.
SDA1			I/O	I^2C	I^2C™ data input/output.
RP8			I/O	DIG	Remappable peripheral pin 8 input/output.
RB6/KBI2/PGC/RP9	27	24			
RB6			I/O	DIG	Digital I/O.
KBI2			I	TTL	Interrupt-on-change pin.
PGC			I	ST	ICSP™ clock input.
RP9			I/O	DIG	Remappable peripheral pin 9 input/output.
RB7/KBI3/PGD/RP10	28	25			
RB7			I/O	DIG	Digital I/O.
KBI3			I	TTL	Interrupt-on-change pin.
PGD			I/O	ST	In-Circuit Debugger and ICSP programming data pin.
RP10			I/O	DIG	Remappable peripheral pin 10 input/output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); DIG = Digital output; I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F2XJ50 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI/RP11	11	8			
RC0			I/O	ST	Digital I/O.
T1OSO			O	Analog	Timer1 oscillator output.
T1CKI			I	ST	Timer1 external digital clock input.
RP11			I/O	DIG	Remappable peripheral pin 11 input/output.
RC1/T1OSI/$\overline{\text{UOE}}$/RP12	12	9			
RC1			I/O	ST	Digital I/O.
T1OSI			I	Analog	Timer1 oscillator input.
$\overline{\text{UOE}}$			O	DIG	External USB transceiver NOE output.
RP12			I/O	DIG	Remappable peripheral pin 12 input/output.
RC2/AN11/CTPLS/RP13	13	10			
RC2			I/O	ST	Digital I/O.
AN11			I	Analog	Analog input 11.
CTPLS			O	DIG	CTMU pulse generator output.
RP13			I/O	DIG	Remappable peripheral pin 13 input/output.
RC4/D-/VM	15	12			
RC4			I	TTL	Digital I.
D-			I/O	—	USB bus minus line input/output.
VM			I	TTL	External USB transceiver FM input.
RC5/D+/VP	16	13			
RC5			I	TTL	Digital I.
D+			I/O	DIG	USB bus plus line input/output.
VP			I	TTL	External USB transceiver VP input.
RC6/TX1/CK1/RP17	17	14			
RC6			I/O	ST	Digital I/O.
TX1			O	DIG	EUSART1 asynchronous transmit.
CK1			I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RP17			I/O	DIG	Remappable peripheral pin 17 input/output.
RC7/RX1/DT1/SDO1/RP18	18	15			
RC7			I/O	ST	Digital I/O.
RX1			I	ST	Asynchronous serial receive data input.
DT1			I/O	ST	Synchronous serial data output/input.
SDO1			O	DIG	SPI data output.
RP18			I/O	DIG	Remappable peripheral pin 18 input/output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); DIG = Digital output; I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-3: PIC18F2XJ50 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	28-SPDIP/ SSOP/ SOIC	28-QFN			
VSS1	8	5	P	—	Ground reference for logic and I/O pins.
VSS2	19	16	—	—	
VDD	20	17	P	—	Positive supply for peripheral digital logic and I/O pins.
VDDCORE/VCAP	6	3	—	—	Core logic power or external filter capacitor connection.
VDDCORE			P	—	Positive supply for microcontroller core logic (regulator disabled).
VCAP			P	—	External filter capacitor connection (regulator enabled).
VUSB	14	11	P	—	USB voltage input pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); DIG = Digital output; I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

TABLE 1-4: PIC18F4XJ50 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
$\overline{MCLR}$	18	18	I	ST	Master Clear (Reset) input; this is an active-low Reset to the device.
OSC1/CLKI/RA7	32	30			Oscillator crystal or external clock input.
OSC1			I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS. Main oscillator input connection.
CLKI			I	CMOS	External clock source input; always associated with pin function OSC1 (see related OSC1/CLKI pins).
RA7(1)			I/O	TTL	Digital I/O.
OSC2/CLKO/RA6	33	31			Oscillator crystal or clock output.
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	Main oscillator feedback output connection in RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6(1)			I/O	TTL	Digital I/O.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); DIG = Digital output; I^2C™ = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.