

## Phase-locked-loop with VCO

## 74HC/HCT4046A

### FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at  $V_{CC} = 4.5\text{ V}$
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range:  
VCO section 3.0 to 6.0 V  
digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- $I_{CC}$  category: MSI.

### GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the “4046” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the “4046A” forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The VCO requires one external capacitor C1 (between C1<sub>A</sub> and C1<sub>B</sub>) and one external resistor R1 (between R<sub>1</sub> and GND) or two external resistors R1 and R2 (between R<sub>1</sub> and GND, and R<sub>2</sub> and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is

provided at pin 10 (DEM<sub>OUT</sub>). In contrast to conventional techniques where the DEM<sub>OUT</sub> voltage is one threshold voltage lower than the VCO input voltage, here the DEM<sub>OUT</sub> voltage equals that of the VCO input. If DEM<sub>OUT</sub> is used, a load resistor (R<sub>S</sub>) should be connected from DEM<sub>OUT</sub> to GND; if unused, DEM<sub>OUT</sub> should be left open. The VCO output (VCO<sub>OUT</sub>) can be connected directly to the comparator input (COMP<sub>IN</sub>), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG<sub>IN</sub> (pin 14) or COMP<sub>IN</sub> (pin 3) inputs between the HC and HCT versions.

### Phase comparators

The signal input (SIG<sub>IN</sub>) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

#### Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies ( $f_i$ ) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ( $f_r = 2f_i$ ) is

$$\text{suppressed, is: } V_{\text{DEMOUT}} = \frac{V_{CC}}{\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where  $V_{\text{DEMOUT}}$  is the demodulator output at pin 10;  $V_{\text{DEMOUT}} = V_{\text{PC1OUT}}$  (via low-pass filter).

The phase comparator gain is:  $K_p = \frac{V_{CC}}{\pi} (V/r)$ .

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of signals (SIG<sub>IN</sub>) and the comparator input (COMP<sub>IN</sub>) as shown in Fig.6. The average of  $V_{\text{DEMOUT}}$  is equal to  $\frac{1}{2}V_{CC}$  when there is no signal or noise at SIG<sub>IN</sub> and with this input the VCO oscillates at the centre frequency ( $f_o$ ). Typical waveforms for the PC1 loop locked at  $f_o$  are shown in Fig.7.

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The frequency capture range ( $2f_c$ ) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ( $2f_l$ ) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range.

This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

### Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of  $SIG_{IN}$  and  $COMP_{IN}$  are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig.5) where  $SIG_{IN}$  causes an up-count and  $COMP_{IN}$  a down-count. The transfer function of PC2, assuming ripple ( $f_r = f_i$ ) is suppressed,

$$\text{is: } V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{4\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where  $V_{\text{DEMOUT}}$  is the demodulator output at pin 10;  
 $V_{\text{DEMOUT}} = V_{\text{PC2OUT}}$  (via low-pass filter).

The phase comparator gain is:  $K_p = \frac{V_{\text{CC}}}{4\pi} (V/r)$ .

$V_{\text{DEMOUT}}$  is the resultant of the initial phase differences of  $SIG_{IN}$  and  $COMP_{IN}$  as shown in Fig.8. Typical waveforms for the PC2 loop locked at  $f_o$  are shown in Fig.9.

When the frequencies of  $SIG_{IN}$  and  $COMP_{IN}$  are equal but the phase of  $SIG_{IN}$  leads that of  $COMP_{IN}$ , the p-type output driver at  $PC2_{\text{OUT}}$  is held "ON" for a time corresponding to the phase difference ( $\phi_{\text{DEMOUT}}$ ). When the phase of  $SIG_{IN}$  lags that of  $COMP_{IN}$ , the n-type driver is held "ON".

When the frequency of  $SIG_{IN}$  is higher than that of  $COMP_{IN}$ , the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the  $SIG_{IN}$  frequency is lower than the  $COMP_{IN}$  frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to  $PC2_{\text{OUT}}$  varies until the signal

and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output ( $PCP_{\text{OUT}}$ ) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between  $SIG_{IN}$  and  $COMP_{IN}$  over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at  $SIG_{IN}$  the VCO adjusts, via PC2, to its lowest frequency.

### Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of  $SIG_{IN}$  and  $COMP_{IN}$  are not important. The transfer characteristic of PC3, assuming ripple ( $f_r = f_i$ ) is suppressed,

$$\text{is: } V_{\text{DEMOUT}} = \frac{V_{\text{CC}}}{2\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

where  $V_{\text{DEMOUT}}$  is the demodulator output at pin 10;  
 $V_{\text{DEMOUT}} = V_{\text{PC3OUT}}$  (via low-pass filter).

The phase comparator gain is:  $K_p = \frac{V_{\text{CC}}}{2\pi} (V/r)$ .

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 ( $V_{\text{DEMOUT}}$ ), is the resultant of the phase differences of  $SIG_{IN}$  and  $COMP_{IN}$  as shown in Fig.10. Typical waveforms for the PC3 loop locked at  $f_o$  are shown in Fig.11.

The phase-to-output response characteristic of PC3 (Fig.10) differs from that of PC2 in that the phase angle between  $SIG_{IN}$  and  $COMP_{IN}$  varies between  $0^\circ$  and  $360^\circ$  and is  $180^\circ$  at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at  $SIG_{IN}$  the VCO adjusts, via PC3, to its lowest frequency.

## Phase-locked-loop with VCO

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**QUICK REFERENCE DATA**GND = 0 V; T<sub>amb</sub> = 25 °C

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f <sub>o</sub>	VCO centre frequency	C1 = 40 pF; R1 = 3 kΩ; V <sub>CC</sub> = 5 V	19	19	MHz
C <sub>i</sub>	input capacitance (pin 5)		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	24	24	pF

**Notes**

- C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz.  
 f<sub>o</sub> = output frequency in MHz.  
 C<sub>L</sub> = output load capacitance in pF.  
 V<sub>CC</sub> = supply voltage in V.  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
- Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

**ORDERING INFORMATION**See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.**APPLICATIONS**

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

**PACKAGE OUTLINES**See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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## RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
$V_{CC}$	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
$V_I$	DC input voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$V_O$	DC output voltage range	0		$V_{CC}$	0		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times (pin 5)		6.0	1000		6.0	500	ns	$V_{CC} = 2.0\text{ V}$
			6.0	500		6.0	500	ns	$V_{CC} = 4.5\text{ V}$
			6.0	400		6.0	500	ns	$V_{CC} = 6.0\text{ V}$

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$
$\pm I_O$	DC output source or sink current		25	mA	for $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$
$\pm I_{CC}; \pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: - 40 to +125 °C
	plastic DIL		750	mW	74HC/HCT above + 70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above + 70 °C: derate linearly with 8 mW/K

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## DC CHARACTERISTICS FOR 74HC

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I <sub>CC</sub>	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V <sub>CC</sub> ; pin 9 at GND; I <sub>I</sub> at pins 3 and 14 to be excluded	

## Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS		
		74HC									V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V <sub>IH</sub>	DC coupled HIGH level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>	1.5	1.2		1.5		1.5		V	2.0			
		3.15	2.4		3.15		3.15			4.5			
		4.2	3.2		4.2		4.2			6.0			
V <sub>IL</sub>	DC coupled LOW level input voltage SIG <sub>IN</sub> , COMP <sub>IN</sub>		0.8	0.5		0.5		0.5	V	2.0			
			2.1	1.35		1.35		1.35		4.5			
			2.8	1.8		1.8		1.8		6.0			
V <sub>OH</sub>	HIGH level output voltage PCP <sub>OUT</sub> , PC <sub>nOUT</sub>	1.9	2.0		1.9		1.9		V	2.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA	
		4.4	4.5		4.4		4.4			4.5		-I <sub>O</sub> = 20 μA	
		5.9	6.0		5.9		5.9			6.0		-I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage PCP <sub>OUT</sub> , PC <sub>nOUT</sub>	3.98	4.32		3.84		3.7		V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA	
		5.48	5.81		5.34		5.2			6.0		-I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage PCP <sub>OUT</sub> , PC <sub>nOUT</sub>		0	0.1		0.1		0.1	V	2.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA	
			0	0.1		0.1		0.1		4.5		I <sub>O</sub> = 20 μA	
			0	0.1		0.1		0.1		6.0		I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage PCP <sub>OUT</sub> , PC <sub>nOUT</sub>		0.15	0.26		0.33		0.4	V	4.5	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA	
			0.16	0.26		0.33		0.4		6.0		I <sub>O</sub> = 5.2 mA	
±I <sub>I</sub>	input leakage current SIG <sub>IN</sub> , COMP <sub>IN</sub>			3.0		4.0		5.0	μA	2.0	V <sub>CC</sub> or GND		
				7.0		9.0		11.0		3.0			
				18.0		23.0		27.0		4.5			
				30.0		38.0		45.0		6.0			
±I <sub>OZ</sub>	3-state OFF-state current PC2 <sub>OUT</sub>			0.5		5.0		10.0	μA	6.0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	

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SYM-BOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
R <sub>I</sub>	input resistance SIG <sub>IN</sub> , COMP <sub>IN</sub>		800 250 150					kΩ kΩ kΩ	3.0 4.5 6.0	V <sub>I</sub> at self-bias operating point; Δ V <sub>I</sub> = 0.5 V; see Figs 12, 13 and 14		

**VCO section**

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2	V	3.0 4.5 6.0			
V <sub>IL</sub>	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8	0.9 1.35 1.8	V	3.0 4.5 6.0			
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9	V	3.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA -I <sub>O</sub> = 20 μA	
V <sub>OH</sub>	HIGH level output voltage VCO <sub>OUT</sub>	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	V	3.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA I <sub>O</sub> = 20 μA	
V <sub>OL</sub>	LOW level output voltage VCO <sub>OUT</sub>		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
V <sub>OL</sub>	LOW level output voltage C1 <sub>A</sub> , C1 <sub>B</sub>			0.40 0.40		0.47 0.47	0.54 0.54	V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA	
±I <sub>I</sub>	input leakage current INH, VCO <sub>IN</sub>			0.1		1.0	1.0	μA	6.0	V <sub>CC</sub> or GND		
R1	resistor range	3.0 3.0 3.0		300 300 300				kΩ	3.0 4.5 6.0		note 1	

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SYM-BOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HC								V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R <sub>2</sub>	resistor range	3.0		300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40		no limit					pF	3.0 4.5 6.0		
V <sub>VCOIN</sub>	operating voltage range at V <sub>VCOIN</sub>	1.1		1.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 20 and 21

**Note**

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

**Demodulator section**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> V	OTHER
		+25			-40 to+85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R <sub>S</sub>	resistor range	50		300					kΩ	3.0 4.5 6.0	at R <sub>S</sub> > 300 kΩ the leakage current can influence V <sub>DEMOUT</sub>
V <sub>OFF</sub>	offset voltage V <sub>VCOIN</sub> to V <sub>DEMOUT</sub>		±30 ±20 ±10						mV	3.0 4.5 6.0	V <sub>I</sub> = V <sub>VCOIN</sub> = 1/2 V <sub>CC</sub> ; values taken over R <sub>S</sub> range; see Fig.15
R <sub>D</sub>	dynamic output resistance at DEM <sub>OUT</sub>		25 25 25						Ω	3.0 4.5 6.0	V <sub>DEMOUT</sub> = 1/2 V <sub>CC</sub>

## Phase-locked-loop with VCO

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## AC CHARACTERISTICS FOR 74HC

## Phase comparator section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/$ $t_{PLH}$	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC1 <sub>OUT</sub>		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.16
$t_{PHL}/$ $t_{PLH}$	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PCP <sub>OUT</sub>		96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig.16
$t_{PHL}/$ $t_{PLH}$	propagation delay SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC3 <sub>OUT</sub>		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig.16
$t_{PZH}/$ $t_{PZL}$	3-state output enable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		83 30 24	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig.17
$t_{PHZ}/$ $t_{PLZ}$	3-state output disable time SIG <sub>IN</sub> , COMP <sub>IN</sub> to PC2 <sub>OUT</sub>		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig.17
$t_{THL}/$ $t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.16
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG <sub>IN</sub> or COMP <sub>IN</sub>		9 11 15 33						mV	2.0 3.0 4.5 6.0	$f_i = 1$ MHz



## Phase-locked-loop with VCO

## 74HC/HCT4046A

## VCO section

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	typ.	max.	min.				max.
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2 V_{CC}$ ; $R1 = 100$ k $\Omega$ ; $R2 = \infty$ ; $C1 = 100$ pF; see Fig.18
$f_o$	VCO centre frequency (duty factor = 50%)	7.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2 V_{CC}$ ; $R1 = 3$ k $\Omega$ ; $R2 = \infty$ ; $C1 = 40$ pF; see Fig.19
$\Delta f_{VCO}$	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	$R1 = 100$ k $\Omega$ ; $R2 = \infty$ ; $C1 = 100$ pF; see Figs 20 and 21
$\delta_{VCO}$	duty factor at $V_{COOUT}$		50 50 50						%	3.0 4.5 6.0	

## DC CHARACTERISTICS FOR 74HCT

## Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$I_{CC}$	quiescent supply current (VCO disabled)			8.0		80.0		160.0	$\mu$ A	6.0	pins 3, 5 and 14 at $V_{CC}$ ; pin 9 at GND; $I_I$ at pins 3 and 14 to be excluded
$\Delta I_{CC}$	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	$\mu$ A	4.5 to 5.5	pins 3 and 14 at $V_{CC}$ ; pin 9 at GND; $I_I$ at pins 3 and 14 to be excluded

## Note

- The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given above. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00