Quad 2-input NAND gate 74HC/HCT03

FEATURES

- Level shift capability
- Output capability: standard (open drain)
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PLZ}	propagation delay	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + \sum (V_O^2/R_L) \times \text{duty factor LOW, where:}$$

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   V_O = output voltage in V
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   R_L = pull-up resistor in MΩ
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   $\sum (V_O^2/R_L)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V
3. The given value of C_{PD} is obtained with:
   C_L = 0 pF and R_L = ∞

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	–0.5	+7	V	
V_O	DC output voltage	–0.5	+7	V	
I_{IK}	DC input diode current		20	mA	for $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V
$–I_{OK}$	DC output diode current		20	mA	for $V_O < –0.5$ V
$–I_O$	DC output sink current		25	mA	for $– 0.5 V < V_O$
$±I_{CC}$; $±I_{GND}$	DC VCC or GND current		50	mA	
T_{stg}	storage temperature range	–65	+150	°C	
P_{tot}	power dissipation per package				for temperature range; –40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			–40 to +85		–40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	µA	2.0 to 6.0	V_{IL}	$V_O = V_{O(max)}$[1] or GND

Note

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig.6
t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6