Dual JK flip-flop with reset; negative-edge trigger 74HC/HCT107

FEATURES

- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ $n\overline{CP}$ to $n\overline{Q}$ $n\overline{R}$ to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	 16 16 16	 16 18 17	 ns ns ns
f_{max}	maximum clock frequency		78	73	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V.

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to nQ		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}$ to $n\overline{Q}$		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$		52 19 15	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	reset pulse width LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time $n\overline{R}$ to $n\overline{CP}$	60 12 10	19 7 6		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time nJ, nK to $n\overline{CP}$	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.6
t_h	hold time nJ, nK to $n\overline{CP}$	3 3 3	−6 −2 −2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.6
f_{max}	maximum clock pulse frequency	6.0 30 35	23 70 85		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6