

SMPS MOSFET IRF830APbF

HEXFET® Power MOSFET

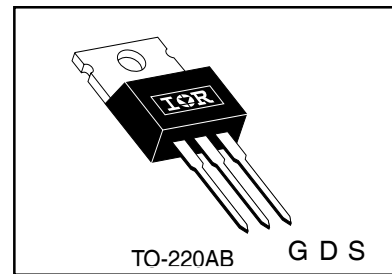
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching
- Lead-Free

V_{DSS}	R_{ds(on)} max	I_D
500V	1.40Ω	5.0A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN 1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	5.0	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	3.2	
I _{DM}	Pulsed Drain Current ①	20	
P _D @ T _C = 25°C	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	5.3	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies:

- Two transistor Forward
- Half Bridge and Full Bridge

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.4	Ω	$V_{GS} = 10V, I_D = 3.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25 250	μA	$V_{DS} = 500V, V_{GS} = 0V$ $V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	2.8	—	—	S	$V_{DS} = 50V, I_D = 3.0A$
Q_g	Total Gate Charge	—	—	24	nC	$I_D = 5.0A$ $V_{DS} = 400V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④
Q_{gs}	Gate-to-Source Charge	—	—	6.3		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	11		
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 250V$ $I_D = 5.0A$ $R_G = 14\Omega$ $R_D = 49\Omega$, See Fig. 10 ④
t_r	Rise Time	—	21	—		
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		
t_f	Fall Time	—	15	—		
C_{iss}	Input Capacitance	—	620	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	93	—		
C_{riss}	Reverse Transfer Capacitance	—	4.3	—		
C_{oss}	Output Capacitance	—	886	—		
C_{oss}	Output Capacitance	—	27	—		
$C_{oss\text{ eff.}}$	Effective Output Capacitance	—	39	—		

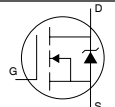
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	230	mJ
I_{AR}	Avalanche Current①	—	5.0	A
E_{AR}	Repetitive Avalanche Energy①	—	7.4	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.7	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

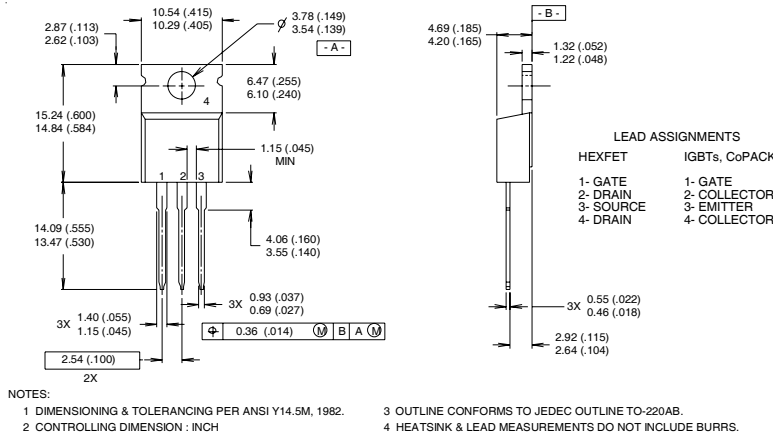
Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	20		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 5.0A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	430	650	ns	$T_J = 25^\circ\text{C}, I_F = 5.0A$
Q_{rr}	Reverse Recovery Charge	—	1.62	2.4	μC	$di/dt = 100A/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

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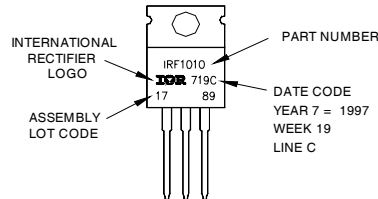
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TO-220AB Package Outline



TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line
 position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 18\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 5.0\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 370\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

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