

## High-Speed, Low-Glitch D/CMOS Analog Switches

### DESCRIPTION

The DG611/612/613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

Each switch conducts equally well in both directions when on and blocks up to 16 V<sub>p-p</sub> when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611/612/613 are built on the Vishay Siliconix proprietary D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

For additional information see Applications Note AN207 (FaxBack number 70605).

### FEATURES

- Fast Switching - t<sub>ON</sub>: 12 ns
- Low Charge Injection: ± 2 pC
- Wide Bandwidth: 500 MHz
- 5 V CMOS Logic Compatible
- Low r<sub>DS(on)</sub>: 18 Ω
- Low Quiescent Power : 1.2 nW
- Single Supply Operation

### BENEFITS

- Improved Data Throughput
- Minimal Switching Transients
- Improved System Performance
- Easily Interfaced
- Low Insertion Loss
- Minimal Power Consumption

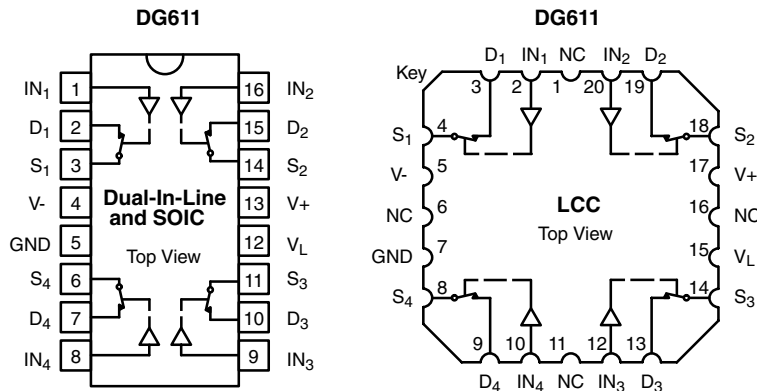
### APPLICATIONS

- Fast Sample-and-Holds
- Synchronous Demodulators
- Pixel-Rate Video Switching
- Disk/Tape Drives
- DAC Deglitching
- Switched Capacitor Filters
- GaAs FET Drivers
- Satellite Receivers



**RoHS\***  
COMPLIANT

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



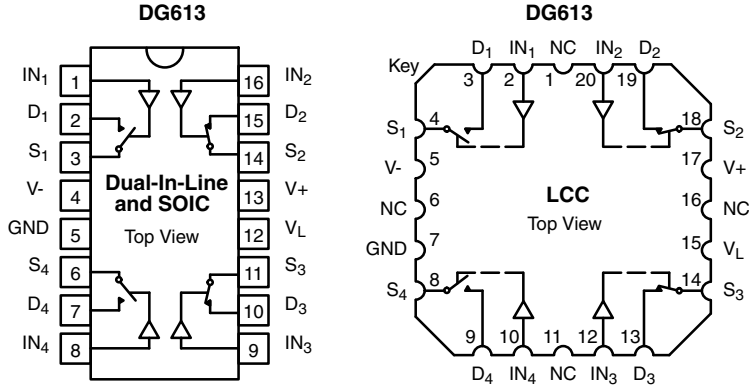
Four SPST Switches per Package

| TRUTH TABLE |       |       |
|-------------|-------|-------|
| Logic       | DG611 | DG612 |
| 0           | ON    | OFF   |
| 1           | OFF   | ON    |

Logic "0" ≤ 1 V  
Logic "1" ≥ 4 V

\* Pb containing terminations are not RoHS compliant, exemptions may apply

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four SPST Switches per Package

| TRUTH TABLE |                                   |                                   |
|-------------|-----------------------------------|-----------------------------------|
| Logic       | SW <sub>1</sub> , SW <sub>4</sub> | SW <sub>2</sub> , SW <sub>3</sub> |
| 0           | OFF                               | ON                                |
| 1           | ON                                | OFF                               |

Logic "0" ≤ 1 V  
 Logic "1" ≥ 4 V

| ORDERING INFORMATION |                    |  |
|----------------------|--------------------|--|
| Temp Range           | Package            | Part Number  |
| <b>DG611/612</b>     |                    |  |
| - 40 to 85 °C        | 16-Pin Plastic DIP | DG611DJ<br>DG611DJ-E3                                |
|                      |                    | DG612DJ<br>DG612DJ-E3                                |
|                      | 16-Pin Narrow SOIC | DG611DY<br>DG611DY-E3<br>DG611DY-T1<br>DG611DY-T1-E3 |
|                      |                    | DG612DY<br>DG612DY-E3<br>DG612DY-T1<br>DG612DY-T1-E3 |
| <b>DG613</b>         |                    |  |
| - 40 to 85 °C        | 16-Pin Plastic DIP | DG613DJ<br>DG613DJ-E3                                |
|                      | 16-Pin Narrow SOIC | DG613DY<br>DG613DY-E3<br>DG613DY-T1<br>DG613DY-T1-E3 |



| ABSOLUTE MAXIMUM RATINGS                          |   |             |    |
|---|---|-------------|----|
| Parameter   | Limit   | Unit        |    |
| V <sub>+</sub> to V <sub>-</sub>                  | - 0.3 to 21   | V           |    |
| V <sub>+</sub> to GND                             | - 0.3 to 21   |             |    |
| V <sub>-</sub> to GND                             | - 19 to 0.3   |             |    |
| V <sub>L</sub> to GND                             | - 1 to (V <sub>+</sub> ) + 1<br>or 20 mA, whichever occurs first                      |             |    |
| V <sub>IN</sub> <sup>a</sup>                      | (V <sub>-</sub> ) - 1 to (V <sub>+</sub> ) + 1<br>or 20 mA, whichever occurs first    |             |    |
| V <sub>S</sub> , V <sub>D</sub> <sup>a</sup>      | (V <sub>-</sub> ) - 0.3 to (V <sub>+</sub> ) + 16<br>or 20 mA, whichever occurs first |             |    |
| Continuous Current (Any Terminal)                 | ± 30  | mA          |    |
| Current, S or D (Pulsed at 1 μs, 10 % Duty Cycle) | ± 100   |             |    |
| Storage Temperature                               | CerDIP  | - 65 to 150 | °C |
|   | Plastic   | - 65 to 125 |    |
| Power Dissipation (Package) <sup>b</sup>          | 16-Pin Plastic DIP <sup>c</sup>   | 470         | mW |
|   | 16-Pin Narrow SOIC <sup>d</sup>   | 600         |    |
|   | 16-Pin CerDIP <sup>e</sup>  | 900         |    |
|   | 20-Pin LCC <sup>e</sup>   | 900         |    |

## Notes:

- Signals on S<sub>x</sub>, D<sub>x</sub>, or IN<sub>x</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6 mW/°C above 75 °C.
- Derate 7.6 mW/°C above 75 °C.
- Derate 12 mW/°C above 75 °C.

| RECOMMENDED OPERATING RANGE |   |      |
|-----------------------------|---|------|
| Parameter                   | Limit                                   | Unit |
| V <sub>+</sub>              | 5 to 21                                 | V    |
| V <sub>-</sub>              | - 10 to 0                               |      |
| V <sub>L</sub>              | 4 to V <sub>+</sub>                     |      |
| V <sub>IN</sub>             | 0 to V <sub>L</sub>                     |      |
| V <sub>ANALOG</sub>         | V <sub>-</sub> to (V <sub>+</sub> ) - 5 |      |



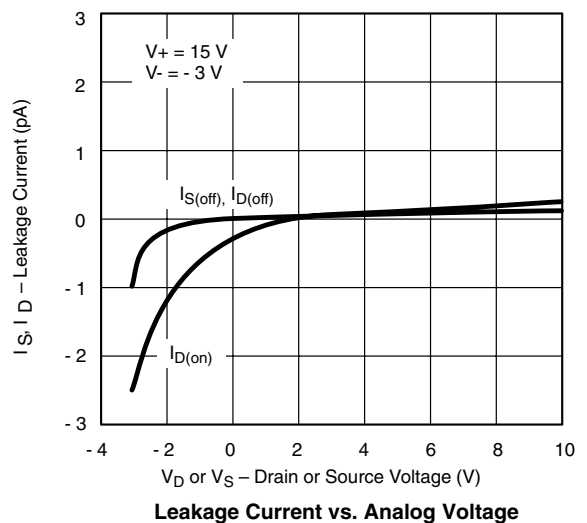
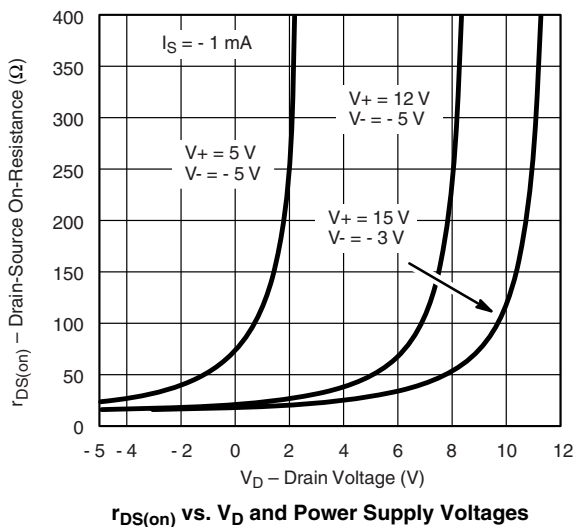
| SPECIFICATIONS <sup>a</sup>         |                      |  |                   |                  |                            |                  |                           |                  |      |    |
|-------------------------------------|----------------------|--|-------------------|------------------|----------------------------|------------------|---------------------------|------------------|------|----|
| Parameter                           | Symbol               | Test Conditions<br>Unless Otherwise Specified<br>V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V<br>V <sub>L</sub> = 5 V, V <sub>IN</sub> = 4 V, 1 V <sup>f</sup> | Temp <sup>b</sup> | Typ <sup>c</sup> | A Suffix<br>- 55 to 125 °C |                  | D Suffix<br>- 40 to 85 °C |                  | Unit |    |
|                                     |                      |  |                   |                  | Min <sup>d</sup>           | Max <sup>d</sup> | Min <sup>d</sup>          | Max <sup>d</sup> |      |    |
| <b>Analog Switch</b>                |                      |  |                   |                  |                            |                  |                           |                  |      |    |
| Analog Signal Range <sup>e</sup>    | V <sub>ANALOG</sub>  | V <sub>-</sub> = -5 V, V <sub>+</sub> = 12 V   | Full              |                  | -5                         | 7                | -5                        | 7                | V    |    |
| Switch On-Resistance                | r <sub>DS(on)</sub>  | I <sub>S</sub> = -1 mA, V <sub>D</sub> = 0 V   | Room              | 18               |                            | 45               |                           | 45               | Ω    |    |
| Resistance Match Bet Ch.            | Δr <sub>DS(on)</sub> |  | Room              | 2                |                            |                  |                           | 60               |      |    |
| Source Off Leakage                  | I <sub>S(off)</sub>  | V <sub>S</sub> = 0 V, V <sub>D</sub> = 10 V  | Room              | ± 0.001          | -0.25                      | 0.25             | -0.25                     | 0.25             | nA   |    |
| Drain Off Leakage Current           | I <sub>D(off)</sub>  | V <sub>S</sub> = 10 V, V <sub>D</sub> = 0 V  | Room              |                  | -20                        | 20               | -20                       | 20               |      |    |
| Switch On Leakage Current           | I <sub>D(on)</sub>   | V <sub>S</sub> = V <sub>D</sub> = 0 V  | Room              | ± 0.001          | -0.4                       | 0.4              | -0.4                      | 0.4              |      |    |
| <b>Digital Control</b>              |                      |  |                   |                  |                            |                  |                           |                  |      |    |
| Input Voltage High                  | V <sub>IH</sub>      |  | Full              |                  | 4                          |                  | 4                         |                  | V    |    |
| Input Voltage Low                   | V <sub>IL</sub>      |  | Full              |                  |                            | 1                |                           | 1                |      |    |
| Input Current                       | I <sub>IN</sub>      |  | Room              | 0.005            | -1                         | 1                | -1                        | 1                | μA   |    |
| Input Capacitance                   | C <sub>IN</sub>      |  | Room              |                  | 5                          |                  |                           |                  |      |    |
| <b>Dynamic Characteristics</b>      |                      |  |                   |                  |                            |                  |                           |                  |      |    |
| Off State Input Capacitance         | C <sub>S(off)</sub>  | V <sub>S</sub> = 0 V   | Room              | 3                |                            |                  |                           |                  | pF   |    |
| Off State Output Capacitance        | C <sub>D(off)</sub>  | V <sub>D</sub> = 0 V   | Room              | 2                |                            |                  |                           |                  |      |    |
| On State Input Capacitance          | C <sub>S(on)</sub>   | V <sub>S</sub> = V <sub>D</sub> = 0 V  | Room              | 10               |                            |                  |                           |                  |      |    |
| Bandwidth                           | BW                   | R <sub>L</sub> = 50 Ω  | Room              | 500              |                            |                  |                           |                  | MHz  |    |
| Turn-On Time <sup>e</sup>           | t <sub>ON</sub>      | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 3 pF<br>V <sub>S</sub> = ± 2 V,<br>See Test Circuit, Figure 2   | Room              | 12               |                            | 25               |                           | 25               | ns   |    |
| Turn-Off Time <sup>e</sup>          | t <sub>OFF</sub>     |  | Room              | 8                |                            | 20               |                           | 20               |      |    |
| Turn-On Time                        | t <sub>ON</sub>      | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 75 pF<br>V <sub>S</sub> = ± 2 V,<br>See Test Circuit, Figure 2  | Room              | 19               |                            | 35               |                           | 35               |      |    |
| Turn-Off Time                       | t <sub>OFF</sub>     |  | Room              | 16               |                            | 25               |                           | 25               |      |    |
| Charge Injection <sup>e</sup>       | Q                    | C <sub>L</sub> = 1 nF, V <sub>S</sub> = 0 V  | Room              | 4                |                            |                  |                           |                  | pC   |    |
| Ch. Injection Change <sup>e,g</sup> | ΔQ                   | C <sub>L</sub> = 1 nF,  V <sub>S</sub>   ≤ 3 V   | Room              | 3                |                            | 4                |                           | 4                |      |    |
| Off Isolation <sup>e</sup>          | OIRR                 | R <sub>IN</sub> = 50 Ω, R <sub>L</sub> = 50 Ω<br>f = 5 MHz   | Room              | 74               |                            |                  |                           |                  | dB   |    |
| Crosstalk <sup>e</sup>              | X <sub>TALK</sub>    | R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 50 Ω<br>f = 5 MHz   | Room              | 87               |                            |                  |                           |                  |      |    |
| <b>Power Supplies</b>               |                      |  |                   |                  |                            |                  |                           |                  |      |    |
| Positive Supply Current             | I <sub>+</sub>       | V <sub>IN</sub> = 0 V or 5 V   | Room              | 0.005            |                            | 1                |                           | 1                | μA   |    |
| Negative Supply Current             | I <sub>-</sub>       |  | Full              |                  | -0.005                     | -1               | -5                        | -1               |      | -5 |
| Logic Supply Current                | I <sub>L</sub>       |  | Room              |                  | 0.005                      |                  | 1                         |                  |      | 1  |
| Ground Current                      | I <sub>GND</sub>     |  | Full              |                  | -0.005                     | -1               | -5                        | -1               |      | -5 |

| <b>SPECIFICATIONS FOR UNIPOLAR SUPPLIES<sup>a</sup></b> |              |   |                   |                  |                            |                  |                           |                  |          |
|---|--------------|---|-------------------|------------------|----------------------------|------------------|---------------------------|------------------|----------|
| Parameter   | Symbol       | Test Conditions<br>Unless Otherwise Specified<br>$V_+ = 15\text{ V}$ , $V_- = -3\text{ V}$<br>$V_L = 5\text{ V}$ , $V_{IN} = 4\text{ V}$ , $1\text{ V}^f$ | Temp <sup>b</sup> | Typ <sup>c</sup> | A Suffix<br>- 55 to 125 °C |                  | D Suffix<br>- 40 to 85 °C |                  | Unit     |
|   |              |   |                   |                  | Min <sup>d</sup>           | Max <sup>d</sup> | Min <sup>d</sup>          | Max <sup>d</sup> |          |
| <b>Analog Switch</b>                                    |              |   |                   |                  |                            |                  |                           |                  |          |
| Analog Signal Range <sup>e</sup>                        | $V_{ANALOG}$ |   | Full              |                  | 0                          | 7                | 0                         | 7                | V        |
| Switch On-Resistance                                    | $r_{DS(on)}$ | $I_S = -1\text{ mA}$ , $V_D = 1\text{ V}$   | Room              | 25               |                            | 60               |                           | 60               | $\Omega$ |
| <b>Dynamic Characteristics</b>                          |              |   |                   |                  |                            |                  |                           |                  |          |
| Turn-On Time <sup>e</sup>                               | $t_{ON}$     | $R_L = 300\ \Omega$ , $C_L = 3\text{ pF}$<br>$V_S = 2\text{ V}$ ,<br>See Test Circuit, Figure 2   | Room              | 15               |                            | 30               |                           | 30               | ns       |
| Turn-Off Time <sup>e</sup>                              | $t_{OFF}$    |   | Room              | 10               |                            | 25               |                           | 25               |          |

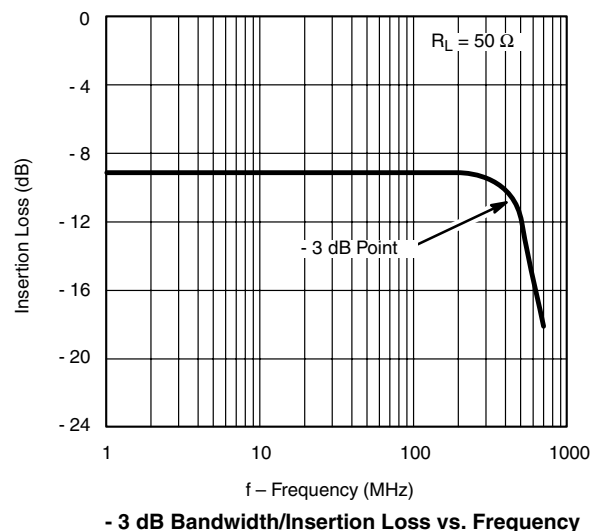
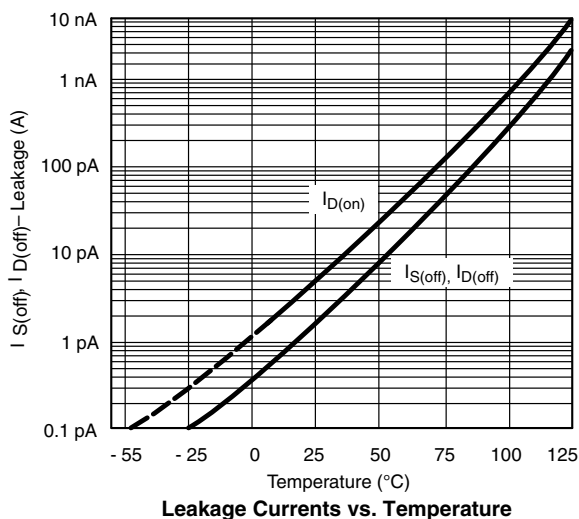
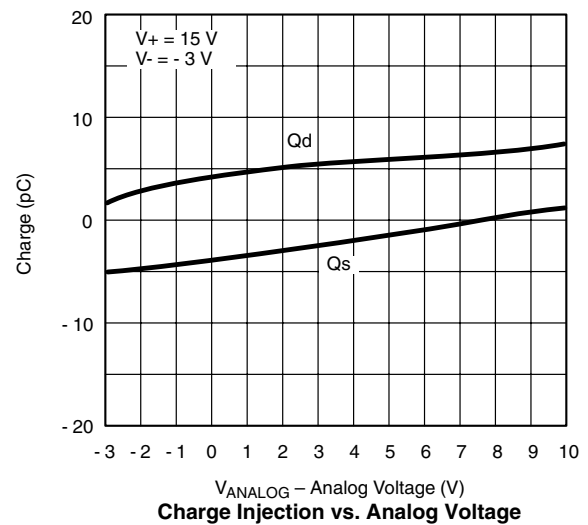
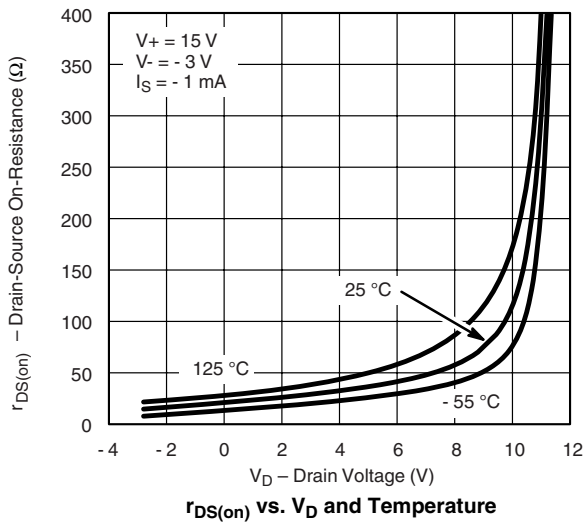
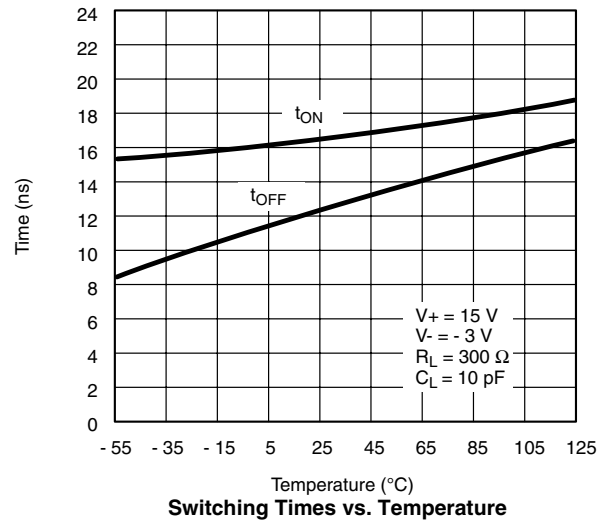
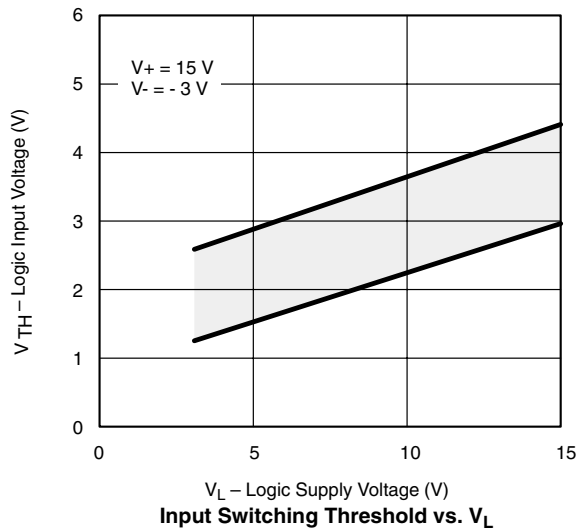
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.
- $\Delta Q = |Q|$  at  $V_S = 3\text{ V}$  -  $Q$  at  $V_S = -3\text{ V}$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


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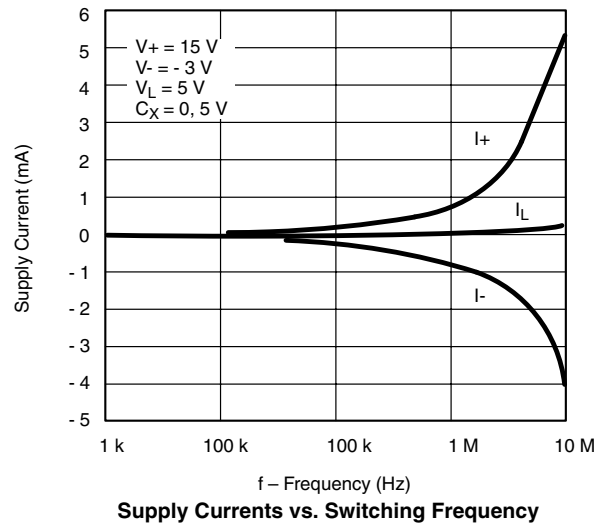
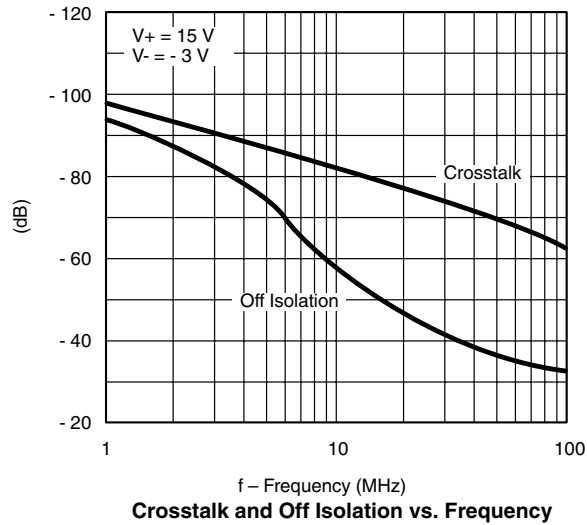
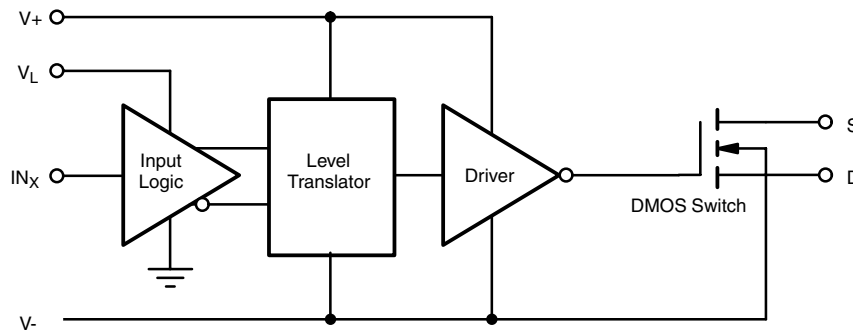
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**


Figure 1.

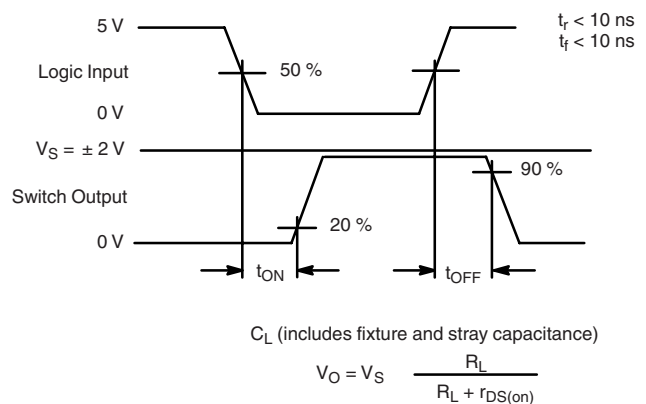
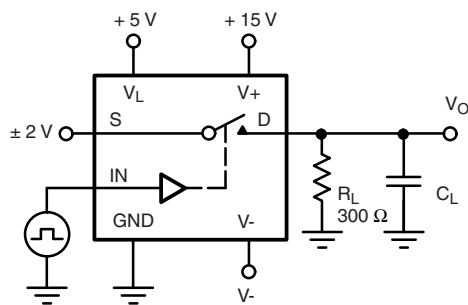
**TEST CIRCUITS**


Figure 2. Switching Time

**TEST CIRCUITS**

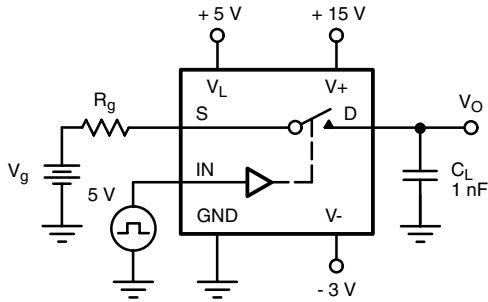
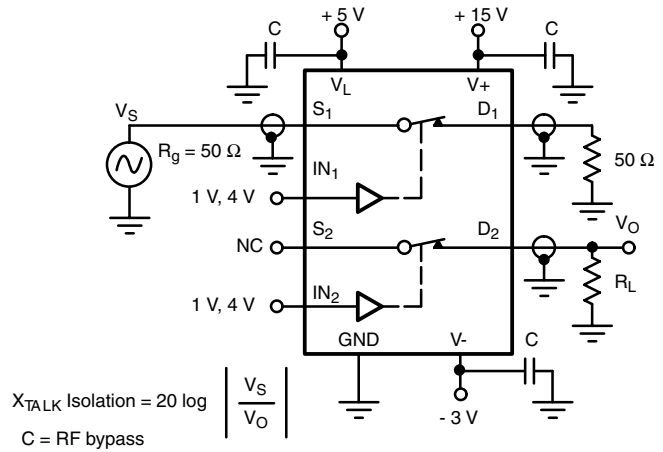


Figure 3. Charge Injection



$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 4. Crosstalk

**APPLICATIONS**

**High-Speed Sample-and-Hold**

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The CLC111, a fast input buffer, helps to shorten acquisition and settling times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (See Figure 5.)

**Pixel-Rate Switch**

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video sources must be sync locked. The glitch-less analog switch eliminates halos. (See Figure 6.)

**GaAs FET Drivers**

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S<sub>1</sub>, whereas to turn it off, - 8 V are applied via S<sub>2</sub>. This high-speed, low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.

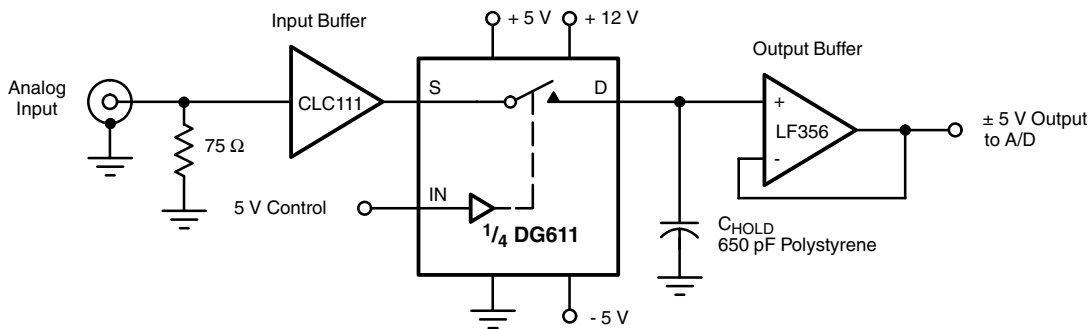
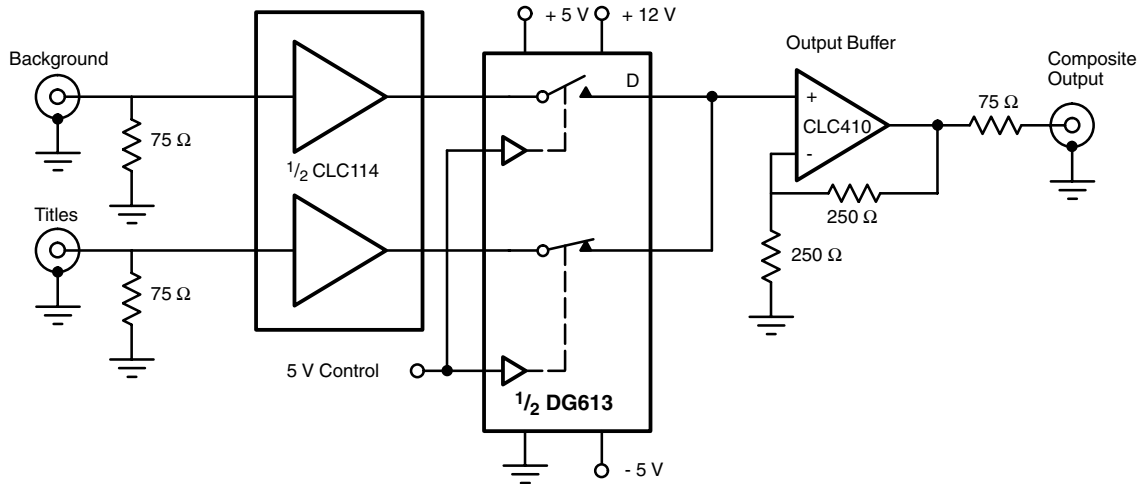
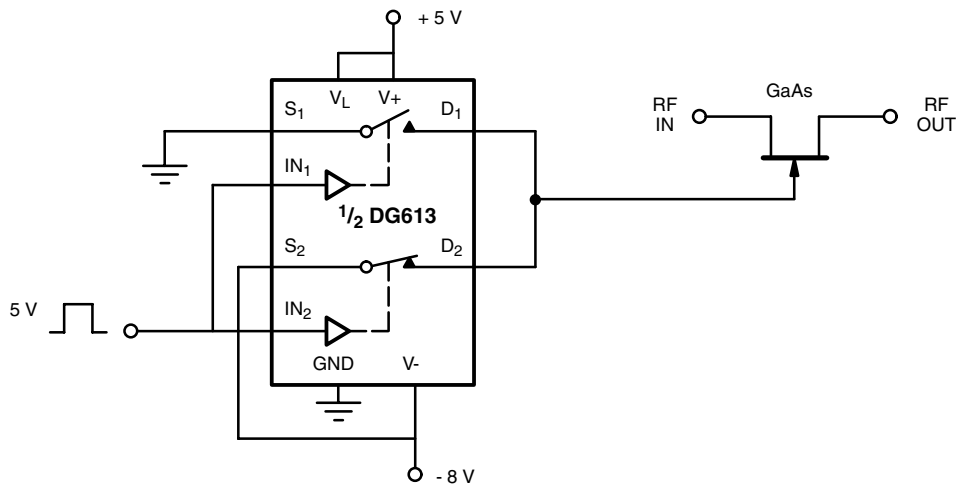


Figure 5. High-Speed Sample-and-Hold



**APPLICATIONS**

**Figure 6. A Pixel-Rate Switch Creates Title Overlays**

**Figure 7. A High-Speed GaAs FET Driver that Saves Power**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70057>.



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