Quad buffer/line driver; 3-state

74HC/HCT125

FEATURES

· Output capability: bus driver

I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}C$; $t_r = t_f = 6 \, \text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT	
STWIBOL	PARAMETER	CONDITIONS	нс	нст	UNIT
t _{PHL} / t _{PLH}	propagation delay nA to nY	C _L = 15 pF; V _{CC} = 5 V	9	12	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	22	24	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

f_o = output frequency in MHz

C_I = output load capacitance in pF

V_{CC} = supply voltage in V

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

Philips Semiconductors Product specification

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

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AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL		74HC									WAVEFORMS
		+25			-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORWIS
		min.	typ.	max.	min.	max.	min.	max.		(•)	
t _{PHL} / t _{PLH}	propagation delay nA to nY		30	100		125		150	ns	2.0	Fig.6
			11	20		25		30		4.5	
			9	17		21		26		6.0	
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		41	125		155		190	ns	2.0	Fig.7
			15	25		31		38		4.5	
			12	21		26		32		6.0	
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		41	125		155		190	ns	2.0	Fig.7
			15	25		31		38		4.5	
			12	21		26		32		6.0	
t _{THL} / t _{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.6
			5	12		15		18		4.5	
			4	10		13		15		6.0	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT						
nA, n OE	1.00						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
SYMBOL		74HCT									WAVEFORMS
		+25			−40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		, ,	
t _{PHL} / t _{PLH}	propagation delay nA to nY		15	25		31		38	ns	4.5	Fig.6
t _{PZH} / t _{PZL}	3-state output enable time nOE to nY		15	28		35		42	ns	4.5	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time nOE to nY		15	25		31		38	ns	4.5	Fig.7
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6