74HC4040; 74HCT4040

12-stage binary ripple counter

Product data sheet

1. General description

The 74HC4040; 74HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4040B series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4040; 74HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

2. Features

- Multiple package options
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114-C exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC4040						
t_{PHL}, t_{PLH}	propagation delay					
	$\overline{CP}$ to Q0	C_L = 15 pF; V_{CC} = 5 V	-	14	-	ns
	Qn to Qn+1	C_L = 15 pF; V_{CC} = 5 V	-	8	-	ns

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum operating frequency	C_L = 15 pF; V_{CC} = 5 V	-	90	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	-	20	-	pF
Type 74HCT4040						
t_{PHL}, t_{PLH}	propagation delay					
	$\overline{CP}$ to Q0	C_L = 15 pF; V_{CC} = 5 V	-	16	-	ns
	Qn to Qn+1	C_L = 15 pF; V_{CC} = 5 V	-	8	-	ns
f_{max}	maximum operating frequency	C_L = 15 pF; V_{CC} = 5 V	-	79	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V	-	20	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4040N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC4040D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4040DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4040PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4040BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4040N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT4040D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

8.2 Timing diagram

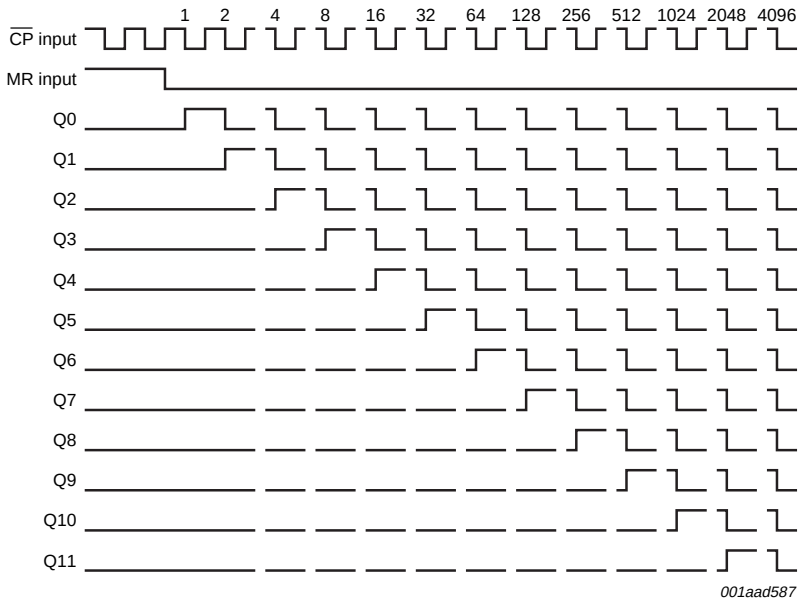


Fig 7. Timing diagram

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or VI > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output diode current	$V_I < –0.5$ V or $V_I > V_{CC}$ + 0.5 V	-	±20	mA
I_O	output source or sink current	$–0.5 V < V_O < V_{CC}$ + 0.5 V	-	±25	mA
I_{CC}	quiescent supply current		-	±50	mA
I_{GND}	ground current		-	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[1]		
	DIP16 package		-	750	mW
	SO16, SSOP16, TSSOP16 and DHVQFN16 packages		-	500	mW

[1] For DIP16 packages: above 70 °C, P_{tot} derates linearly with 12 mW/K.
For SO16, SSOP16, TSSOP16 and DHVQFN16 packages, above 70 °C, P_{tot} derates linearly with 8 mW/K.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
type 74HC4040						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	see Section 11 and 12 per device	–40	-	+125	°C
t_r, t_f	input rise and fall times	except for Schmitt-trigger inputs				
		V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
type 74HCT4040						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	see Section 11 and 12 per device	–40	-	+125	°C
t_r, t_f	input rise and fall times	except for Schmitt-trigger inputs				
		V_{CC} = 2.0 V	-	-	-	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	-	ns

11. Static characteristics

Table 7: Static characteristics for 74HC4040

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V

Table 7: Static characteristics for 74HC4040 *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V;	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80.0	µA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V

Table 7: Static characteristics for 74HC4040 *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20$ µA; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V;	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	160.0	µA

Table 8: Static characteristics for 74HCT4040

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	0	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		$\overline{CP}$	-	85	306	µA
		MR	-	110	396	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V

12. Dynamic characteristics

Table 9: Dynamic characteristics for type 74HC4040

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	47	150	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	17	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	14	26	ns
	propagation delay Qn to Qn+1	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	28	100	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	10	20	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	8	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	8	17	ns
t_{PHL}	propagation delay MR to Qn	see Figure 8				
		V_{CC} =2.0 V; C_L = 50 pF	-	61	185	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	22	37	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	18	31	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	19	75	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	7	15	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	6	13	ns
t_W	clock pulse width HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	80	14	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	16	5	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	14	4	-	ns
	master reset pulse width; HIGH	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	80	22	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	16	8	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	14	6	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	50	8	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	10	3	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	9	2	-	ns
f_{max}	maximum operating frequency	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	6.0	27	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF	30	82	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	90	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF	35	98	-	MHz
C_{PD}	power dissipation capacitance		-	20	-	pF

Table 9: Dynamic characteristics for type 74HC4040 *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	190	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	38	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	33	ns
	propagation delay Qn to Qn+1	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	125	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	25	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	21	ns
t_{PHL}	propagation delay MR to Qn	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	230	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	46	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	39	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	95	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	19	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	16	ns
t_W	clock pulse width HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	100	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	20	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	17	-	-	ns
	master reset pulse width; HIGH	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	100	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	20	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	17	-	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	65	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	13	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	11	-	-	ns
f_{max}	maximum operating frequency	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	4.8	-	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF	24	-	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF	28	-	-	MHz

Table 9: Dynamic characteristics for type 74HC4040 *...continued*

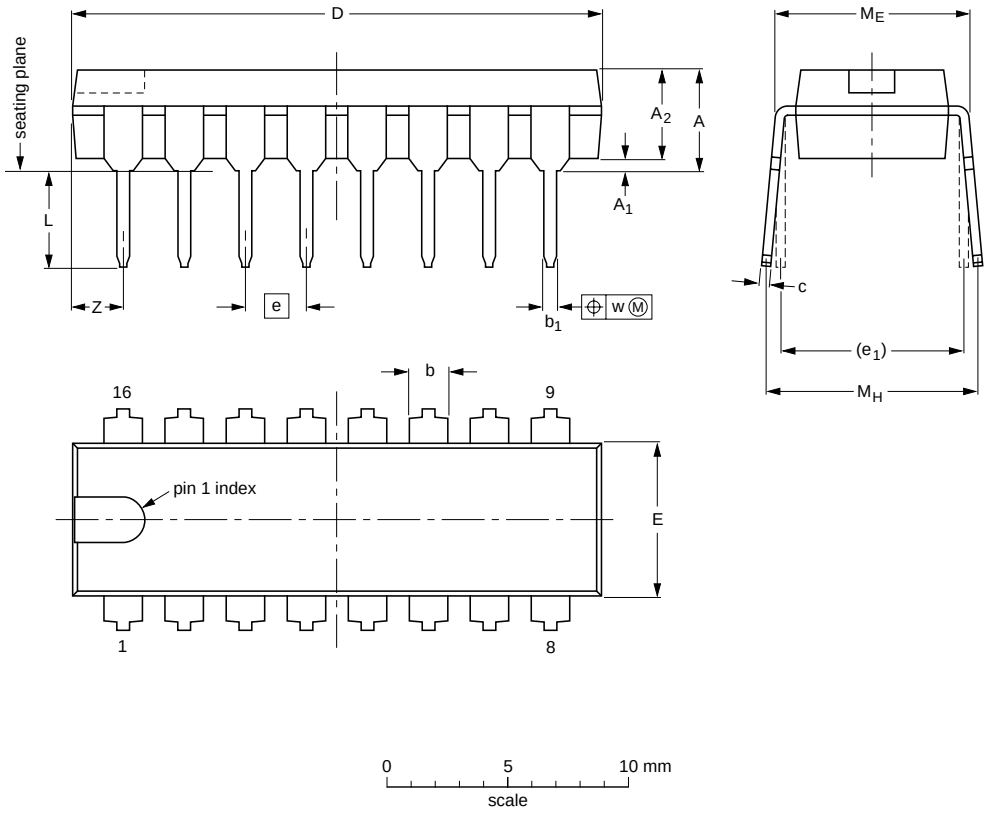
GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	225	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	45	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	38	ns
	propagation delay Qn to Qn+1	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	150	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	30	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	26	ns
t_{PHL}	propagation delay MR to Qn	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	280	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	56	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	48	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	110	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	22	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	19	ns
t_W	clock pulse width HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	120	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	24	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	20	-	-	ns
	master reset pulse width; HIGH	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	120	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	24	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	20	-	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	75	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	15	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	13	-	-	ns
f_{max}	maximum operating frequency	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	4.0	-	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF	20	-	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF	24	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

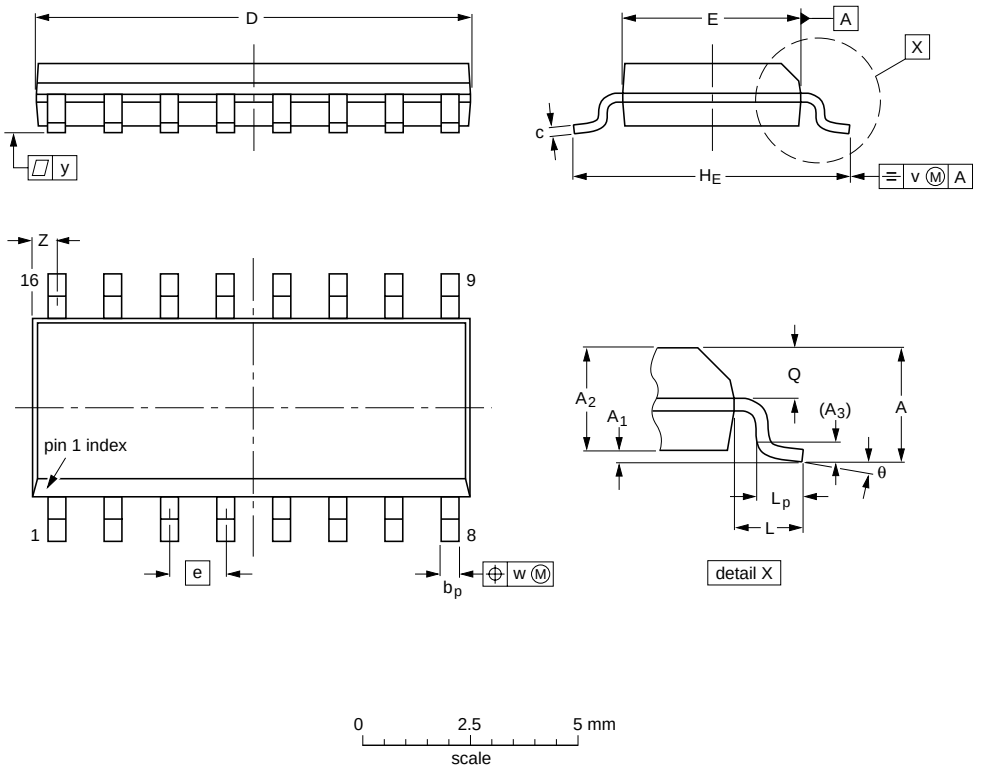
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			

Fig 10. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				

Fig 11. Package outline SOT109-1 (SO16)