

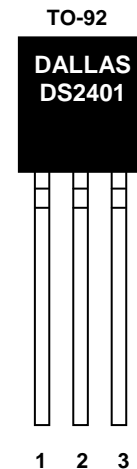


DS2401 Silicon Serial Number

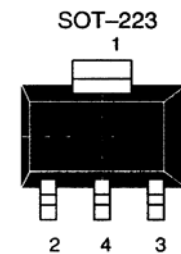
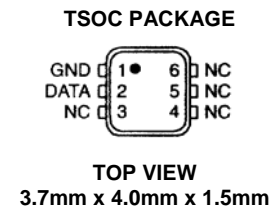
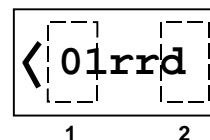
FEATURES

- Upgrade and drop-in replacement for DS2400
 - Extended 2.8 to 6.0 voltage range
 - Multiple DS2401s can reside on a common 1-Wire[®] Net
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester); guaranteed no two parts alike
- Built-in multidrop controller ensures compatibility with other 1-Wire Net products
- 8-bit family code specifies DS2401 communications requirements to reader
- Presence Pulse acknowledges when the reader first applies voltage
- Low-cost TO-92, SOT-223, and TSOC surface mount packages
- Reduces control, address, data, and power to a single pin
- Zero standby power required
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
- TO-92 Tape & Reel version with leads bent to 100mil spacing (default) or with straight leads (DS2401T-SL)
- Applications
 - PCB Identification
 - Network Node ID
 - Equipment Registration
- Operates over industrial temperature range of -40°C to +85°C

PIN ASSIGNMENT



BOTTOM VIEW

TOP VIEW
See Mech. Drawings Section

Flip Chip, Top View with Laser Mark, Contacts Not Visible. "rrrd" = Revision/Date

PIN DESCRIPTION

	TO-92, SOT-223	TSOC	Flip Chip
Pin 1	Ground	Ground	Data (DQ)
Pin 2	Data (DQ)	Data (DQ)	Ground
Pin 3	No Connect	No Connect	—
Pin 4	Ground	No Connect	—
Pin 5-6	—	No Connect	—

ORDERING INFORMATION

<u>Standard</u>	<u>Lead-Free</u>	<u>Description</u>
DS2401	DS2401+	TO-92 Package
DS2401/T&R	DS2401+T&R	TO-92 Package, Tape-and-Reel
DS2401/T&R/SL	DS2401-SL+T&R	TO-92 Package with Straight Leads, Tape-and-Reel
DS2401Z	DS2401Z+	SOT-223 Surface-Mount Package
DS2401Z/T&R	DS2401Z+T&R	SOT-223 Surface-Mount Package, Tape-and-Reel
DS2401P	DS2401P+	TSOC Surface-Mount Package
DS2401P/T&R	DS2401P+T&R	TSOC Surface-Mount Package, Tape-and-Reel
DS2401X1	—	Flip-Chip Package, Tape & Reel

DESCRIPTION

The DS2401 enhanced Silicon Serial Number is a low-cost, electronic registration number that provides an absolutely unique identity which can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The DS2401 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol that requires only a single data lead and a ground return. Power for reading and writing the device is derived from the data line itself with no need for an external power source. The DS2401 is an upgrade to the DS2400. The DS2401 is fully reverse-compatible with the DS2400 but provides the additional multi-drop capability that enables many devices to reside on a single data line. The familiar TO-92, SOT-223 or TSOC package provides a compact enclosure that allows standard assembly equipment to handle the device easily.

OPERATION

The DS2401's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

1-Wire BUS SYSTEM

The 1-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS2401 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing).

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open-drain connection or 3-state outputs. The DS2401 is an open-drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pullup resistor should be approximately 5k Ω for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbits per second.

The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 μ s, one or more of the devices on the bus may be reset.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{PUP} = 2.8V$ to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		$V_{CC} + 0.3$	V	1,6
Logic 0	V_{IL}	-0.3		+0.3	V	1
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1,2
Input Load Current	I_L		5		μA	3
Operating Charge	Q_{OP}			30	nC	7,8

CAPACITANCE ($t_A = +25^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$			800	pF	9

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{PUP} = 2.8V$ to 6.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	μs	
Write 1 Low Time	t_{LOW1}	1		15	μs	12
Write 0 Low Time	t_{LOW0}	60		120	μs	
Read Data Valid	t_{RDV}		15		μs	11
Release Time	$t_{RELEASE}$	0	15	45	μs	
Read Data Setup	t_{SU}			1	μs	5
Recovery Time	t_{REC}	1			μs	
Reset Time High	t_{RSTH}	480			μs	4
Reset Time Low	t_{RSTL}	480		960	μs	10
Presence Detect High	t_{PDH}	15		60	μs	
Presence Detect Low	t_{PDL}	60		240	μs	

NOTES:

- 1) All voltages are referenced to ground.
- 2) V_{PUP} = external pullup voltage.
- 3) Input load is to ground.
- 4) An additional reset or communication sequence cannot begin until the reset high time has expired.
- 5) Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within $1\mu\text{s}$ of this falling edge and will remain valid for $14\mu\text{s}$ minimum ($15\mu\text{s}$ total from falling edge on 1-Wire bus).
- 6) V_{IH} is a function of the external pullup resistor and the V_{CC} supply.
- 7) 30 nanocoulombs per 72 time slots @ 5.0V.
- 8) At $V_{CC} = 5.0\text{V}$ with a $5\text{k}\Omega$ pullup to V_{CC} and a maximum time slot of $120\mu\text{s}$.
- 9) Capacitance on the I/O pin could be 800pF when power is first applied. If a $5\text{k}\Omega$ resistor is used to pullup the I/O line to V_{CC} , $5\mu\text{s}$ after power has been applied the parasite capacitance will not affect normal communications.
- 10) The reset low time (t_{RSTL}) should be restricted to a maximum of $960\mu\text{s}$, to allow interrupt signaling, otherwise it could mask or conceal interrupt pulses if this device is used in parallel with a DS2404 or DS1994.
- 11) The optimal sampling point for the master is as close as possible to the end time of the t_{RDV} period without exceeding t_{RDV} . For the case of a Read-One Time slot, this maximizes the amount of time for the pullup resistor to recover to a high level. For a Read-Zero Time slot, it ensures that a read will occur before the fastest 1-Wire device(s) releases the line.
- 12) The duration of the low pulse sent by the master should be a minimum of $1\mu\text{s}$ with a maximum value as short as possible to allow time for the pullup resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write-One Time or before the master samples in the case of a Read-One Time.