74HC123; 74HCT123

Dual retriggerable monostable multivibrator with reset

Product data sheet

1. General description

The 74HC123; 74HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC123; 74HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{RD}$, which also inhibits the triggering.
3. An internal connection from $n\overline{RD}$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\overline{RD}$ as shown in the function table.

Schmitt-trigger action in the $n\overline{A}$ and nB inputs, makes the circuit highly tolerant to slower input rise and fall times.

The 74HC123; 74HCT123 is identical to the 74HC423; 74HCT423 but can be triggered via the reset input.

2. Features

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Schmitt-trigger action on all inputs except for the reset input
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

PHILIPS

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC123				
74HC123N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC123D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC123DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC123PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC123BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT123				
74HCT123N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT123D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT123DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT123PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	except for pins nREXT/CEXT; $V_O = -0.5$ V to (V_{CC} + 0.5 V)	-	±25	mA
I_{CC}	quiescent supply current		-	50	mA
I_{GND}	ground current		-	–50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation				
	DIP16 package	[1]	-	750	mW
	SO16 package	[2]	-	500	mW
	SSOP16 package	[3]	-	500	mW
	TSSOP16 package	[3]	-	500	mW
	DHVQFN16 package	[4]	-	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC123						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall time	n$\overline{RD}$ input				
		V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
T_{amb}	ambient temperature		–40	+25	+125	°C
74HCT123						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall time	n$\overline{RD}$ input; V_{CC} = 4.5 V	-	6.0	500	ns
T_{amb}	ambient temperature		–40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics 74HC123

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V

Table 6. Static characteristics 74HC123 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

Table 7. Static characteristics 74HCT123

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = –20 µA	4.4	4.5	-	V
		I_O = –4 mA	3.98	4.32	-	V

Table 7. Static characteristics 74HCT123 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ µA	-	0	0.1	V
		$I_O = 4.0$ mA	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pins n$\overline{A}$, nB	-	35	125	µA
		pin n$\overline{RD}$	-	50	180	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20$ µA	4.4	-	-	V
		$I_O = -4.0$ mA	3.84	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ µA	-	-	0.1	V
		$I_O = 4.0$ mA	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pins n$\overline{A}$, nB	-	-	160	µA
		pin n$\overline{RD}$	-	-	225	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = -20$ µA	4.4	-	-	V
		$I_O = -4$ mA	3.7	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V				
		$I_O = 20$ µA	-	-	0.1	V
		$I_O = 4.0$ mA	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160	µA

Table 7. Static characteristics 74HCT123 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V and other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V				
		pins $n\overline{A}$, nB	-	-	170	µA
		pin $n\overline{RD}$	-	-	245	µA

10. Dynamic characteristics

Table 8. Dynamic characteristics 74HC123

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.

For test circuit see Figure 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL}, t_{PLH}	propagation delay	$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$	$V_{CC} = 2.0$ V	-	83	255	ns
		$V_{CC} = 4.5$ V	-	30	51	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	26	-	ns
		$V_{CC} = 6.0$ V	-	24	43	ns
	$n\overline{RD}$ (reset) to nQ or $n\overline{Q}$	$V_{CC} = 2.0$ V	-	66	215	ns
		$V_{CC} = 4.5$ V	-	24	43	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	20	-	ns
		$V_{CC} = 6.0$ V	-	19	37	ns
t_{THL}, t_{TLH}	output transition time	see Figure 9				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
t_W	pulse width					
	$n\overline{A}$ LOW	see Figure 10				
		$V_{CC} = 2.0$ V	100	8	-	ns
		$V_{CC} = 4.5$ V	20	3	-	ns
		$V_{CC} = 6.0$ V	17	2	-	ns
	nB HIGH	see Figure 10				
		$V_{CC} = 2.0$ V	100	17	-	ns
		$V_{CC} = 4.5$ V	20	6	-	ns
		$V_{CC} = 6.0$ V	17	5	-	ns
	$n\overline{RD}$ LOW	see Figure 11				
		$V_{CC} = 2.0$ V	100	14	-	ns
		$V_{CC} = 4.5$ V	20	5	-	ns
		$V_{CC} = 6.0$ V	17	4	-	ns
	nQ HIGH and $n\overline{Q}$ LOW	$V_{CC} = 5.0$ V; see Figure 10 and 11 [1]				
		$C_{EXT} = 100$ nF; $R_{EXT} = 10$ kΩ	-	450	-	µs
		$C_{EXT} = 0$ pF; $R_{EXT} = 5$ kΩ	-	75	-	ns

Table 8. Dynamic characteristics 74HC123 *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.
For test circuit see Figure 12.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rt}	retrigger time n$\overline{A}$, nB	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; see Figure 10	[2][3]	-	110	-	ns
R_{EXT}	external timing resistor	see Figure 7					
		V_{CC} = 2.0 V		10	-	1000	kΩ
		V_{CC} = 5.0 V		2	-	1000	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 7	[3]		no limits		pF
C_{PD}	power dissipation capacitance	per monostable	[4][5]	-	54	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9					
	n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$	V_{CC} = 2.0 V		-	-	320	ns
		V_{CC} = 4.5 V		-	-	64	ns
		V_{CC} = 6.0 V		-	-	54	ns
	n$\overline{RD}$ (reset) to nQ or n$\overline{Q}$	V_{CC} = 2.0 V		-	-	270	ns
		V_{CC} = 4.5 V		-	-	54	ns
		V_{CC} = 6.0 V		-	-	46	ns
t_{THL}, t_{TLH}	output transition time	see Figure 9					
		V_{CC} = 2.0 V		-	-	95	ns
		V_{CC} = 4.5 V		-	-	19	ns
		V_{CC} = 6.0 V		-	-	16	ns
t_W	pulse width						
	n$\overline{A}$ LOW	see Figure 10					
		V_{CC} = 2.0 V		125	-	-	ns
		V_{CC} = 4.5 V		25	-	-	ns
		V_{CC} = 6.0 V		21	-	-	ns
	nB HIGH	see Figure 10					
		V_{CC} = 2.0 V		125	-	-	ns
		V_{CC} = 4.5 V		25	-	-	ns
		V_{CC} = 6.0 V		21	-	-	ns
	n$\overline{RD}$ LOW	see Figure 11					
		V_{CC} = 2.0 V		125	-	-	ns
		V_{CC} = 4.5 V		25	-	-	ns
		V_{CC} = 6.0 V		21	-	-	ns

Table 8. Dynamic characteristics 74HC123 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.
For test circuit see Figure 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9				
	n$\overline{RD}$, n$\overline{A}$, nB to nQ or n$\overline{Q}$	V_{CC} = 2.0 V	-	-	385	ns
		V_{CC} = 4.5 V	-	-	77	ns
		V_{CC} = 6.0 V	-	-	65	ns
	n$\overline{RD}$ (reset) to nQ or n$\overline{Q}$	V_{CC} = 2.0 V	-	-	325	ns
		V_{CC} = 4.5 V	-	-	65	ns
		V_{CC} = 6.0 V	-	-	55	ns
t_{THL}, t_{TLH}	output transition time	see Figure 9				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	pulse width					
	n$\overline{A}$ LOW	see Figure 10				
		V_{CC} = 2.0 V	150	-	-	ns
		V_{CC} = 4.5 V	30	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns
	nB HIGH	see Figure 10				
		V_{CC} = 2.0 V	150	-	-	ns
		V_{CC} = 4.5 V	30	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns
	n$\overline{RD}$ LOW	see Figure 11				
		V_{CC} = 2.0 V	150	-	-	ns
		V_{CC} = 4.5 V	30	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns

[1] For other R_{EXT} and C_{EXT} combinations see Figure 7. If C_{EXT} > 10 nF, the next formula is valid.
$t_W = K \times R_{EXT} \times C_{EXT}$, where:
t_W = typical output pulse width in ns;
R_{EXT} = external resistor in kΩ;
C_{EXT} = external capacitor in pF;
K = constant = 0.45 for V_{CC} = 5.0 V and 0.55 for V_{CC} = 2.0 V.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

[2] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT} >10 pF, the next formula (at V_{CC} = 5.0 V) for the setup time of a retrigger pulse is valid:
$t_{rt} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:
t_{rt} = retrigger time in ns;
C_{EXT} = external capacitor in pF;
R_{EXT} = external resistor in kΩ.
The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[3] When the device is powered-up, initiate the device via a reset pulse, when C_{EXT} < 50 pF.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

D = duty factor in %;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

C_{EXT} = timing capacitance in pF;

$\sum(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

[5] The condition is V_I = GND to V_{CC}.

Table 9. Dynamic characteristics 74HCT123

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.
For test circuit see Figure 12.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9					
	n$\overline{RD}$, n$\overline{A}$, nB to n$\overline{Q}$	V_{CC} = 4.5 V		-	30	51	ns
		V_{CC} = 5 V; C_L = 15 pF		-	26	-	ns
	n$\overline{RD}$ (reset) to nQ	V_{CC} = 4.5 V		-	27	46	ns
		V_{CC} = 5 V; C_L = 15 pF		-	23	-	ns
t_{PLH}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9					
	n$\overline{RD}$, n$\overline{A}$, nB to nQ	V_{CC} = 4.5 V		-	28	51	ns
		V_{CC} = 5 V; C_L = 15 pF		-	26	-	ns
	n$\overline{RD}$ (reset) to n$\overline{Q}$	V_{CC} = 4.5 V		-	23	46	ns
		V_{CC} = 5 V; C_L = 15 pF		-	23	-	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 9		-	7	15	ns
t_W	pulse width	V_{CC} = 4.5 V					
	n$\overline{A}$ LOW	see Figure 10		20	3	-	ns
	nB HIGH	see Figure 10		20	5	-	ns
	n$\overline{RD}$ LOW	see Figure 11		20	7	-	ns
	nQ HIGH and n$\overline{Q}$ LOW	V_{CC} = 5.0 V; see Figure 10 and 11	[1]				
		C_{EXT} = 100 nF; R_{EXT} = 10 kΩ		-	450	-	µs
		C_{EXT} = 0 pF; R_{EXT} = 5 kΩ		-	75	-	ns
t_{rt}	retrigger time n$\overline{A}$, nB	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; V_{CC} = 5.0 V; see Figure 10	[2][3]	-	110	-	ns
R_{EXT}	external timing resistor	V_{CC} = 5.0 V; see Figure 7		2	-	1000	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V; see Figure 7	[3]		no limits		pF
C_{PD}	power dissipation capacitance	per monostable	[4][5]	-	56	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9					
	n$\overline{RD}$, n$\overline{A}$, nB to n$\overline{Q}$	V_{CC} = 4.5 V		-	-	64	ns
	n$\overline{RD}$ (reset) to nQ	V_{CC} = 4.5 V		-	-	58	ns

Table 9. Dynamic characteristics 74HCT123 *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified.
For test circuit see Figure 12.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to nQ	V_{CC} = 4.5 V	-	-	64	ns
	$n\overline{RD}$ (reset) to $n\overline{Q}$	V_{CC} = 4.5 V	-	-	58	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V	-	-	19	ns
t_W	pulse width	V_{CC} = 4.5 V				
	$n\overline{A}$ LOW	see Figure 10	25	-	-	ns
	nB HIGH	see Figure 10	25	-	-	ns
	$n\overline{RD}$ LOW	see Figure 11	25	-	-	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to $n\overline{Q}$	V_{CC} = 4.5 V	-	-	77	ns
	$n\overline{RD}$ to nQ (reset)	V_{CC} = 4.5 V	-	-	69	ns
t_{PLH}	propagation delay	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; see Figure 9				
	$n\overline{RD}$, $n\overline{A}$, nB to nQ	V_{CC} = 4.5 V	-	-	77	ns
	$n\overline{RD}$ to $n\overline{Q}$ (reset)	V_{CC} = 4.5 V	-	-	69	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V	-	-	22	ns
t_W	pulse width	V_{CC} = 4.5 V				
	$n\overline{A}$ LOW	see Figure 10	30	-	-	ns
	nB HIGH	see Figure 10	30	-	-	ns
	$n\overline{RD}$ LOW	see Figure 11	30	-	-	ns

[1] For other R_{EXT} and C_{EXT} combinations see Figure 7. If C_{EXT} > 10 nF, the next formula is valid.

$t_W = K \times R_{EXT} \times C_{EXT}$, where:

t_W = typical output pulse width in ns;

R_{EXT} = external resistor in kΩ;

C_{EXT} = external capacitor in pF;

K = constant = 0.45 for V_{CC} = 5.0 V, see Figure 8.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7 pF.

[2] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT} >10 pF, the next formula (at V_{CC} = 5.0 V) for the setup time of a retrigger pulse is valid:

$t_{rt} = 30 + 0.19 \times R_{EXT} \times C_{EXT}^{0.9} + 13 \times R_{EXT}^{1.05}$, where:

t_{rt} = typical retrigger time in ns;

C_{EXT} = external capacitor in pF;

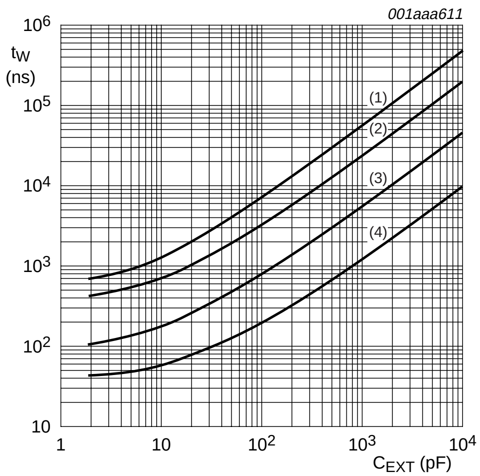
R_{EXT} = external resistor in kΩ.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7 pF.

[3] When the device is powered-up, initiate the device via a reset pulse, when C_{EXT} < 50 pF.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) + 0.75 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 16 \times V_{CC}$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
D = duty factor in %;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
C_{EXT} = timing capacitance in pF;
$\sum(C_L \times V_{CC}^2 \times f_o)$ sum of outputs.

[5] The condition is V_I = GND to V_{CC} – 1.5 V.



V_{CC} = 5.0 V; T_{amb} = 25 °C.

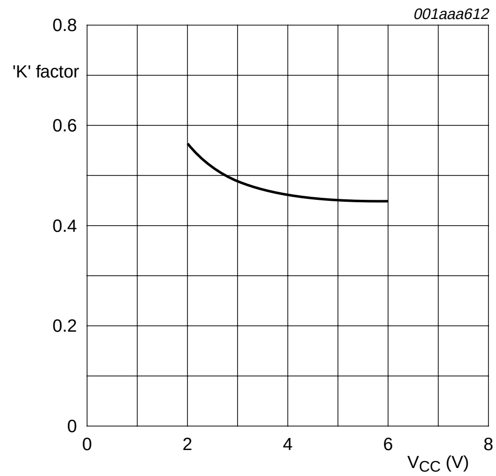
(1) R_{EXT} = 100 kΩ

(2) R_{EXT} = 50 kΩ

(3) R_{EXT} = 10 kΩ

(4) R_{EXT} = 2 kΩ

Fig 7. Typical output pulse width as a function of the external capacitor value

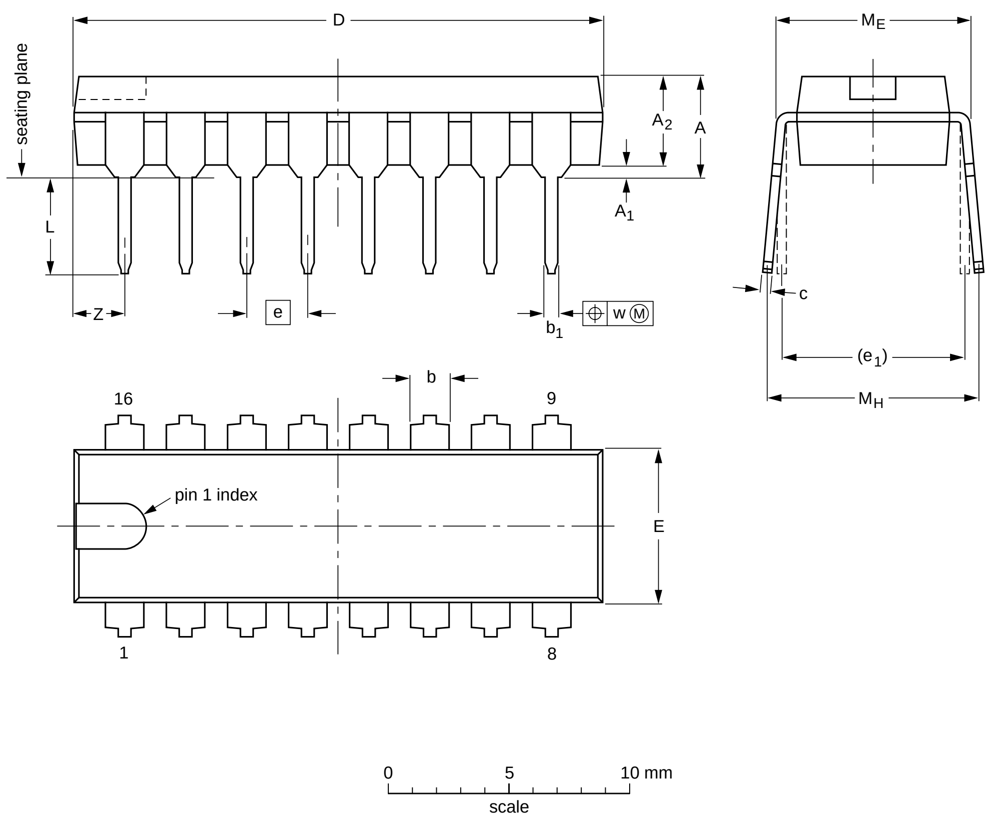


C_X = 10 nF; R_X = 10 kΩ to 100 kΩ

Fig 8. 74HCT123 typical 'K' factor as function of V_{CC}

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

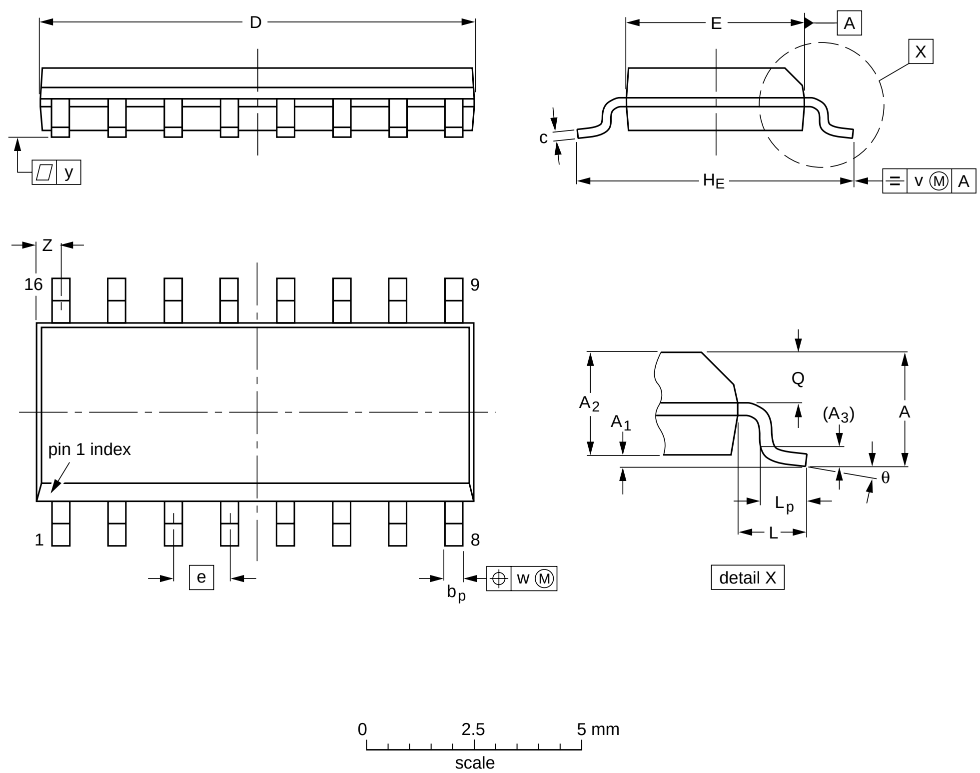
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			

Fig 16. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				

Fig 17. Package outline SOT109-1 (SO16)