

74HC573; 74HCT573

Octal D-type transparent latch; 3-state

Product data sheet

1. General description

The 74HC573; 74HCT573 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC573; 74HCT573 has octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state true outputs for bus oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all latches.

When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The 74HC573; 74HCT573 is functionally identical to:

- 74HC563; 74HCT563, but inverted outputs
- 74HC373; 74HCT373, but different pin arrangement

2. Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to 74HC563; 74HCT563 and 74HC373; 74HCT373
- Complies with JEDEC standard no. 7A
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-C exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

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3. Quick reference data

Table 1: Quick reference data
 $GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC573						
t_{PHL} , t_{PLH}	propagation delay	$V_{CC} = 5\text{ V}$; $C_L = 15\text{ pF}$				
	Dn to Qn		-	14	-	ns
	LE to Qn		-	15	-	ns
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	per latch; $V_I = GND\text{ to }V_{CC}$	[1]	26	-	pF
74HCT573						
t_{PHL} , t_{PLH}	propagation delay	$V_{CC} = 5\text{ V}$; $C_L = 15\text{ pF}$				
	Dn to Qn		-	17	-	ns
	LE to Qn		-	15	-	ns
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	per latch; $V_I = GND\text{ to } (V_{CC} - 1.5\text{ V})$	[1]	26	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC573				
74HC573N	-40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HC573D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC573DB	-40 °C to +125 °C	SSOP20	plastic small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC573PW	-40 °C to +125 °C	TSSOP20	plastic small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC573BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

Table 3: Pin description ...continued

Symbol	Pin	Description
Q4	15	3-state latch output 4
Q3	16	3-state latch output 3
Q2	17	3-state latch output 2
Q1	18	3-state latch output 1
Q0	19	3-state latch output 0
V _{CC}	20	supply voltage

7. Functional description

Table 4: Function table [1]

Operating mode	Control		Input	Internal latches	Output
	OE	LE	D _n		Q _n
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±35	mA
I _{CC}	quiescent supply current		-	70	mA
I _{GND}	ground current		-	-70	mA
T _{stg}	storage temperature		-65	+150	°C

Table 5: Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
P _{tot}	total power dissipation					
	DIP20 package		[1]	-	750	mW
	SO20 package		[2]	-	500	mW
	SSOP20 package		[3]	-	500	mW
	TSSOP20 package		[3]	-	500	mW
	DHSVFN20 package		[4]	-	500	mW

[1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C

[4] For DHSVFN20 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC573						
V _{CC}	supply voltage		2.0	5.0	6.0	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
t _r , t _f	input rise and fall time	V _{CC} = 2.0 V	-	-	1000	ns
		V _{CC} = 4.5 V	-	6.0	500	ns
		V _{CC} = 6.0 V	-	-	400	ns
74HCT573						
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
t _r , t _f	input rise and fall time	V _{CC} = 4.5 V	-	6.0	500	ns

10. Static characteristics

Table 7: Static characteristics 74HC573
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}	-	-	-	
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -6.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
		$I_O = -7.8\text{ mA}$; $V_{CC} = 6\text{ V}$	5.48	5.81	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}	-	-	-	
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	V
		$I_O = 6.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	V
		$I_O = 7.8\text{ mA}$; $V_{CC} = 6\text{ V}$	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6\text{ V}$	-	-	± 0.1	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	-	-	± 0.5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	8.0	μA
C_i	input capacitance		-	3.5	-	pF
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	-	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}	-	-	-	
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	-	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	-	-	V
		$I_O = -6.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.84	-	-	V
		$I_O = -7.8\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.34	-	-	V

Table 7: Static characteristics 74HC573 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 7.8 mA; V _{CC} = 6 V	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6 V	-	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	-	±5.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	80	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.2	-	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	-	±10.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	160	μA

Table 8: Static characteristics 74HCT573

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V

Table 8: Static characteristics 74HCT573 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
T_{amb} = -40 °C to +125 °C							
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V	
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V	
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V					
		I _O = -20 µA	4.4	-	-	V	
		I _O = -6.0 mA	3.7	-	-	V	
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V					
		I _O = 20 µA	-	-	0.1	V	
		I _O = 6.0 mA	-	-	0.4	V	
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	µA	
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND per input pin; other inputs at GND or V _{CC} ; I _O = 0 A; V _{CC} = 5.5 V	-	-	±10.0	µA	
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	160	µA	
ΔI _{CC}	additional quiescent supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V					
			Dn	-	-	172	µA
			LE	-	-	319	µA
			$\overline{\text{OE}}$	-	-	613	µA

11. Dynamic characteristics

Table 9: Dynamic characteristics 74HC573Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t _{PHL} , t _{PLH}	propagation delay Dn to Qn	see Figure 7				
		V _{CC} = 2.0 V	-	47	150	ns
		V _{CC} = 4.5 V	-	17	30	ns
		V _{CC} = 5 V; C _L = 15 pF	-	14	-	ns
		V _{CC} = 6.0 V	-	14	26	ns
t _{PHL} , t _{PLH}	propagation delay LE to Qn	see Figure 8				
		V _{CC} = 2.0 V	-	50	150	ns
		V _{CC} = 4.5 V	-	18	30	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	ns
		V _{CC} = 6.0 V	-	14	26	ns
t _{PZH} , t _{PZL}	3-state output enable time $\overline{\text{OE}}$ to Qn	see Figure 9				
		V _{CC} = 2.0 V	-	44	140	ns
		V _{CC} = 4.5 V	-	16	28	ns
		V _{CC} = 6.0 V	-	13	24	ns

Table 9: Dynamic characteristics 74HC573 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ} , t_{PLZ}	3-state output disable time \overline{OE} to Qn	see Figure 9				
		$V_{CC} = 2.0$ V	-	55	150	ns
		$V_{CC} = 4.5$ V	-	20	30	ns
		$V_{CC} = 6.0$ V	-	16	26	ns
t_{THL} , t_{TLH}	output transition time	see Figure 7				
		$V_{CC} = 2.0$ V	-	14	60	ns
		$V_{CC} = 4.5$ V	-	5	12	ns
		$V_{CC} = 6.0$ V	-	4	10	ns
t_W	pulse width LE HIGH	see Figure 8				
		$V_{CC} = 2.0$ V	80	14	-	ns
		$V_{CC} = 4.5$ V	16	5	-	ns
		$V_{CC} = 6.0$ V	14	4	-	ns
t_{su}	set-up time Dn to LE	see Figure 10				
		$V_{CC} = 2.0$ V	50	11	-	ns
		$V_{CC} = 4.5$ V	10	4	-	ns
		$V_{CC} = 6.0$ V	9	3	-	ns
t_h	hold time Dn to LE	see Figure 10				
		$V_{CC} = 2.0$ V	5	3	-	ns
		$V_{CC} = 4.5$ V	5	1	-	ns
		$V_{CC} = 6.0$ V	5	1	-	ns
C_{PD}	power dissipation capacitance	per latch; $V_I = \text{GND to } V_{CC}$	[1]	-	26	pF
$T_{amb} = -40$ to $+85$ °C						
t_{PHL} , t_{PLH}	propagation delay Dn to Qn	see Figure 7				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns
t_{PHL} , t_{PLH}	propagation delay LE to Qn	see Figure 8				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns
t_{PZH} , t_{PZL}	3-state output enable time \overline{OE} to Qn	see Figure 9				
		$V_{CC} = 2.0$ V	-	-	175	ns
		$V_{CC} = 4.5$ V	-	-	35	ns
		$V_{CC} = 6.0$ V	-	-	30	ns
t_{PHZ} , t_{PLZ}	3-state output disable time \overline{OE} to Qn	see Figure 9				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns

Table 9: Dynamic characteristics 74HC573 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{THL} , t_{TLH}	output transition time	see Figure 7				
		$V_{CC} = 2.0$ V	-	-	75	ns
		$V_{CC} = 4.5$ V	-	-	15	ns
		$V_{CC} = 6.0$ V	-	-	13	ns
t_W	pulse width LE HIGH	see Figure 8				
		$V_{CC} = 2.0$ V	100	-	-	ns
		$V_{CC} = 4.5$ V	20	-	-	ns
		$V_{CC} = 6.0$ V	17	-	-	ns
t_{su}	set-up time Dn to LE	see Figure 10				
		$V_{CC} = 2.0$ V	65	-	-	ns
		$V_{CC} = 4.5$ V	13	-	-	ns
		$V_{CC} = 6.0$ V	11	-	-	ns
t_h	hold time Dn to LE	see Figure 10				
		$V_{CC} = 2.0$ V	5	-	-	ns
		$V_{CC} = 4.5$ V	5	-	-	ns
		$V_{CC} = 6.0$ V	5	-	-	ns
$T_{amb} = -40$ to $+125$ °C						
t_{PHL} , t_{PLH}	propagation delay Dn to Qn	see Figure 7				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
t_{PHL} , t_{PLH}	propagation delay LE to Qn	see Figure 8				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
t_{PZH} , t_{PZL}	3-state output enable time \overline{OE} to Qn	see Figure 9				
		$V_{CC} = 2.0$ V	-	-	210	ns
		$V_{CC} = 4.5$ V	-	-	42	ns
		$V_{CC} = 6.0$ V	-	-	36	ns
t_{PHZ} , t_{PLZ}	3-state output disable time \overline{OE} to Qn	see Figure 9				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
t_{THL} , t_{TLH}	output transition time	see Figure 7				
		$V_{CC} = 2.0$ V	-	-	90	ns
		$V_{CC} = 4.5$ V	-	-	18	ns
		$V_{CC} = 6.0$ V	-	-	15	ns

Table 9: Dynamic characteristics 74HC573 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width LE HIGH	see Figure 8				
		$V_{CC} = 2.0$ V	120	-	-	ns
		$V_{CC} = 4.5$ V	24	-	-	ns
t_{su}	set-up time Dn to LE	see Figure 10				
		$V_{CC} = 2.0$ V	75	-	-	ns
		$V_{CC} = 4.5$ V	15	-	-	ns
t_h	hold time Dn to LE	see Figure 10				
		$V_{CC} = 2.0$ V	5	-	-	ns
		$V_{CC} = 4.5$ V	5	-	-	ns
		$V_{CC} = 6.0$ V	5	-	-	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 10: Dynamic characteristics 74HCT573

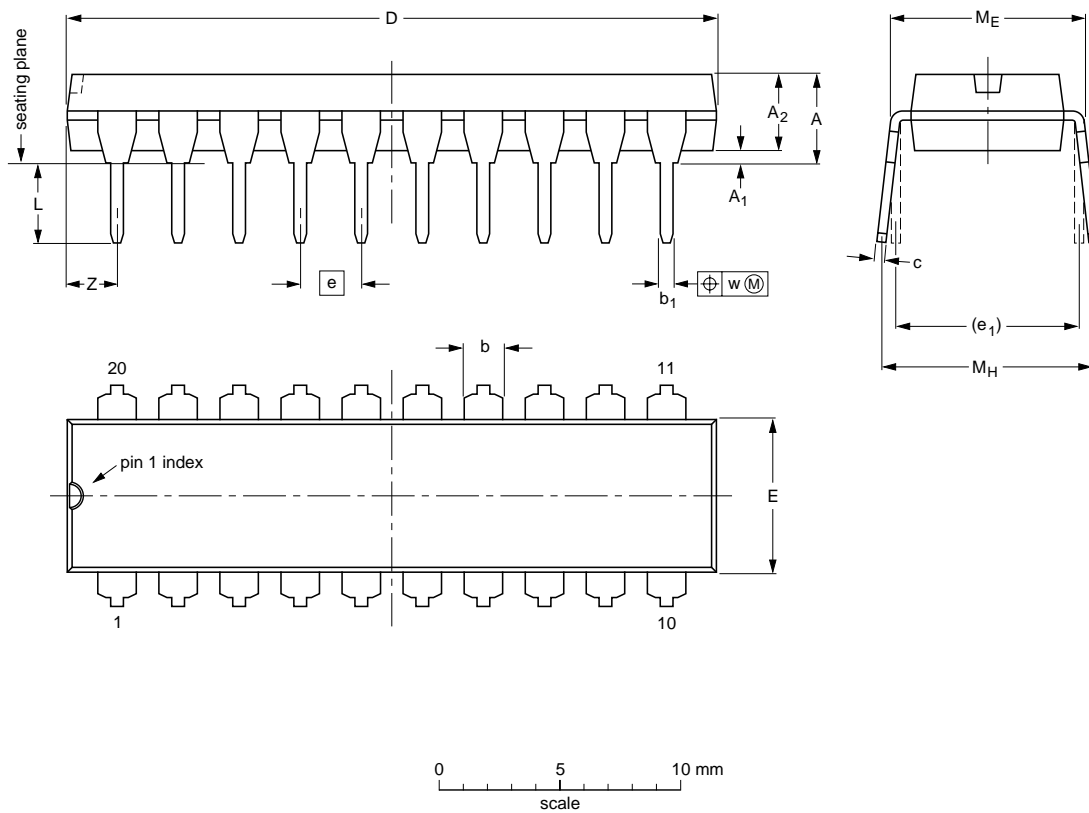
Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL} , t_{PLH}	propagation delay Dn to Qn	see Figure 7				
		$V_{CC} = 4.5$ V	-	20	35	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	ns
t_{PHL} , t_{PLH}	propagation delay LE to Qn	see Figure 8				
		$V_{CC} = 4.5$ V	-	18	35	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	ns
t_{PZH} , t_{PZL}	3-state output enable time \overline{OE} to Qn	$V_{CC} = 4.5$ V; see Figure 9	-	17	30	ns
t_{PHZ} , t_{PLZ}	3-state output disable time \overline{OE} to Qn	$V_{CC} = 4.5$ V; see Figure 9	-	18	30	ns
t_{THL} , t_{TLH}	output transition time	$V_{CC} = 4.5$ V; see Figure 7	-	5	12	ns
t_W	pulse width LE HIGH	$V_{CC} = 4.5$ V; see Figure 8	16	5	-	ns
t_{su}	set-up time Dn to LE	$V_{CC} = 4.5$ V; see Figure 10	13	7	-	ns
t_h	hold time Dn to LE	$V_{CC} = 4.5$ V; see Figure 10	9	4	-	ns
C_{PD}	power dissipation capacitance	per latch; $V_1 = \text{GND to } (V_{CC} - 1.5 \text{ V})$	[1] -	26	-	pF

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

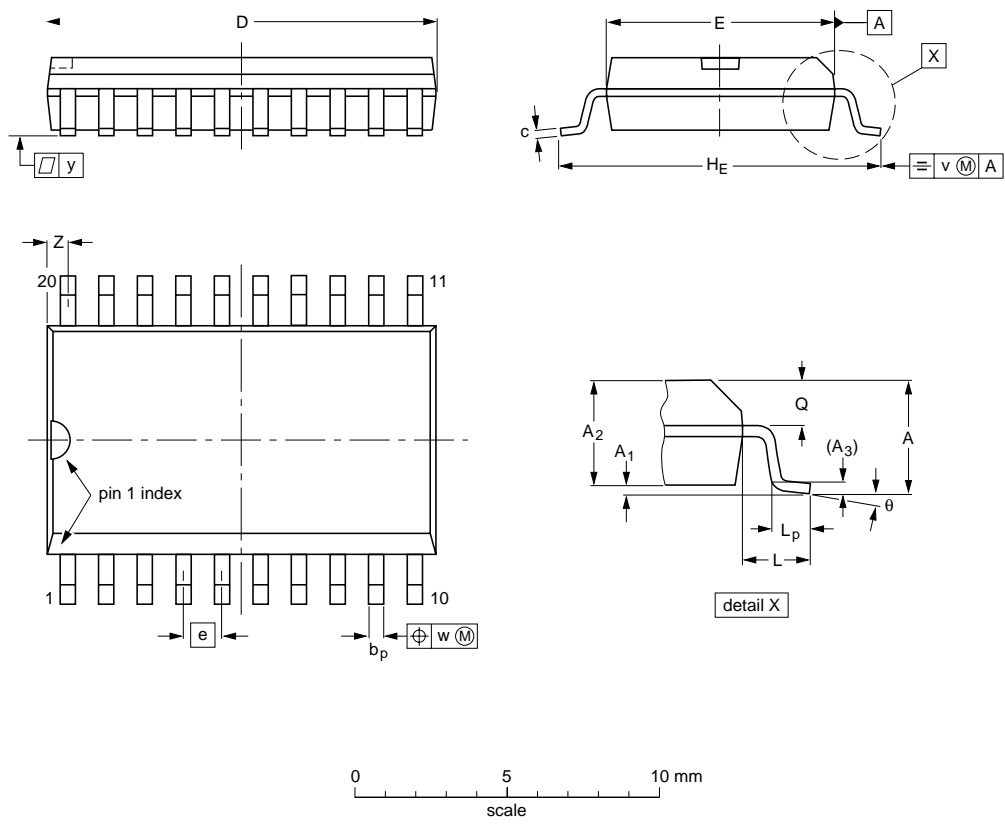
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT146-1		MS-001	SC-603	

Fig 12. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT163-1	075E04	MS-013		

Fig 13. Package outline SOT163-1 (SO20)