5 Volt, Byte Alterable EEPROM

FEATURES

- **70ns access time**
- **Simple byte and page write**
  - **—Single 5V supply**
  - **—No external high voltages or V_{PP} control circuits**
  - **—Self-timed**
  - **—No erase before write**
  - **—No complex programming algorithms**
  - **—No overerase problem**
- **Low power CMOS**
  - **—40mA active current max.**
  - **—200µA standby current max.**
- **Fast write cycle times**
  - **—64-byte page write operation**
  - **—Byte or page write cycle: 2ms typical**
  - **—Complete memory rewrite: 0.25 sec. typical**
  - **—Effective byte write cycle time: 32µs typical**
- **Software data protection**
- **End of write detection**
  - **—DATA polling**
  - **—Toggle bit**
- **High reliability**
  - **—Endurance: 1 million cycles**
  - **—Data retention: 100 years**
- **JEDEC approved byte-wide pin out**
- **Pb-free plus anneal available (RoHS compliant)**

DESCRIPTION

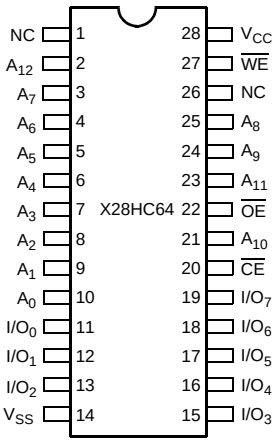
The X28HC64 is an 8K x 8 EEPROM, fabricated with Intersil's proprietary, high performance, floating gate CMOS technology. Like all Intersil programmable non-volatile memories, the X28HC64 is a 5V only device. It features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28HC64 supports a 64-byte page write operation, effectively providing a 32µs/byte write cycle, and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features DATA Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Intersil's hardware write protect capability.

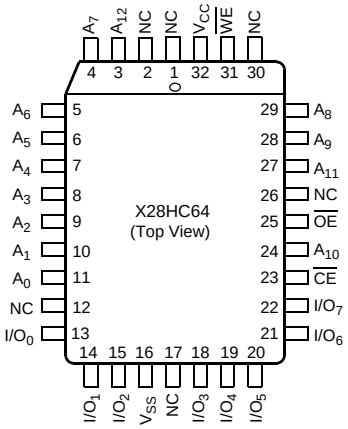
Intersil EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN CONFIGURATIONS

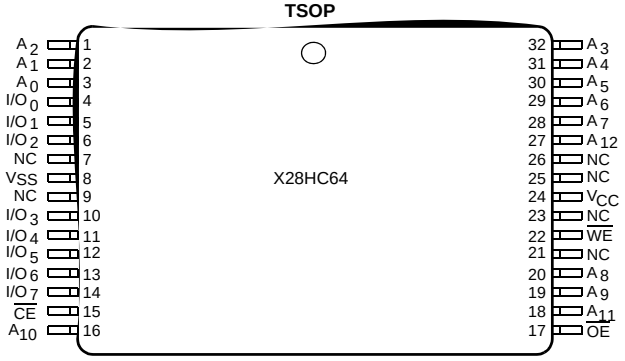
Plastic DIP, Flat Pack, CERDIP, SOIC



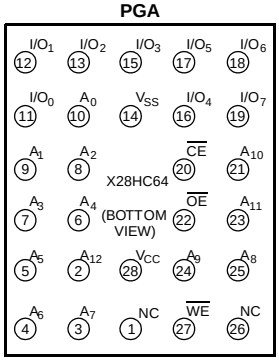
LCC, PLCC



TSOP



PGA



Bottom View

Ordering Information

PART NUMBER	PART MARKING	TEMPERATURE RANGE (°C)	ACCESS TIME (ns)	PACKAGE	PKG. DWG. #
X28HC64EM-70	X28HC64EM-70	-55 to 125	70	32 Ld LCC (458 mil)	
X28HC64J-70*	X28HC64J-70	0 to 70		32 Ld PLCC	N32.45x55
X28HC64JI-70*	X28HC64JI-70	-40 to 85		32 Ld PLCC	N32.45x55
X28HC64JIZ-70* (Note)	X28HC64JI-70 Z	-40 to 85		32 Ld PLCC (Pb-free)	N32.45x55
X28HC64JZ-70* (Note)	X28HC64J-70 Z	0 to 70		32 Ld PLCC (Pb-free)	N32.45x55
X28HC64KM-70	X28HC64KM-70	-55 to 125		28 Ld PGA	G28.550x650A
X28HC64P-70	X28HC64P-70	0 to 70		28 Ld PDIP	E28.6
X28HC64PZ-70 (Note)	X28HC64P-70 Z	0 to 70		28 Ld PDIP** (Pb-free)	E28.6
X28HC64S-70*	X28HC64S-70	0 to 70		28 Ld SOIC (300 mil)	M28.3
X28HC64SI-70*	X28HC64SI-70	-40 to 85		28 Ld SOIC (300 mil)	M28.3
X28HC64SM-70*	X28HC64SM-70	-55 to 125		28 Ld SOIC (300 mil)	M28.3
X28HC64SZ-70 (Note)	X28HC64S-70 Z	0 to 70		28 Ld SOIC (300 mil) (Pb-free)	M28.3
X28HC64J-90*	X28HC64J-90	0 to 70	90	32 Ld PLCC	N32.45x55
X28HC64JI-90*	X28HC64JI-90	-40 to 85		32 Ld PLCC	N32.45x55
X28HC64JIZ-90* (Note)	X28HC64JI-90 Z	-40 to 85		32 Ld PLCC (Pb-free)	N32.45x55
X28HC64KM-90	X28HC64KM-90	-55 to 125		28 Ld PGA	G28.550x650A
X28HC64KMB-90	C X28HC64KMB-90	MIL-STD-883		28 Ld PGA	G28.550x650A
X28HC64P-90	X28HC64P-90	0 to 70		28 Ld PDIP	E28.6
X28HC64PI-90	X28HC64PI-90	-40 to 85		28 Ld PDIP	E28.6
X28HC64PIZ-90 (Note)	X28HC64PI-90 Z	-40 to 85		28 Ld PDIP** (Pb-free)	E28.6
X28HC64PZ-90 (Note)	X28HC64P-90 Z	0 to 70		28 Ld PDIP** (Pb-free)	E28.6
X28HC64S-90*	X28HC64S-90	0 to 70		28 Ld SOIC (300 mil)	M28.3

Ordering Information (Continued)

PART NUMBER	PART MARKING	TEMPERATURE RANGE (°C)	ACCESS TIME (ns)	PACKAGE	PKG. DWG. #
X28HC64D-12	X28HC64D-12	0 to 70	120	28 Ld CERDIP	
X28HC64DI-12	X28HC64DI-12	-40 to 85		28 Ld CERDIP	
X28HC64DM-12	X28HC64DM-12	-55 to 125		28 Ld CERDIP	
X28HC64DMB-12	C X28HC64DMB-12	MIL-STD-883		28 Ld CERDIP	
X28HC64FM-12	X28HC64FM-12	-55 to 125		28 Ld FLATPACK (440 mil)	
X28HC64J-12*	X28HC64J-12	0 to 70		32 Ld PLCC	N32.45x55
X28HC64JI-12*	X28HC64JI-12	-40 to 85		32 Ld PLCC	N32.45x55
X28HC64JIZ-12* (Note)	X28HC64JI-12 Z	-40 to 85		32 Ld PLCC (Pb-free)	N32.45x55
X28HC64JZ-12* (Note)	X28HC64J-12 Z	0 to 70		32 Ld PLCC (Pb-free)	N32.45x55
X28HC64KMB-12	C X28HC64KMB-12	MIL-STD-883		28 Ld PGA	G28.550x650A
X28HC64P-12	X28HC64P-12	0 to 70		28 Ld PDIP	E28.6
X28HC64PI-12	X28HC64PI-12	-40 to 85		28 Ld PDIP	E28.6
X28HC64PIZ-12 (Note)	X28HC64PI-12 Z	-40 to 85		28 Ld PDIP** (Pb-free)	E28.6
X28HC64PZ-12 (Note)	X28HC64P-12 Z	0 to 70		28 Ld PDIP** (Pb-free)	E28.6
X28HC64S-12*	X28HC64S-12	0 to 70		28 Ld SOIC (300 mil)	M28.3
X28HC64SI-12*	X28HC64SI-12	-40 to 85		28 Ld SOIC (300 mil)	M28.3
X28HC64SIZ-12* (Note)	X28HC64SI-12 Z	-40 to 85		28 Ld SOIC (300 mil) (Pb-free)	M28.3
X28HC64SZ-12 (Note)	X28HC64S-12 Z	0 to 70		28 Ld SOIC (300 mil) (Pb-free)	M28.3
X28HC64DM-15	X28HC64DM-15	-55 to 125	150	28 Ld CERDIP	
X28HC64J-15T1	X28HC64J-15	0 to 70		32 Ld PLCC Tape and Reel	N32.45x55
X28HC64JI-15	X28HC64JI-15	-40 to 85		32 Ld PLCC	N32.45x55
X28HC64JM-15	X28HC64JM-15	-55 to 125		32 Ld PLCC	N32.45x55
X28HC64JZ-15* (Note)	X28HC64J-15 Z	0 to 70		32 Ld PLCC (Pb-free)	N32.45x55
X28HC64KMB-15	C X28HC64KMB-15	MIL-STD-883		28 Ld PGA	G28.550x650A
X28HC64P-15	X28HC64P-15	0 to 70		28 Ld PDIP	E28.6
X28HC64PIZ-15 (Note)	X28HC64PI-15 Z	-40 to 85		28 Ld PDIP** (Pb-free)	E28.6
X28HC64PZ-15 (Note)	X28HC64P-15 Z	0 to 70		28 Ld PDIP** (Pb-free)	E28.6
X28HC64S-15	X28HC64S-15	0 to 70		28 Ld SOIC (300 mil)	M28.3
X28HC64SI-15	X28HC64SI-15	-40 to 85		28 Ld SOIC (300 mil)	M28.3

*Add "T1" suffix for tape and reel.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias
X28HC64 ..... -10°C to +85°C
X28HC64I, X28HC64M ..... -65°C to +135°C
Storage temperature..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1V to +7V
D.C. output current 5mA
Lead temperature
(soldering, 10 seconds)..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

Supply Voltage	Limits
X28HC64	5V ±10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} current (active) (TTL inputs)		15	40	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O’s = open, address inputs = TTL levels @ f = 10 MHz
I_{SB1}	V_{CC} current (standby) (TTL inputs)		1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O’s = open, other inputs = V_{IH}
I_{SB2}	V_{CC} current (standby) (CMOS inputs)		100	200	µA	$\overline{CE}$ = V_{CC} - 0.3V, $\overline{OE}$ = GND, All I/O’s = open, other inputs = V_{CC} - 0.3V
I_{LI}	Input leakage current			±10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			±10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW voltage	-1		0.8	V	
V_{IH}(2)	Input HIGH voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 5mA
V_{OH}	Output HIGH voltage	2.4			V	I_{OH} = -5mA

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum endurance	100,000		Cycles
Data retention	100		Years

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Unit
t_{PUR}(3)	Power-up to read operation	100	µs
t_{PUW}(3)	Power-up to write operation	5	ms

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}$(3)	Input/output capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

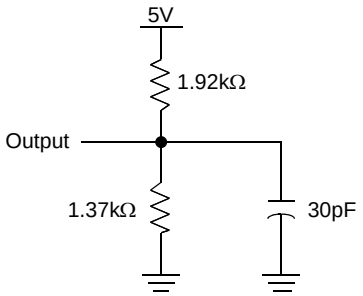
Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and write inhibit	High Z	Standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



SYMBOL TABLE

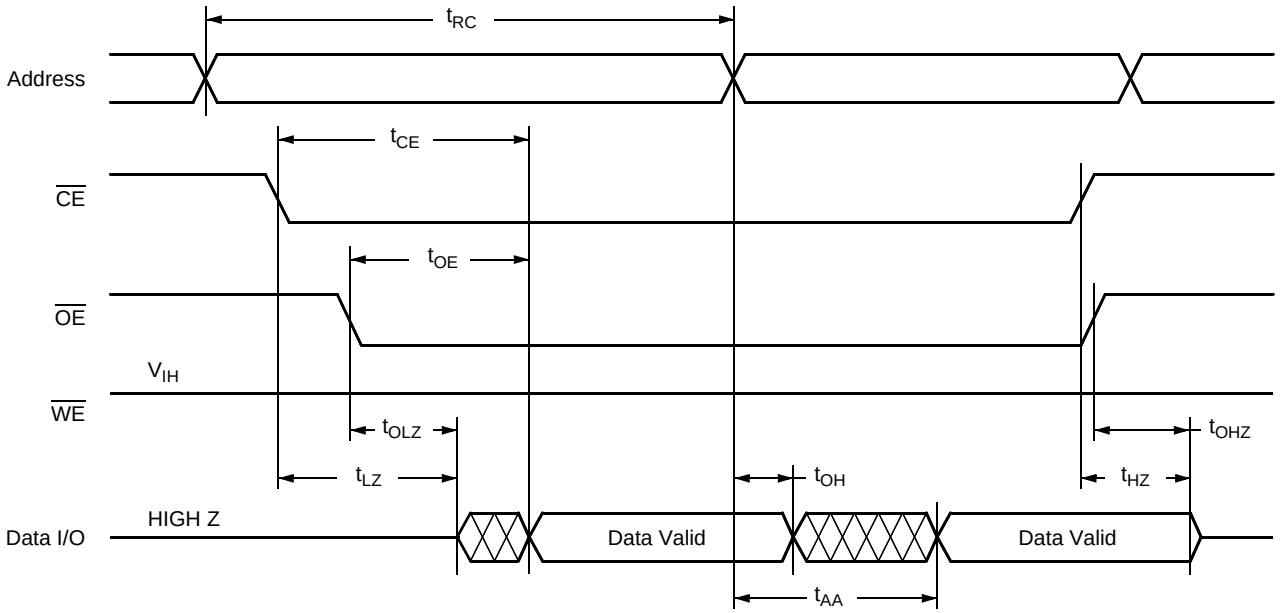
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HC64-70		X28HC64-90		X28HC64-12		Unit
		-55°C to +125°C		-55°C to +125°C		-55°C to +125°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	70		90		120		ns
t_{CE}	Chip enable access time		70		90		120	ns
t_{AA}	Address access time		70		90		120	ns
t_{OE}	Output enable access time		35		40		50	ns
t_{LZ}(4)	$\overline{CE}$ LOW to active output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to active output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to high Z output		30		30		30	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to high Z output		30		30		30	ns
t_{OH}	Output hold from address change	0		0		0		ns

Read Cycle

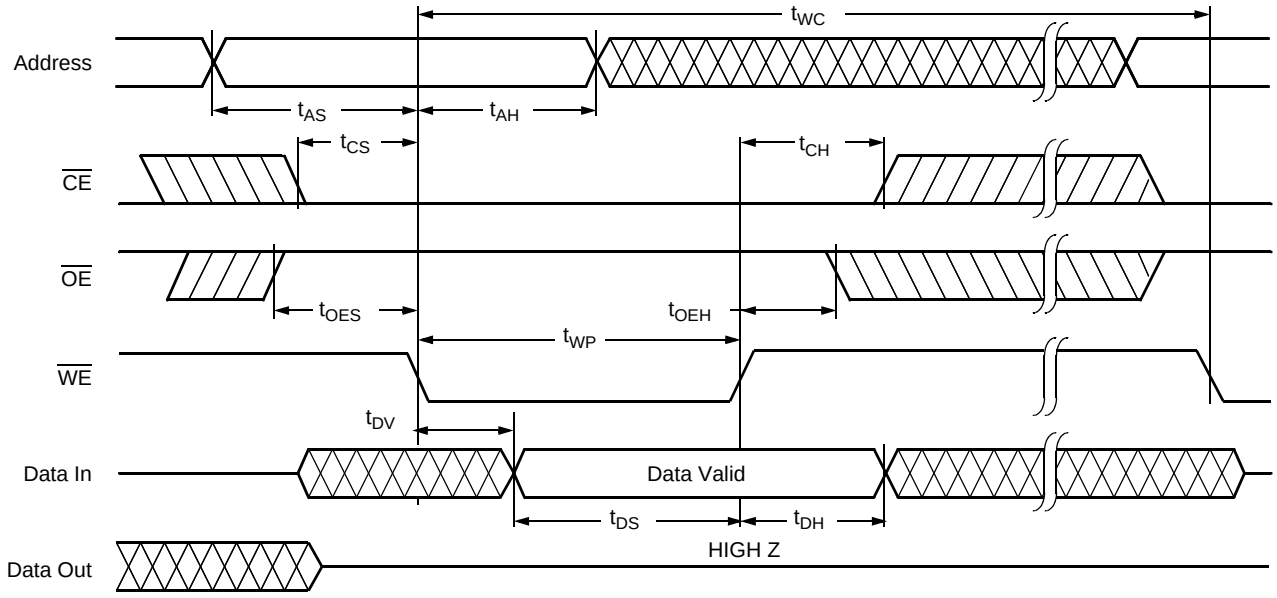


Note: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC}(5)	Write cycle time		2	5	ms
t_{AS}	Address setup time	0			ns
t_{AH}	Address hold time	50			ns
t_{CS}	Write setup time	0			ns
t_{CH}	Write hold time	0			ns
t_{CW}	$\overline{CE}$ pulse width	50			ns
t_{OES}	$\overline{OE}$ High setup time	0			ns
t_{OEH}	$\overline{OE}$ High hold time	0			ns
t_{WP}	$\overline{WE}$ pulse width	50			ns
t_{WPH}(6)	$\overline{WE}$ HIGH recovery	50			ns
t_{DV}(6)	Data valid			1	µs
t_{DS}	Data setup	50			ns
t_{DH}	Data hold	0			ns
t_{DW}(6)	Delay to next write	10			µs
t_{BLC}	Byte load cycle	0.15		100	µs

$\overline{WE}$ Controlled Write Cycle



Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

(6) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.