GAL22V10

High Performance E²CMOS PLD Generic Array Logic™

Lead-Free Package Options Available!

Features

- HIGH PERFORMANCE E²CMOS® TECHNOLOGY
  - 4 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3.5 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- ACTIVE PULL-UPS ON ALL PINS
- COMPATIBLE WITH STANDARD 22V10 DEVICES
  - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices
- 50% to 75% REDUCTION IN POWER VERSUS BIPOLAR
  - 90mA Typical Icc on Low Power Device
  - 45mA Typical Icc on Quarter Power Device
- E² CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- TEN OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
- PRELOAD AND POWER-ON RESET OF REGISTERS
  - 100% Functional Testability
- APPLICATIONS INCLUDE:
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- ELECTRONIC SIGNATURE FOR IDENTIFICATION
- LEAD-FREE PACKAGE OPTIONS

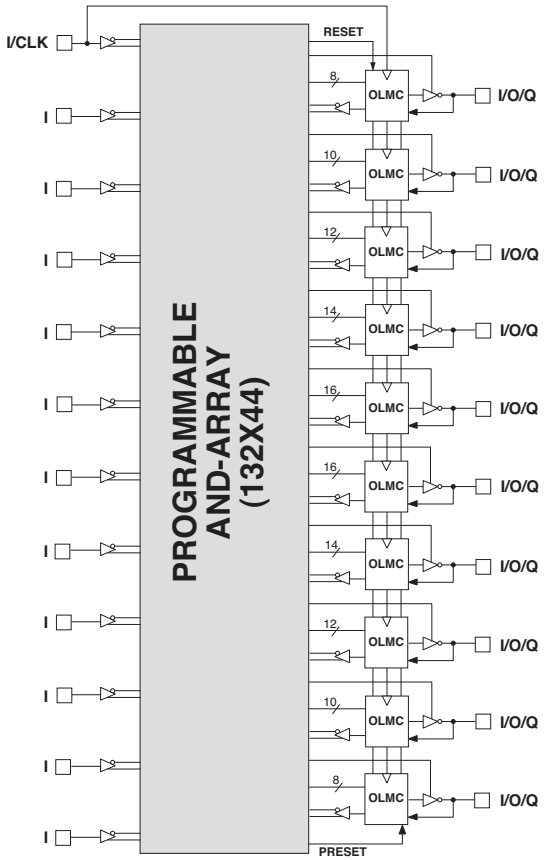
Description

The GAL22V10, at 4ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

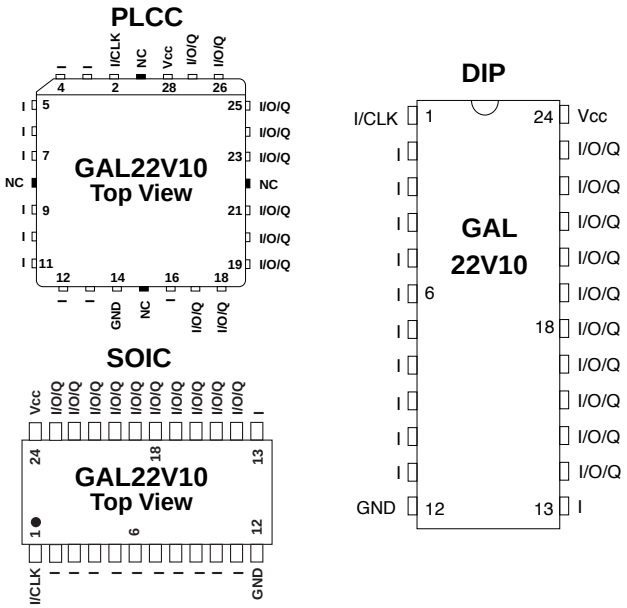
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram



Pin Configuration



Select devices have been discontinued. See Ordering Information section for product status.

LATTICE SEMICONDUCTOR CORP

Lead-Free Packaging
Commercial Grade Specifications

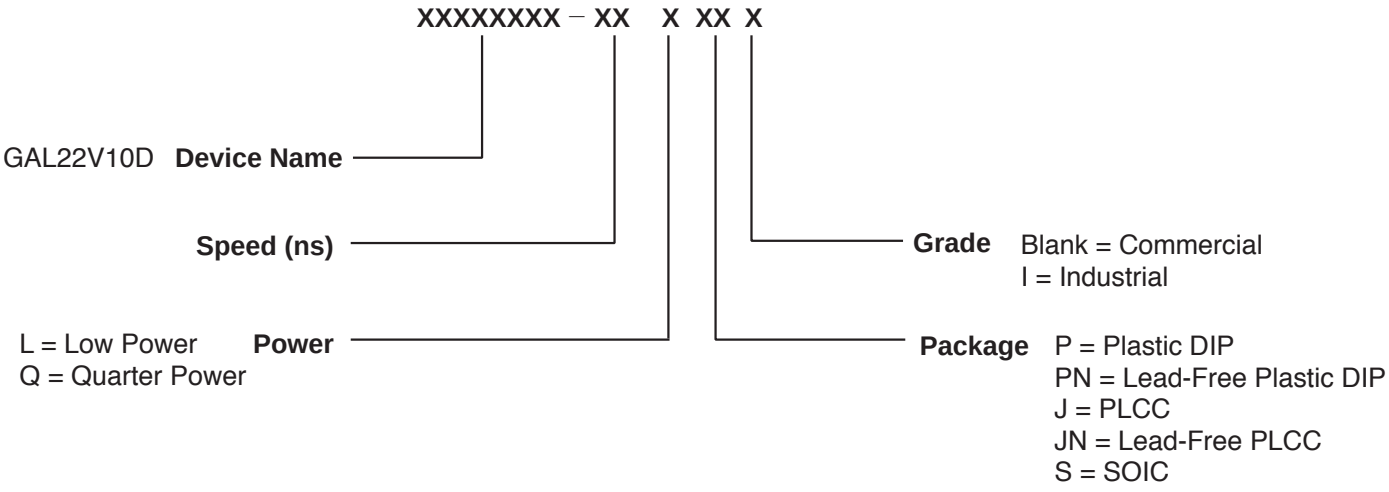
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
4	2.5	3.5	140	GAL22V10D-4LJN	Lead-Free 28-Lead PLCC
5	3	4	140	GAL22V10D-5LJN	Lead-Free 28-Lead PLCC
7.5	4.5	4.5	140	GAL22V10D-7LPN	Lead-Free 24-Pin Plastic DIP
	4.5	4.5	140	GAL22V10D-7LJN	Lead-Free 28-Lead PLCC
10	7	7	55	GAL22V10D-10QPN	Lead-Free 24-Pin Plastic DIP
			55	GAL22V10D-10QJN	Lead-Free 28-Lead PLCC
			130	GAL22V10D-10LPN	Lead-Free 24-Pin Plastic DIP
			130	GAL22V10D-10LJN	Lead-Free 28-Lead PLCC
15	10	8	55	GAL22V10D-15QPN	Lead-Free 24-Pin Plastic DIP
			55	GAL22V10D-15QJN	Lead-Free 28-Lead PLCC
			90	GAL22V10D-15LPN	Lead-Free 24-Pin Plastic DIP
			90	GAL22V10D-15LJN	Lead-Free 28-Lead PLCC
25	15	15	55	GAL22V10D-25QPN	Lead-Free 24-Pin Plastic DIP
			55	GAL22V10D-25QJN	Lead-Free 28-Lead PLCC
			90	GAL22V10D-25LPN	Lead-Free 24-Pin Plastic Dip
			90	GAL22V10D-25LJN	Lead-Free 28-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	5	4.5	160	GAL22V10D-7LPNI	Lead-Free 24-Pin Plastic DIP
	4.5	4.5	160	GAL22V10D-7LJNI	Lead-Free 28-Lead PLCC
10	7	7	160	GAL22V10D-10LPNI	Lead-Free 24-Pin Plastic DIP
			160	GAL22V10D-10LJNI	Lead-Free 28-Lead PLCC
15	10	8	130	GAL22V10D-15LPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL22V10D-15LJNI	Lead-Free 28-Lead PLCC
20	14	10	130	GAL22V10D-20LPNI	Lead-Free 24-Pin Plastic DIP
			130	GAL22V10D-20LJNI	Lead-Free 28-Lead PLCC
25	15	15	130	GAL22V10D-25LPNI	Lead-Free 24-Pin Plastic Dip
			130	GAL22V10D-25LJNI	Lead-Free 28-Lead PLCC

Select devices have been discontinued.
See Ordering Information section for product status.

Part Number Description



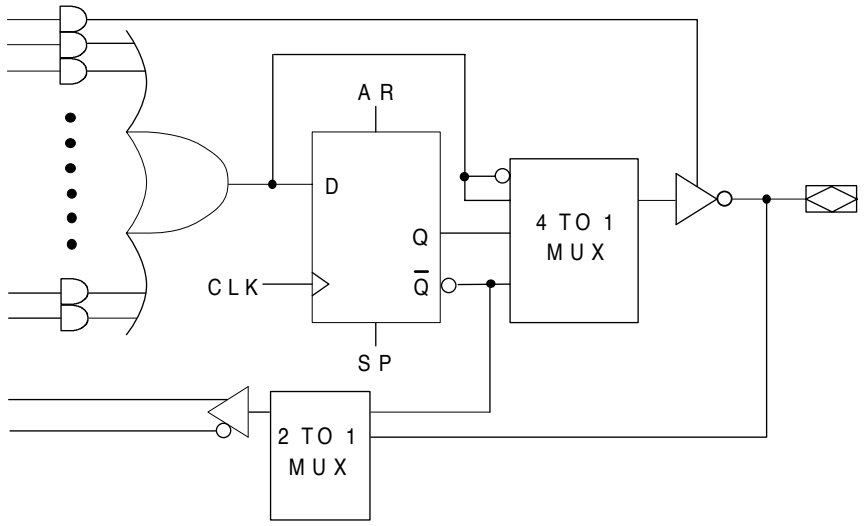
Output Logic Macrocell (OLMC)

The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23, DIP pinout), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10 has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

Output Logic Macrocell Configurations

Each of the Macrocells of the GAL22V10 has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

REGISTERED

In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

Absolute Maximum Ratings[1]

Supply voltage V_{CC} ..... -0.5 to +7V

Input voltage applied ..... -2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... -2.5 to V_{CC} +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to +75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... -40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage			Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage			2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)		—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$		—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}		—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}		2.4	—	—	V
I_{OL}	Low Level Output Current			—	—	16	mA
I_{OH}	High Level Output Current			—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C		–30	—	–130	mA
COMMERCIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-4/-5/-7	—	90	140	mA
			L-10	—	90	130	mA
			L-15/-25	—	75	90	mA
			Q-10/-15/-25	—	45	55	mA
INDUSTRIAL							
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L-7/-10	—	90	160	mA
			L-15/-20/-25	—	75	130	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND.[1]	DESCRIPTION	COM / IND -10 MIN.	COM / IND -10 MAX.	COM / IND -15 MIN.	COM / IND -15 MAX.	IND -20 MIN.	IND -20 MAX.	COM / IND -25 MIN.	COM / IND -25 MAX.	UNITS
tpd	A	Input or I/O to Comb. Output	1	10	3	15	3	20	3	25	ns
tco	A	Clock to Output Delay	1	7	2	8	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	2.5	—	8	—	13	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	6	—	10	—	12	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	83.3	—	55.5	—	41.6	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	110	—	80	—	45.4	—	35.7	—	MHz
	A	Maximum Clock Frequency with No Feedback	125	—	83.3	—	50	—	38.5	—	MHz
twh	—	Clock Pulse Duration, High	4	—	6	—	10	—	13	—	ns
twl	—	Clock Pulse Duration, Low	4	—	6	—	10	—	13	—	ns
ten	B	Input or I/O to Output Enabled	1	10	3	15	3	20	3	25	ns
tdis	C	Input or I/O to Output Disabled	1	9	3	15	3	20	3	25	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	1	13	3	20	3	25	3	25	ns
tarw	—	Asynch. Reset Pulse Duration	8	—	15	—	20	—	25	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	8	—	10	—	20	—	25	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	8	—	10	—	14	—	15	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

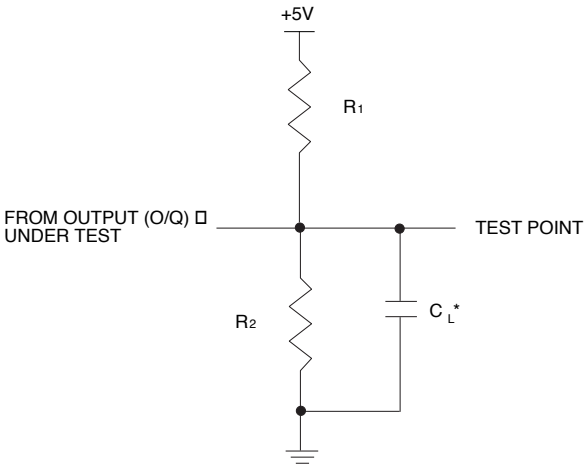
Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	D-4/-5/-7	1.5ns 10% – 90%
	D-10/-15/-20/-25	2.0ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (except D-4) (see figure below)

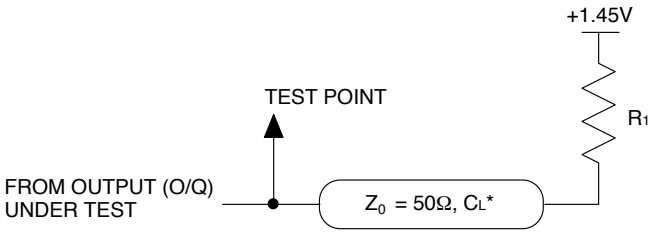
Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL22V10D-4 Output Load Conditions (see figure below)

Test Condition		R_1	C_L
A		50Ω	50pF
B	Z to Active High at 1.9V	50Ω	50pF
	Z to Active Low at 1.0V	50Ω	50pF
C	Active High to Z at 1.9V	50Ω	50pF
	Active Low to Z at 1.0V	50Ω	50pF



AC Switching Characteristics

Over Recommended Operating Conditions

PARAM	TEST COND.[1]	DESCRIPTION	COM -4 MIN.	COM -4 MAX.	COM -5 MIN.	COM -5 MAX.	COM/IND -7 MIN.	COM/IND -7 MAX.	UNITS
tpd	A	Input or I/O to Combinatorial Output	1	4	1	5	1	7.5	ns
tco	A	Clock to Output Delay	1	3.5	1	4	1	4.5	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	3	—	3	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	2.5	—	3	—	4.5	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	167	—	142.8	—	111	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	133	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	200	—	166	—	MHz
twh	—	Clock Pulse Duration, High	2	—	2.5	—	3	—	ns
twl	—	Clock Pulse Duration, Low	2	—	2.5	—	3	—	ns
ten	B	Input or I/O to Output Enabled	1	5	1	6	1	7.5	ns
tdis	C	Input or I/O to Output Disabled	1	5	1	5.5	1	7.5	ns
tar	A	Input or I/O to Asynch. Reset of Reg.	1	4.5	1	5.5	1	9	ns
tarw	—	Asynch. Reset Pulse Duration	4.5	—	4.5	—	7	—	ns
tarr	—	Asynch. Reset to Clk↑ Recovery Time	3	—	4	—	5	—	ns
tspr	—	Synch. Preset to Clk↑ Recovery Time	3	—	4	—	5	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section. Characterized initially and after any design or process changes that may affect these parameters.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.