



## DS1220Y 16k Nonvolatile SRAM

### FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2k x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 24-pin DIP package
- Read and write access times as fast as 100 ns
- Full  $\pm 10\%$  operating range
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND

### PIN ASSIGNMENT

A7	1	24	VCC
A6	2	23	A8
A5	3	22	A9
A4	4	21	WE
A3	5	20	OE
A2	6	19	A10
A1	7	18	CE
A0	8	17	DQ7
DQ0	9	16	DQ6
DQ1	10	15	DQ5
DQ2	11	14	DQ4
GND	12	13	DQ3

24-Pin ENCAPSULATED PACKAGE  
720-mil EXTENDED

### PIN DESCRIPTION

A0-A10	- Address Inputs
DQ0-DQ7	- Data In/Data Out
$\overline{\text{CE}}$	- Chip Enable
$\overline{\text{WE}}$	- Write Enable
$\overline{\text{OE}}$	- Output Enable
V <sub>CC</sub>	- Power (+5V)
GND	- Ground

### DESCRIPTION

The DS1220Y 16k Nonvolatile SRAM is a 16,384-bit, fully static, nonvolatile RAM organized as 2048 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitor V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 2k x 8 SRAMs directly conforming to the popular byte-wide 24-pin DIP standard. The DS1220Y also matches the pinout of the 2716 EPROM or the 2816 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	+260°C for 10 seconds
Caution: Do Not Reflow	(Wave or Hand Solder Only)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** ( $T_A$  : See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input Logic 1	$V_{IH}$	2.2		$V_{CC}$	V	
Input Logic 0	$V_{IL}$	0.0		+0.8	V	

**DC ELECTRICAL CHARACTERISTICS** ( $T_A$  : See Note 10;  $V_{CC} = 5V \pm 10\%$ )

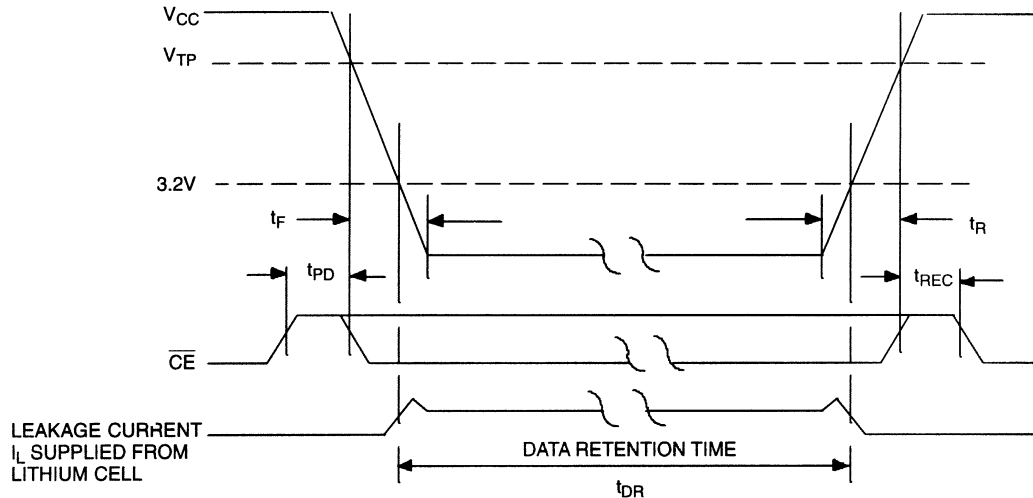
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	$I_{IL}$	-1.0		+1.0	$\mu A$	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	$I_{IO}$	-1.0		+1.0	$\mu A$	
Output Current @ 2.4V	$I_{OH}$	-1.0			mA	
Output Current @ 0.4V	$I_{OL}$	2.0			mA	
Standby Current $\overline{CE} = 2.2V$	$I_{CCS1}$		3.0	7.0	mA	
Standby Current $\overline{CE} = V_{CC} - 0.5V$	$I_{CCS2}$		2.0	4.0	mA	
Operating Current $t_{CYC} = 200ns$ (Commercial)	$I_{CCO1}$			75	mA	
Operating Current $t_{CYC} = 200ns$ (Industrial)	$I_{CCO1}$			85	mA	
Write Protection Voltage	$V_{TP}$		4.25		V	

**CAPACITANCE** ( $T_A = 25^\circ C$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	12	pF	

**AC ELECTRICAL CHARACTERISTICS** ( $T_A$  : See Note 10;  $V_{CC} = 5.0V \pm 10\%$ )

PARAMETER	SYM	DS1220Y-100		DS1220Y-120		DS1220Y-150		DS1220Y-200		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	$t_{RC}$	100		120		150		200		ns	
Access Time	$t_{ACC}$		100		120		150		200	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$		50		60		70		100	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$		100		120		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	$t_{COE}$	5		5		5		5		ns	5
Output High-Z from Deslection	$t_{OD}$		35		35		35		35	ns	5
Output Hold from Address Change	$t_{OH}$	5		5		5		5		ns	
Write Cycle Time	$t_{WC}$	100		120		150		200		ns	
Write Pulse Width	$t_{WP}$	75		90		100		150		ns	3
Address Setup Time	$t_{AW}$	0		0		0		0		ns	
Write Recovery Time	$t_{WR1}$	0		0		0		0		ns	12
	$t_{WR2}$	10		10		10		10		ns	13
Output High-Z from $\overline{WE}$	$t_{ODW}$		35		35		35		35	ns	5
Output Active from $\overline{WE}$	$t_{OEWE}$	5		5		5		5		ns	5
Data Setup Time	$t_{DS}$	40		50		60		80		ns	4
Data Hold Time	$t_{DH1}$	0		0		0		0		ns	12
	$t_{DH2}$	10		10		10		10		ns	13

**POWER-DOWN/POWER-UP CONDITION**

SEE NOTE 11

**POWER-DOWN/POWER-UP TIMING**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ at $V_{IH}$ before Power-Down	$t_{PD}$	0		$\mu\text{s}$	11
$V_{CC}$ Slew from $V_{TP}$ to 0V	$t_F$	100		$\mu\text{s}$	
$V_{CC}$ Slew from 0V to $V_{TP}$	$t_R$	0		$\mu\text{s}$	
$\overline{CE}$ at $V_{IH}$ after Power-Up	$t_{REC}$		2	ms	

 $(T_A = +25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Expected Data Retention Time	$t_{DR}$	10		years	9

**WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

- $\overline{WE}$  is high for a read cycle.
- $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during a write cycle, the output buffers remain in a high impedance state.
- $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- $t_{DS}$  are measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.

6. If the  $\overline{\text{CE}}$  low transition occurs simultaneously with or later than the  $\overline{\text{WE}}$  low transition in write cycle 1, the output buffers remain in a high impedance state during this period.
7. If the  $\overline{\text{CE}}$  high transition occurs prior to or simultaneously with the  $\overline{\text{WE}}$  high transition, the output buffers remain in a high impedance state during this period.
8. If  $\overline{\text{WE}}$  is low or the  $\overline{\text{WE}}$  low transition occurs prior to or simultaneously with the  $\overline{\text{CE}}$  low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1220Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected  $t_{\text{DR}}$  is defined as starting at the date of manufacture.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power-down condition the voltage on any pin may not exceed the voltage of  $V_{\text{CC}}$ .
12.  $t_{\text{WR1}}$ ,  $t_{\text{DH1}}$  are measured from  $\overline{\text{WE}}$  going high.
13.  $t_{\text{WR2}}$ ,  $t_{\text{DH2}}$  are measured from  $\overline{\text{CE}}$  going high.
14. DS1220Y modules are recognized by Underwriters Laboratories (UL®) under file E99151 (R).

## DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

## AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate

Input Pulse Levels: 0-3.0V

Timing Measurement Reference Levels

Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

## ORDERING INFORMATION/SELECTOR GUIDE

PART	TEMP RANGE	SUPPLY TOLERANCE	PIN-PACKAGE	SPEED GRADE (ns)
DS1220Y-100	0°C to +70°C	5V ± 10%	24 / 720 EMOD	100
DS1220Y-100+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	100
DS1220Y-100IND	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	100
DS1220Y-100IND+	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	100
DS1220Y-120	0°C to +70°C	5V ± 10%	24 / 720 EMOD	120
DS1220Y-120+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	120
DS1220Y-150	0°C to +70°C	5V ± 10%	24 / 720 EMOD	150
DS1220Y-150+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	150
DS1220Y-200	0°C to +70°C	5V ± 10%	24 / 720 EMOD	200
DS1220Y-200+	0°C to +70°C	5V ± 10%	24 / 720 EMOD	200
DS1220Y-200IND	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	200
DS1220Y-200IND+	-40°C to +85°C	5V ± 10%	24 / 720 EMOD	200

+ Denotes a lead-free/RoHS-compliant package.