GAL16V8

High Performance E²CMOS PLD Generic Array Logic™

Lead-Free Package Options Available!

Select devices have been discontinued. See Ordering Information section for product status.

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 3.5 ns Maximum Propagation Delay
  - Fmax = 250 MHz
  - 3.0 ns Maximum from Clock Input to Data Output
  - UltraMOS® Advanced CMOS Technology
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - 75mA Typ Icc on Low Power Device
  - 45mA Typ Icc on Quarter Power Device
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **LEAD-FREE PACKAGE OPTIONS**

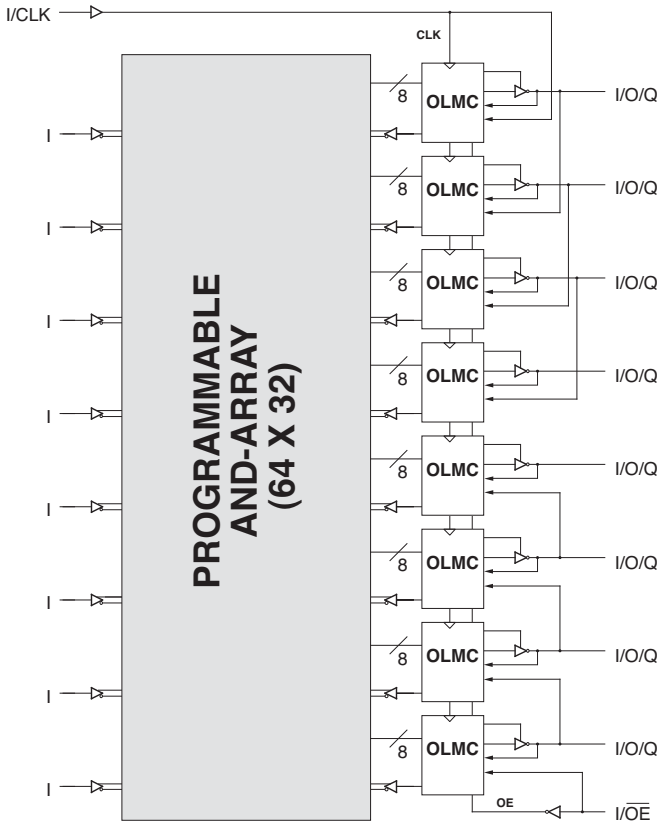
Description

The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

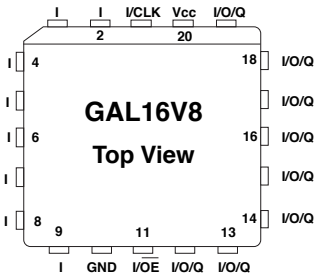
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram

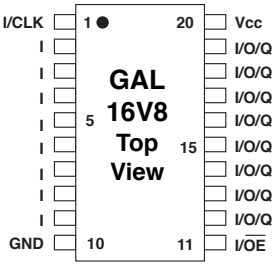


Pin Configuration

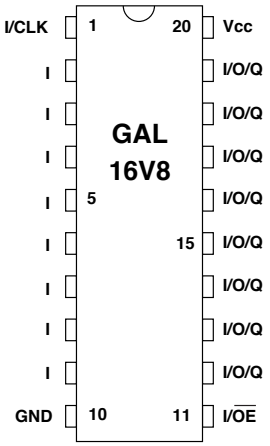
PLCC



SOIC



DIP



LATTICE SEMICONDUCTOR CORP

Lead-Free Packaging
Commercial Grade Specifications

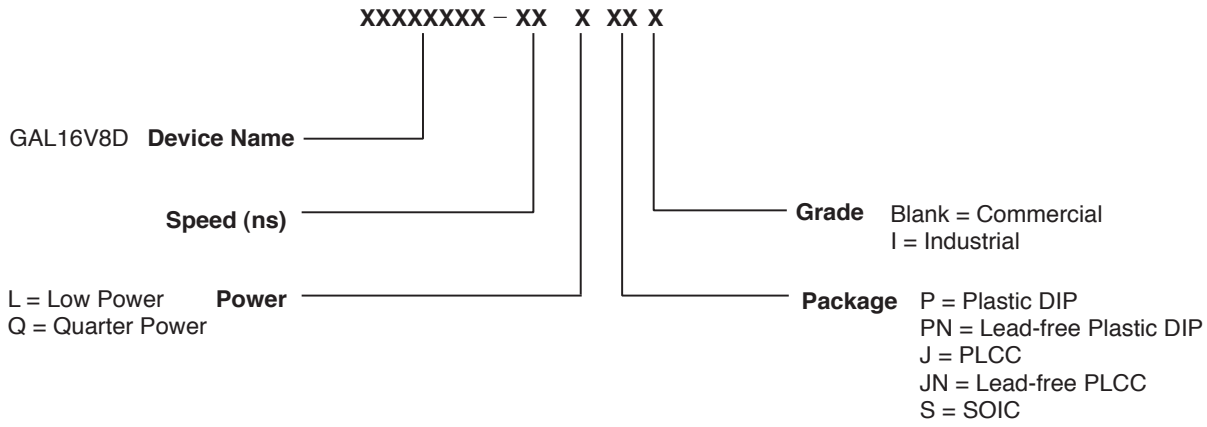
Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
3.5	2.5	3.0	115	GAL16V8D-3LJN[1]	Lead-Free 20-Lead PLCC
5	3	4	115	GAL16V8D-5LJN	Lead-Free 20-Lead PLCC
7.5	7	5	115	GAL16V8D-7LPN	Lead-Free 20-Pin Plastic DIP
			115	GAL16V8D-7LJN	Lead-Free 20-Lead PLCC
10	10	7	55	GAL16V8D-10QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-10QJN	Lead-Free 20-Lead PLCC
			115	GAL16V8D-10LPN	Lead-Free 20-Pin Plastic DIP
			115	GAL16V8D-10LJN	Lead-Free 20-Lead PLCC
15	12	10	55	GAL16V8D-15QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-15QJN	Lead-Free 20-Lead PLCC
			90	GAL16V8D-15LPN	Lead-Free 20-Pin Plastic DIP
			90	GAL16V8D-15LJN	Lead-Free 20-Lead PLCC
25	15	12	55	GAL16V8D-25QPN	Lead-Free 20-Pin Plastic DIP
			55	GAL16V8D-25QJN	Lead-Free 20-Lead PLCC
			90	GAL16V8D-25LPN	Lead-Free 20-Pin Plastic DIP
			90	GAL16V8D-25LJN	Lead-Free 20-Lead PLCC

1. Discontinued per PCN #06-07. Contact Rochester Electronics for available inventory.

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	130	GAL16V8D-7LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-7LPNI	Lead-Free 20-Pin Plastic DIP
10	10	7	130	GAL16V8D-10LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-10LPNI	Lead-Free 20-Pin Plastic DIP
15	12	10	130	GAL16V8D-15LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-15LPNI	Lead-Free 20-Pin Plastic DIP
20	13	11	65	GAL16V8D-20QJNI	Lead-Free 20-Lead PLCC
			65	GAL16V8D-20QPNI	Lead-Free 20-Pin Plastic DIP
25	15	12	65	GAL16V8D-25QJNI	Lead-Free 20-Lead PLCC
			65	GAL16V8D-25QPNI	Lead-Free 20-Pin Plastic DIP
			130	GAL16V8D-25LJNI	Lead-Free 20-Lead PLCC
			130	GAL16V8D-25LPNI	Lead-Free 20-Pin Plastic DIP

Part Number Description



Select devices have been discontinued.
See Ordering Information section for product status.

Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8 can emulate. It also shows the OLMC mode under which the GAL16V8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8	GAL16V8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

Industrial Devices:
Ambient Temperature (T_A) ..... –40 to 85°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current	L-3/-5 & -7 (Ind. PLCC)	—	—	16	mA
		L-7 (Except Ind. PLCC)/-10/-15/-25 Q-10/-15/-20/-25	—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -3/-5/-7/-10	—	75	115	mA
			L-15/-25	—	75	90	mA
			Q-10/-15/-25	—	45	55	mA

INDUSTRIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -7/-10/-15/-25	—	75	130	mA
			Q -20/-25	—	45	65	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -3		COM -5		COM / IND -7		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	1	3.5	1	5	1	7.5	ns
tco	A	Clock to Output Delay	1	3	1	4	1	5	ns
tcf[2]	—	Clock to Feedback Delay	—	2.5	—	3	—	3	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	2.5	—	3	—	5	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	182	—	142.8	—	100	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	200	—	166	—	125	—	MHz
	A	Maximum Clock Frequency with No Feedback	250	—	166	—	125	—	MHz
twh	—	Clock Pulse Duration, High	2[4]	—	3[4]	—	4	—	ns
twl	—	Clock Pulse Duration, Low	2[4]	—	3[4]	—	4	—	ns
ten	B	Input or I/O to Output Enabled	—	4.5	1	6	1	9	ns
	B	$\overline{OE}$ to Output Enabled	—	4.5	1	6	1	6	ns
tdis	C	Input or I/O to Output Disabled	—	4.5	1	5	1	9	ns
	C	$\overline{OE}$ to Output Disabled	—	4.5	1	5	1	6	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized but not 100% tested.
4) Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM.	TEST COND[1].	DESCRIPTION	COM / IND -10		COM / IND -15		IND -20		COM / IND -25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Comb. Output	3	10	3	15	3	20	3	25	ns
tco	A	Clock to Output Delay	2	7	2	10	2	11	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	8	—	9	—	10	ns
tsu	—	Setup Time, Input or Fdbk before Clk↑	7.5	—	12	—	13	—	15	—	ns
th	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	66.7	—	45.5	—	41.6	—	37	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	71.4	—	50	—	45.4	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	50	—	41.6	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	10	—	12	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	10	—	12	—	ns
ten	B	Input or I/O to Output Enabled	1	10	—	15	—	18	—	20	ns
	B	$\overline{OE}$ to Output Enabled	1	10	—	15	—	18	—	20	ns
tdis	C	Input or I/O to Output Disabled	1	10	—	15	—	18	—	20	ns
	C	$\overline{OE}$ to Output Disabled	1	10	—	15	—	18	—	20	ns

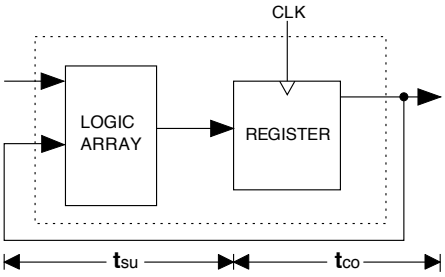
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section. Characterized but not 100% tested.

Capacitance (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

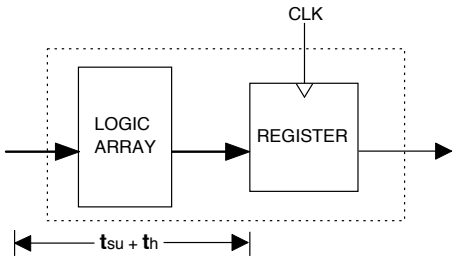
*Characterized but not 100% tested.

fmax Descriptions



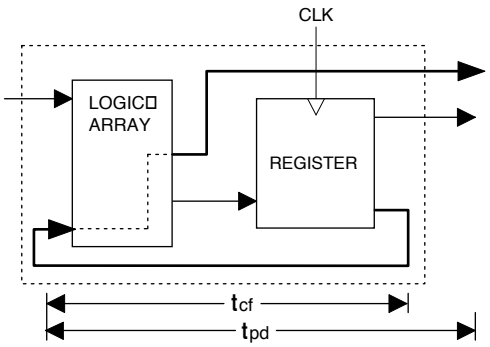
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

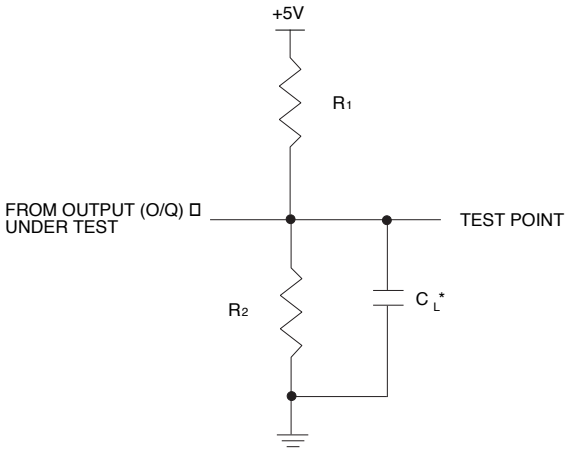
Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

Input Pulse Levels		GND to 3.0V
Input Rise and Fall Times	GAL16V8D-10 (and slower)	2 – 3ns 10% – 90%
	GAL16V8D-3/-5/-7	1.5ns 10% – 90%
Input Timing Reference Levels		1.5V
Output Timing Reference Levels		1.5V
Output Load		See figure at right

Table 2-0003/16V8

3-state levels are measured 0.5V from steady-state active level.



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

GAL16V8D (except -3) Output Load Conditions (see figure above)

Test Condition		R1	R2	CL
A		200Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF