19-5516; Rev 0; 11/10

EVALUATION KIT AVAILABLE

7A Sink, 3A Source, 12ns, SOT23 MOSFET Drivers

MAX15070A/MAX15070B

General Description

The MAX15070A/MAX15070B are high-speed MOSFET drivers capable of sinking 7A and sourcing 3A peak currents. The ICs, which are an enhancement over MAX5048 devices, have inverting and noninverting inputs that provide greater flexibility in controlling the MOSFET. They also feature two separate outputs working in complementary mode, offering flexibility in controlling both turn-on and turn-off switching speeds.

The ICs have internal logic circuitry that prevents shoot-through during output-state changes. The logic inputs are protected against voltage spikes up to +16V, regardless of V+ voltage. Propagation delay time is minimized and matched between the inverting and noninverting inputs. The ICs have a very fast switching time, combined with short propagation delays (12ns typ), making them ideal for high-frequency circuits. The ICs operate from a +4V to +14V single power supply and typically consume 0.5mA of supply current. The MAX15070A has standard TTL input logic levels, while the MAX15070B has CMOS-like high-noise-margin (HNM) input logic levels.

Both ICs are available in a 6-pin SOT23 package and operate over the -40°C to +125°C temperature range.

Applications

Power MOSFET Switching

Switch-Mode Power Supplies

DC-DC Converters

Motor Control

Power-Supply Modules

Features

- ♦ Independent Source and Sink Outputs
- ♦ +4V to +14V Single Power-Supply Range
- ♦ 7A Peak Sink Current
- ♦ 3A Peak Source Current
- ♦ Inputs Rated to +14V Regardless of V+ Voltage
- ♦ 12ns Propagation Delay
- ♦ Matched Delays Between Inverting and Noninverting Inputs Within 500ps
- ♦ HNM or TTL Logic-Level Inputs
- ♦ Low-Input Capacitance: 10pF (typ)
- ♦ Thermal-Shutdown Protection
- ♦ Small SOT23 Package Allows Routing PCB Traces Underneath
- ♦ -40°C to +125°C Operating Temperature Range

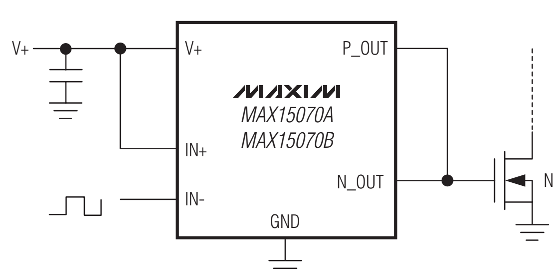
Ordering Information

PART	INPUT LOGIC LEVELS	PIN-PACKAGE
MAX15070AAUT+	TTL	6 SOT23
MAX15070BAUT+	HNM	6 SOT23

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

7A Sink, 3A Source, 12ns, SOT23 MOSFET Drivers

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V+, IN+, IN- .... -0.3V to +16V
N_OUT, P_OUT ....-0.3V to (V+ + 0.3V)
N_OUT Continuous Output Current (Note 1)................. -200mA
P_OUT Continuous Output Current (Note 1) .... +125mA
Continuous Power Dissipation (T_A = +70°C)
SOT23 (derate 8.7mW/°C above +70°C)................. 696mW*
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range.......................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

**As per JEDEC 51 standard.*

Note 1: Continuous output current is limited by the power dissipation of the package.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

SOT23
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....115°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 80°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +12V, C_L = 0, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. Parameters specified at V+ = +4.5V apply to the MAX15070A only; see Figure 1.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY (V+)							
Input Voltage Range		MAX15070A		4		14	V
		MAX15070B		6		14	
Undervoltage Lockout	V_{UVLO}	V+ rising		3.3	3.45	3.6	V
Undervoltage-Lockout Hysteresis					200		mV
Undervoltage Lockout to Output Rising Delay		V+ rising			100		µs
Undervoltage Lockout to Output Falling Delay		V+ falling			2		µs
Supply Current	I_{V+}	V+ = 14V, no switching			0.5	1	mA
		V+ = 14V, switching at 1MHz			2.3		
n-CHANNEL OUTPUT (N_OUT)							
N_OUT Resistance	R_{N_OUT}	V+ = +12V, I_{N_OUT} = -100mA	T_A = +25°C		0.256	0.32	Ω
			T_A = +125°C			0.45	
		V+ = +4.5V, I_{N_OUT} = -100mA	T_A = +25°C		0.268	0.33	
			T_A = +125°C			0.465	
Power-Off Pulldown Resistance		V+ = unconnected, I_{N_OUT} = -1mA, T_A = +25°C			1.3	1.9	kΩ
Output Bias Current	I_{BIASN}	V_{N_OUT} = V+			6	11	µA
Peak Output Current	I_{PEAKN}	C_L = 22nF			7.0		A

ELECTRICAL CHARACTERISTICS (continued)

($V+ = +12V$, $C_L = 0$, $T_A = T_J = -40°C$ to $+125°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. Parameters specified at $V+ = +4.5V$ apply to MAX15070A only, see Figure 1.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
p-CHANNEL OUTPUT (P_OUT)							
P_OUT Resistance	R_{P_OUT}	V+ = +12V, I_{P_OUT} = 100mA	T_A = +25°C		0.88	1.2	Ω
			T_A = +125°C			1.7	
		V+ = +4.5V, I_{P_OUT} = 100mA	T_A = +25°C		0.91	1.25	
			T_A = +125°C			1.75	
Output Leakage Current	I_{LEAKP}	V_{P_OUT} = 0V			0.01	1	µA
Peak Output Current	I_{PEAKN}	C_L = 22nF			3.0		A
LOGIC INPUTS (IN+, IN-)							
Logic-High Input Voltage	V_{IH}	MAX15070A		2.0			V
		MAX15070B		4.25			
Logic-Low Input Voltage	V_{IL}	MAX15070A				0.8	V
		MAX15070B				2.0	
Logic-Input Hysteresis	V_{HYS}	MAX15070A			0.2		V
		MAX15070B			0.9		
Logic-Input Leakage Current		$V_{IN+} = V_{IN-}$ = 0V or V+, MAX15070A			0.02		µA
Logic-Input Bias Current		$V_{IN+} = V_{IN-}$ = 0V or V+, MAX15070B			10		
Input Capacitance					10		pF
SWITCHING CHARACTERISTICS FOR V+ = +12V (Figure 1)							
Rise Time	t_R	C_L = 1nF			6		ns
		C_L = 5nF			22		
		C_L = 10nF			36		
Fall Time	t_F	C_L = 1nF			4		ns
		C_L = 5nF			11		
		C_L = 10nF			17		
Turn-On Delay Time	t_{D-ON}	C_L = 1nF (Note 4)		7	11	17	ns
Turn-Off Delay Time	t_{D-OFF}	C_L = 1nF (Note 4)		7	12	18	ns
Break-Before-Make Time	t_{BBM}				2		ns
SWITCHING CHARACTERISTICS FOR V+ = +4.5V (MAX15070A only) (Figure 1)							
Rise Time	t_R	C_L = 1nF			5		ns
		C_L = 5nF			16		
		C_L = 10nF			25		
Fall Time	t_F	C_L = 1nF			4		ns
		C_L = 5nF			10		
		C_L = 10nF			14		
Turn-On Delay Time	t_{D-ON}	C_L = 1nF (Note 4)		7	13	21	ns
Turn-Off Delay Time	t_{D-OFF}	C_L = 1nF (Note 4)		7	14	22	ns
Break-Before-Make Time	t_{BBM}				2		ns
THERMAL CHARACTERISTICS							
Thermal Shutdown		Temperature rising (Note 4)			166		°C
Thermal-Shutdown Hysteresis		(Note 4)			13		°C

Note 3: Limits are 100% tested at T_A = +25°C. Limits over operating temperature range are guaranteed through correlation using the statistical quality control (SQC) method.

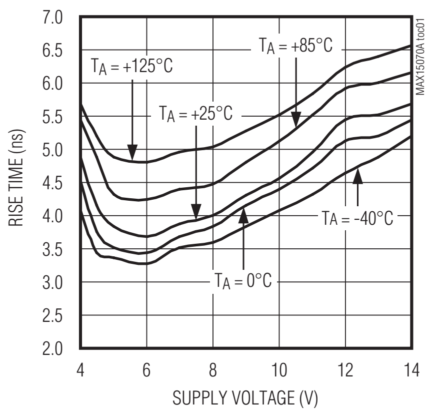
Note 4: Design guaranteed by bench characterization. Limits are not production tested.

7A Sink, 3A Source, 12ns, SOT23 MOSFET Drivers

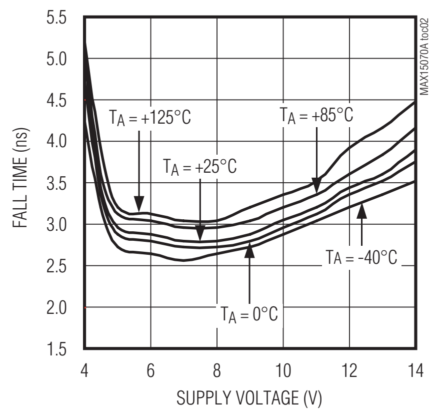
Typical Operating Characteristics

(C_L = 1000pF, T_A = +25°C, unless otherwise noted. See Figure 1.)

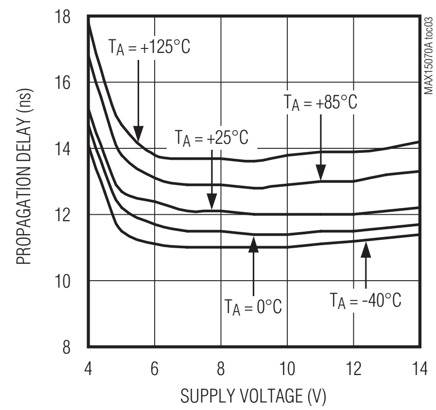
RISE TIME vs. SUPPLY VOLTAGE



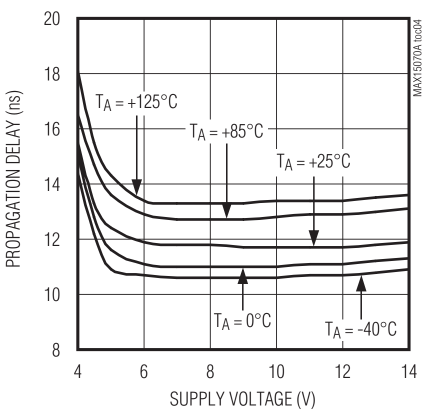
FALL TIME vs. SUPPLY VOLTAGE



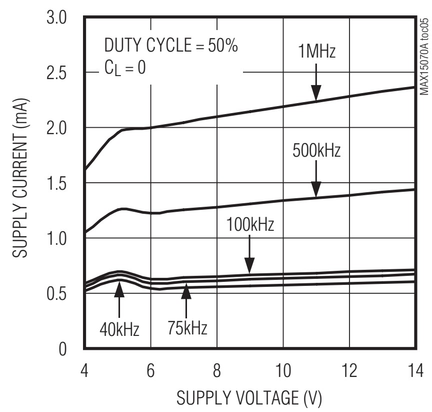
PROPAGATION DELAY (LOW TO HIGH) vs. SUPPLY VOLTAGE



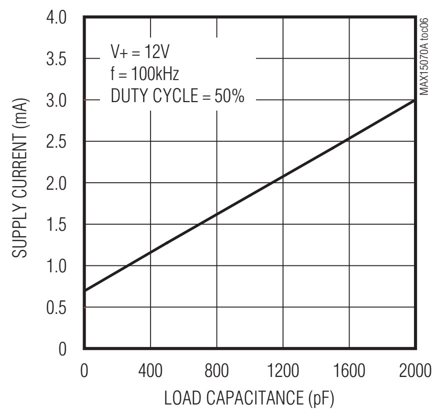
PROPAGATION DELAY (HIGH TO LOW) vs. SUPPLY VOLTAGE



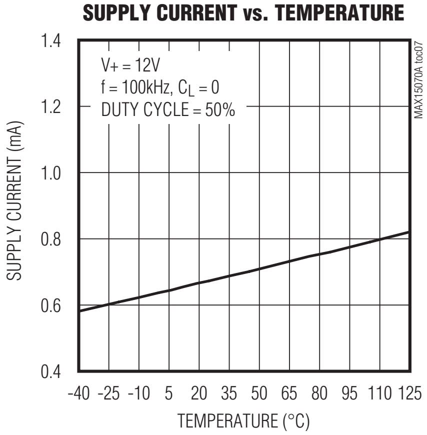
SUPPLY CURRENT vs. SUPPLY VOLTAGE



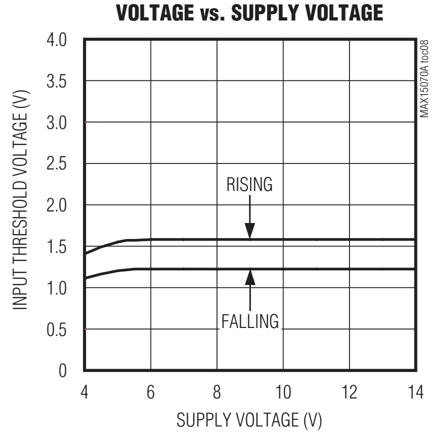
SUPPLY CURRENT vs. LOAD CAPACITANCE



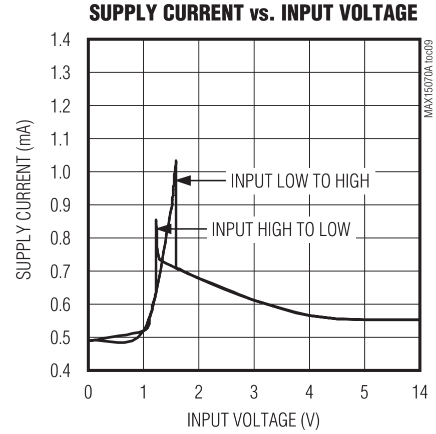
SUPPLY CURRENT vs. TEMPERATURE



MAX15070A INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



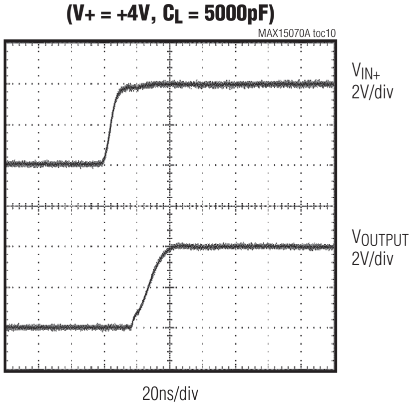
MAX15070A SUPPLY CURRENT vs. INPUT VOLTAGE



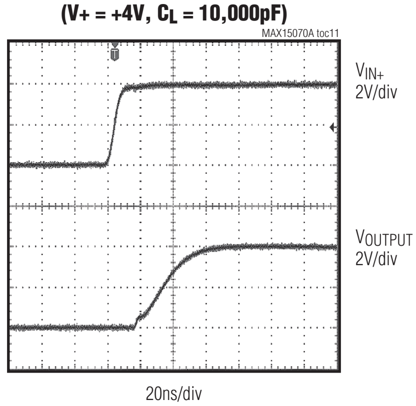
Typical Operating Characteristics (continued)

(C_L = 1000pF, T_A = +25°C, unless otherwise noted. See Figure 1.)

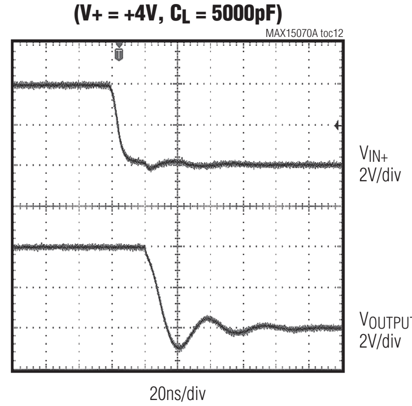
INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +4V, C_L = 5000pF)



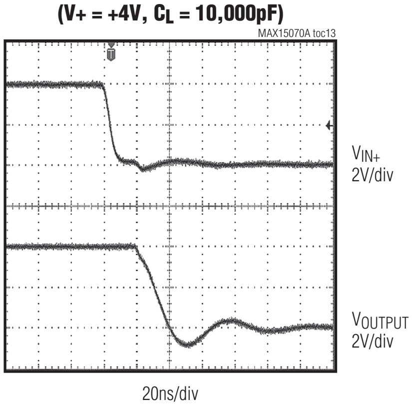
INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +4V, C_L = 10,000pF)



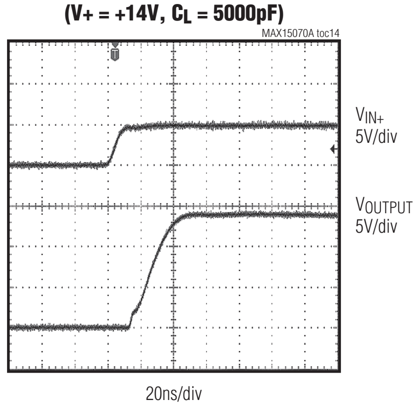
INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +4V, C_L = 5000pF)



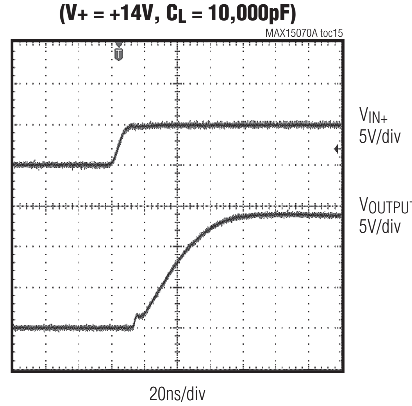
INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +4V, C_L = 10,000pF)



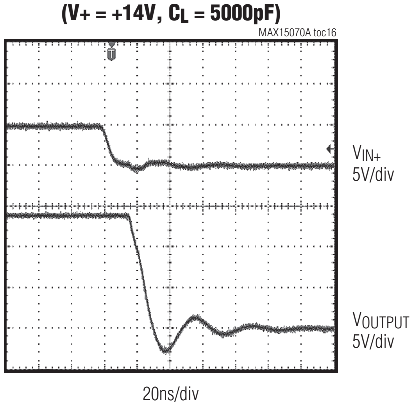
INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +14V, C_L = 5000pF)



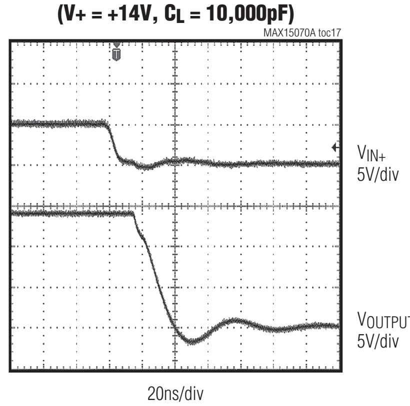
INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +14V, C_L = 10,000pF)



INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +14V, C_L = 5000pF)

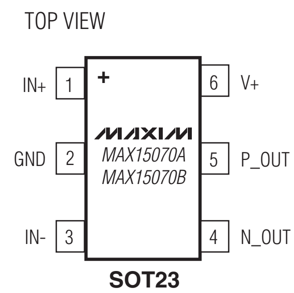


INPUT VOLTAGE vs. OUTPUT VOLTAGE ($V+$ = +14V, C_L = 10,000pF)



7A Sink, 3A Source, 12ns, SOT23 MOSFET Drivers

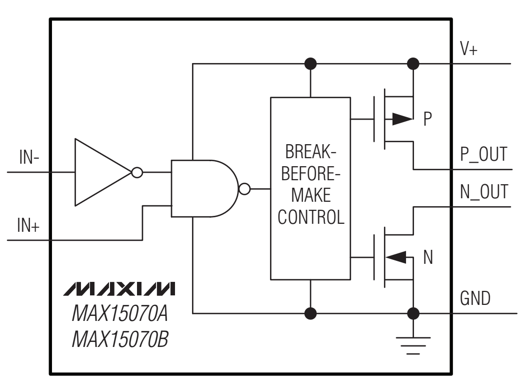
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	IN+	Noninverting Logic Input. Connect IN+ to V+ when not used.
2	GND	Ground
3	IN-	Inverting Logic Input. Connect IN- to GND when not used.
4	N_OUT	Driver Sink Output. Open-drain n-channel output. Sinks current for power MOSFET turn-off.
5	P_OUT	Driver Source Output. Open-drain p-channel output. Sources current for power MOSFET turn-on.
6	V+	Power-Supply Input. Bypass V+ to GND with a 1µF low-ESR ceramic capacitor.

Functional Diagram



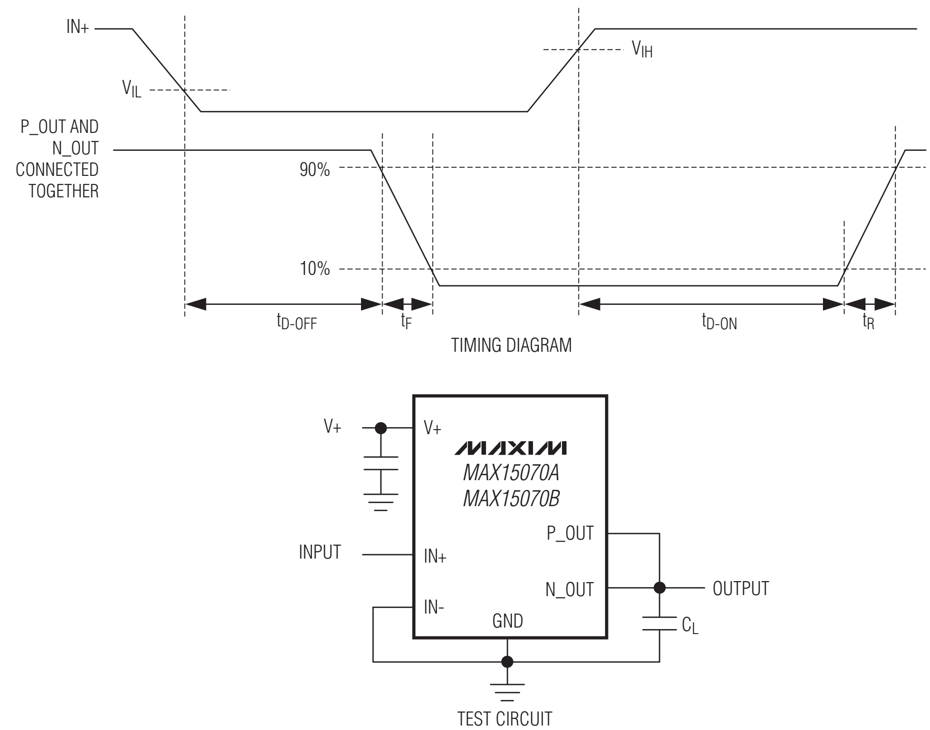


Figure 1. Timing Diagram and Test Circuit

Detailed Description

Logic Inputs

The MAX15070A/MAX15070Bs' logic inputs are protected against voltage spikes up to +16V, regardless of the V+ voltage. The low 10pF input capacitance of the inputs reduces loading and increases switching speed. These ICs have two inputs that give the user greater flexibility in controlling the MOSFET. Table 1 shows all possible input combinations. The difference between the MAX15070A and the MAX15070B is the input threshold voltage. The MAX15070A has TTL logic-level thresholds, while the MAX15070B has HNM (CMOS-like) logic-level thresholds (see the *Electrical Characteristics*). Connect IN+ to V+ or IN- to GND when not used. Alternatively, the unused input can be used as an on/off control input (Table 1).

Table 1. Truth Table

IN+	IN-	p-CHANNEL	n-CHANNEL
L	L	Off	On
L	H	Off	On
H	L	On	Off
H	H	Off	On

L = Logic-low, H = Logic-high.

Undervoltage Lockout (UVLO)

When V+ is below the UVLO threshold, the n-channel is on and the p-channel is off, independent of the state of the inputs. The UVLO is typically 3.45V with 200mV typical hysteresis to avoid chattering. A typical falling delay of 2µs makes the UVLO immune to narrow negative transients in noisy environments.

Driver Outputs

The ICs provide two separate outputs. One is an open-drain p-channel, the other an open-drain n-channel. They have distinct current sourcing/sinking capabilities to independently control the rise and fall times of the MOSFET gate. Add a resistor in series with P_OUT/N_OUT to slow the corresponding rise/fall time of the MOSFET gate.

Applications Information

Supply Bypassing, Device Grounding, and Placement

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V+ pin can approach 3A, while at the GND pin, the peak current can approach 7A. V_{CC} drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the IN- input is used and the input slew rate is low. The device driving the input should be referenced to the ICs' GND pin, especially when the IN- input is used. Ground shifts due to insufficient device grounding can disturb other circuits sharing the same AC ground return path. Any series inductance in the V+, P_OUT, N_OUT, and/or GND paths can cause oscillations due to the very high di/dt that results when the ICs are switched with any capacitive load. A 1µF or larger value ceramic capacitor is recommended, bypassing V+ to GND and placed as close as possible to the pins. When driving very large loads (e.g., 10nF) at minimum rise time, 10µF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the ICs as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

Power Dissipation

Power dissipation of the ICs consists of three components, caused by the quiescent current, capacitive charge and discharge of internal nodes, and the output current (either capacitive or resistive load). The sum of these components must be kept below the maximum power-dissipation limit of the package at the operating temperature.

The quiescent current is 0.5mA typical. The current required to charge and discharge the internal nodes is frequency dependent (see the *Typical Operating Characteristics*).

For capacitive loads, the total power dissipation is approximately:

$$P = C_{LOAD} \times (V+)^2 \times FREQ$$

where C_{LOAD} is the capacitive load, V+ is the supply voltage, and FREQ is the switching frequency.

Layout Information

The ICs' MOSFET drivers source and sink large currents to create very fast rise and fall edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the ICs:

- Place one or more 1µF decoupling ceramic capacitor(s) from V+ to GND as close as possible to the IC. At least one storage capacitor of 10µF (min) should be located on the PCB with a low resistance path to the V+ pin of the ICs. There are two AC current loops formed between the IC and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from N_OUT of the ICs to the MOSFET gate to the MOSFET source and to GND of the ICs. When the gate of the MOSFET is being pulled high, the active current loop is from P_OUT of the ICs to the MOSFET gate to the MOSFET source to the GND terminal of the decoupling capacitor to the V+ terminal of the decoupling capacitor and to the V+ terminal of the ICs. While the charging current loop is important, the discharging current loop is critical. It is important to minimize the physical distance and the impedance in these AC current paths.
- In a multilayer PCB, the component surface layer surrounding the ICs should consist of a GND plane containing the discharging and charging current loops.

Chip Information

Process: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SOT23	U6+1	21-0058	90-0175

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/10	Initial release	—