DDR VDDQ and VTT Termination Voltage Regulator

Features

- Two linear regulators
  - -Maximum 2A current from VDDQ
  - -Source and sink up to 2A VTT current
- 1.7V to 2.8V adjustable VDDQ output voltage
- 0.85V to 1.4V VTT output voltage (tracking at 50% of VDDQ)
- Buffered VREF output
- 500mV typical VDDQ dropout voltage at 2A
- Excellent load and line regulation, low noise
- Meets JEDEC DDR-I and DDR-II memory power spec
- Linear regulator design requires no inductors and has low external component count
- Integrated power MOSFETs
- Dual purpose ADJ/Shutdown pin
- Enable VTT pin for sleep or suspend to RAM function
- Built-in over-current limit and thermal shutdown for VDDQ and VTT
- Fast transient response
- Low quiescent current
- TDFN-8 RoHS compliant lead-free package
- SOIC-8 RoHS compliant lead-free package

Applications

- DDR memory and active termination buses
- Desktop computers, servers
- Residential and enterprise gateways
- DSL modems
- Routers and switches
- DVD recorders, LCD TV and STB
- 3D AGP cards

Product Description

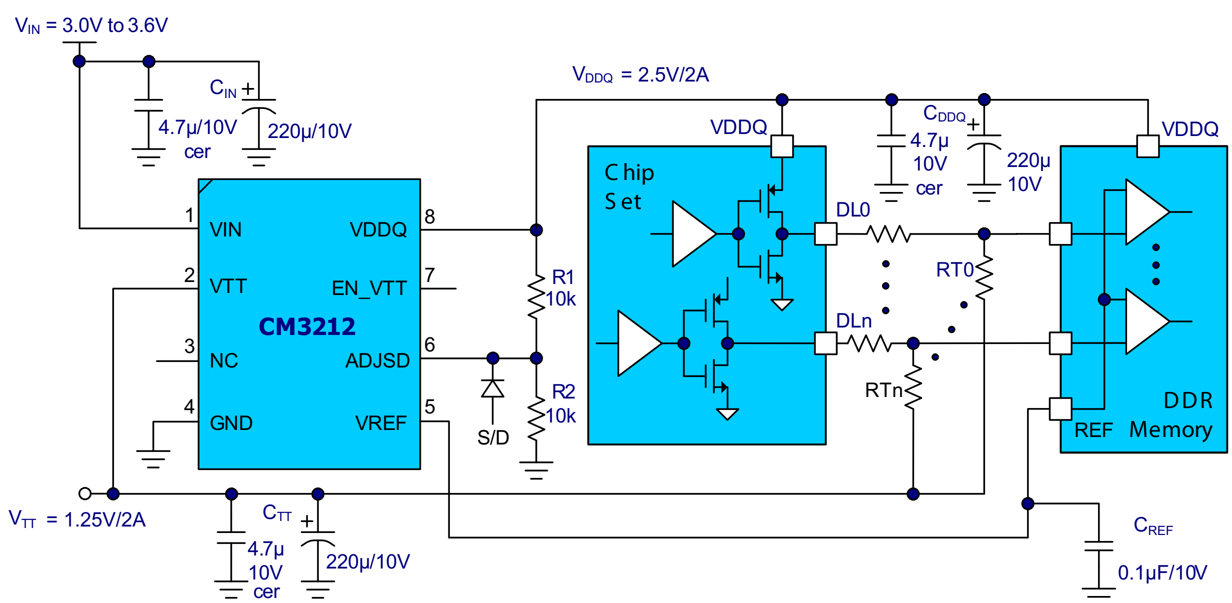
The CM3212 is a dual-output low noise linear regulator designed to meet SSTL-2 and SSTL-3 specifications for DDR-SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFETs the CM3212 can source up to 2A of VDDQ continuous current, and source or sink up to 2A VTT continuous current. The typical dropout voltage for VDDQ is 500mV at 2A load current.

The CM3212 provides excellent full load regulation and fast response to transient load changes. It also has built-in over-current limits and thermal shutdown at 170°C.

The CM3212 supports Suspend-To-RAM (STR) and ACPI compliance with Shutdown Mode which tri-states VTT to minimize quiescent system current.

The CM3212 is available in a space saving TDFN-8 and SOIC-8 surface mount packages. Low thermal resistance allows them to withstand high power dissipation at 85°C ambient. The CM3212 can operate over the industrial ambient temperature range of –40°C to 85°C.

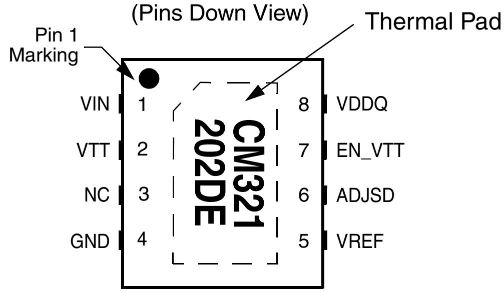
Typical Application



Package Pinout

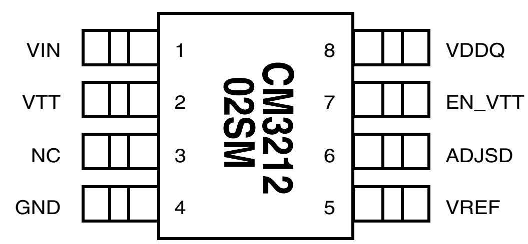
PACKAGE / PINOUT DIAGRAM

Top View
(Pins Down View)



8-Lead TDFN Package
CM3212-02DE

Top View
(Pins Down View)



8-Lead SOIC Package
CM3212-02SM

Note: These drawings are not to scale.

PIN DESCRIPTIONS

PIN(s) TDFN-8	PIN(s) SOIC-8	NAME	DESCRIPTION
1	1	VIN	Input supply voltage pin. Bypass with a 220µF capacitor to GND.
2	2	VTT	V_{TT} regulator output pin, which is preset to 50% of V_{DDQ}.
3	3	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
4	4	GND	Ground pin.
5	5	VREF	Reference voltage output pin. This pin buffers internal reference of $V_{DDQ}/2$. Bypass with 0.1µF ceramic to GND. It is available as long as V_{DDQ} is enabled. During Manual Shutdown or Thermal Shutdown, it is tied to GND.
6	6	ADJSD	This pin is for V_{DDQ} output voltage adjustment. It is available as long as V_{DDQ} is enabled. During Manual/Thermal shutdown, it is tightened to GND. The V_{DDQ} output voltage is set using an external resistor divider connected to ADJSD: $V_{DDQ} = 1.25V \times \frac{R1 + R2}{R2}$ where R1 is the upper resistor and R2 is the ground-side resistor. In addition, the ADJSD pin functions as a Shutdown pin. When ADJSD voltage is higher than 2.7V (SHDN_H), the circuit is in Shutdown mode. When ADJSD voltage is below 1.5V (SHDN_L), both VDDQ and VTT are enabled. A low-leakage Schottky diode in series with ADJSD pin is recommended to avoid interference with the voltage adjustment setting.
7	7	EN_VTT	Enable pin for V_{TT} regulator (it is internally pulled 'high'). A logic HIGH on this pin enables the V_{TT} output, and a logic LOW on this pin tri-states the V_{TT} output.
8	8	VDDQ	VDDQ regulator output voltage pin.
EPad		GND	The backside exposed pad which serves as the package heatsink. Must be connected to GND.

Ordering Information

PART NUMBERING INFORMATION			
		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking
8	TDFN	CM3212-02DE	CM321 202DE
8	SOIC	CM3212-02SM	CM3212 02SM

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
VIN to GND	[GND - 0.3] to +6.0	V
Pin Voltages V_{DDQ},V_{TT} to GND ADJSD to GND	 [GND - 0.3] to +6.0 [GND - 0.3] to +6.0	 V V
Output Current VDDQ / VTT, continuous(1) VDDQ / VTT, peak VDDQ Source + VTT Source	 2.0 / ± 2.0 2.8 / ± 2.8 3	 A A A
Temperature Operating Ambient Operating Junction Storage	 –40 to +85 –40 to + 170 –40 to +150	 °C °C °C
Thermal Resistance, R_{JA}(2) TDFN-8, 3mm x 3mm SOIC-8	 55 120	 °C/W °C/W
Continuous Power Dissipation(2) TDFN-8, T_A = 25°C / 85°C SOIC-8, T_A = 25°C / 85°C	 2.6 / 1.5 1.2 / 0.7	 W W
ESD Protection (HBM)	2000	V
Lead Temperature (soldering, 10sec)	300	°C

Note 1: Despite the fact that the device is designed to handle large continuous/peak output currents, it is not capable of handling these under all conditions. Limited by the package thermal resistance, the maximum output current of the device cannot exceed the limit imposed by the maximum power dissipation value.

Note 2: Measured with the package using a 4 in^2 / 2 layers PCB with thermal vias.

Specifications (cont'd)

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Ambient Operating Temperature Range	–40 to +85	°C
VDDQ Regulator Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 sec) C_{DDQ}	 3.0 to 3.6 0 to 2 2.5 220	 V A A µF
VTT Regulator Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 sec) C_{TT}	 3.0 to 3.6 0 to ±2.0 ±2.50 220	 V A A µF
VIN Supply Voltage Range	3.0 to 3.6	V
VDDQ Source + VTT Source Load Current, Continuous Load Current, Peak (1 sec)	 2.5 3.5	 A A
Junction Operating Temperature Range	–40 to +150	°C

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
General						
VIN	Supply Voltage Range		3.0		3.6	V
I_Q	Quiescent Current	$I_{DDQ} = 0$, $I_{TT} = 0$		8	15	mA
V_{ADJSD}	ADJSD Voltage	(3)	1.225	1.250	1.275	V
I_{SHDN}	Shutdown Current	$V_{ADJSD} = 3.3V$ (shutdown)		0.2	0.5	mA
SHDN_H	ADJSD Logic High	(2)	2.7			V
SHDN_L	ADJSD Logic Low	(3)			1.5	V
UVLO	Under-voltage Lockout	Hysteresis = 100mV (3)	2.40	2.70	2.90	V
T_{OVER}	Thermal SHDN Threshold	(3)	150	170		°C
T_{HYS}	Thermal SHDN Hysteresis			50		°C
TEMPCO	V_{DDQ}, V_{TT} TEMPCO	$I_{OUT} = 1A$ (3)		100		ppm/°C
VDDQ Regulator						
$V_{DDQ\ DEF}$	VDDQ Output Voltage	$I_{DDQ} = 100mA$	2.450	2.500	2.550	V
$V_{DDQ\ LOAD}$	VDDQ Load Regulation	$10mA \le I_{DDQ} \le 2A$ (4)		10	25	mV
$V_{DDQ\ LINE}$	VDDQ Line Regulation	$3.0V \le VIN \le 3.6V$, $I_{DDQ} = 0.1A$		5	25	mV
V_{DROP}	VDDQ Dropout Voltage	$I_{DDQ} = 2A$ (5)		500		mV
I_{ADJ}	ADJSD Bias Current	(3)		0.8	3	µA
$I_{DDQ\ LIM}$	VDDQ Current Limit		2.0	2.5		A
VTT Regulator						
$V_{TT\ DEF}$	VTT Output Voltage	$I_{TT} = 100mA$	1.225	1.250	1.275	V

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{TT\ LOAD}$	VTT Load Regulation	Source, 10mA ≤ I_{TT} ≤ 2A(4) Sink, -2A ≤ I_{TT} ≤ 10mA(4)	 –30	10 –10	30	mV mV
$V_{TT\ LINE}$	VTT Line Regulation	3.0V ≤ VIN ≤ 3.6V, I_{TT} = 0.1A		5	15	mV
$I_{TT\ LIM}$	ITT Current Limit	Source / Sink(4)	±2.0	±2.5		A
$I_{VTT\ OFF}$	VTT Shutdown Leakage Current	V_{EN_VTT} = 0.4V (shutdown)			10	µA
V_{REF}	Reference Voltage	C_{REF} = 0.1µF, I_{REF} = 100µA	1.225	1.250	1.275	V

Note 1: VIN = 3.3V, V_{DDQ} = 2.50V, VTT = 1.25V (default values), C_{DDQ}=C_{TT}=47µF, T_A = 25°C unless otherwise specified.

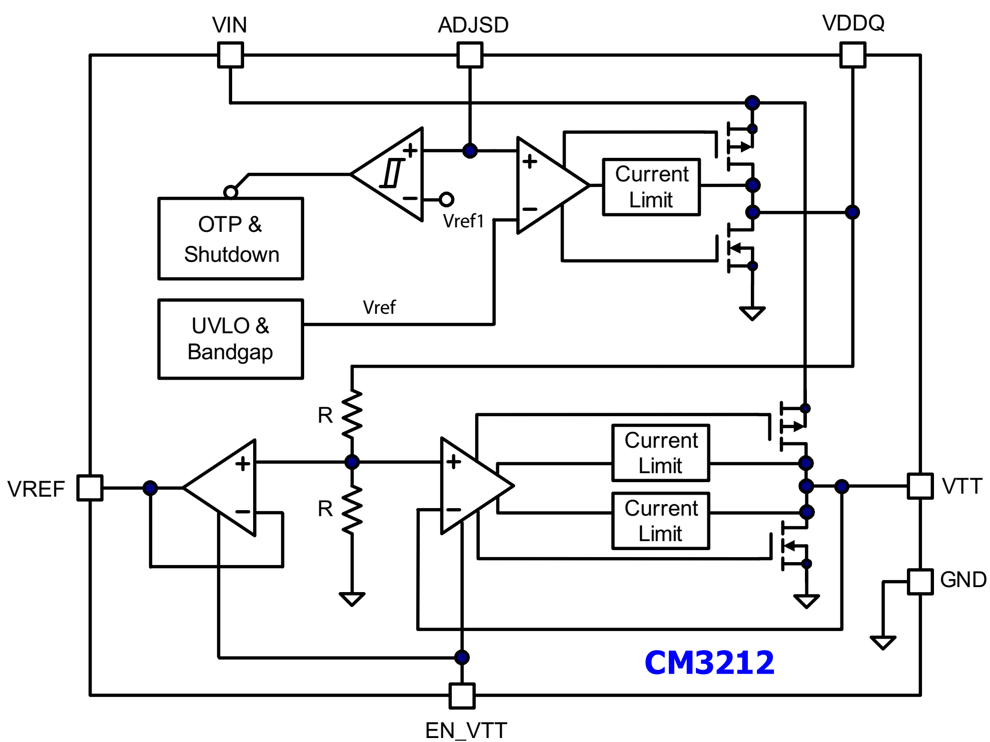
Note 2: The ADJSD Logic High value is normally satisfied for full input voltage range by using a low leakage current (below 1µA). Schottky diode at ADJSD control pin.

Note 3: Guaranteed by design.

Note 4: Load and line regulation are measured at constant junction temperature by using pulse testing with a low duty cycle. For high current tests, correlation method can be used. Changes in output voltage due to heating effects must be taken into account separately. Load and line regulation values are guaranteed by design up to the maximum power dissipation.

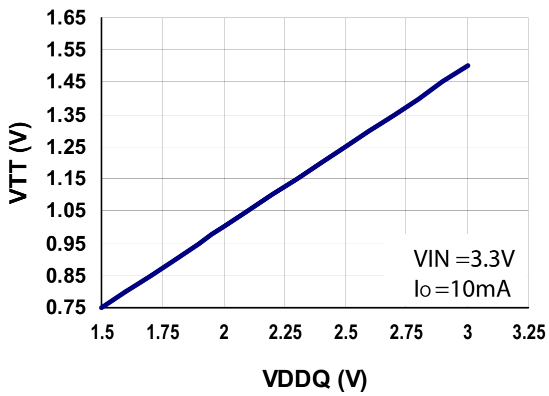
Note 5: Dropout voltage is the input to output voltage differential at which output voltage has dropped 100mV from the nominal value obtained at 3.3V input. It depends on load current and junction temperature. Guaranteed by design.

Functional Block Diagram

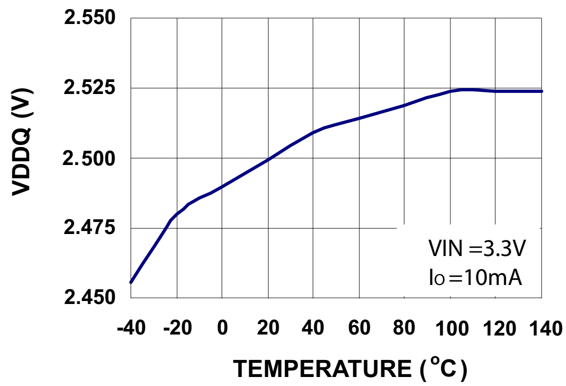


Typical Operating Characteristics

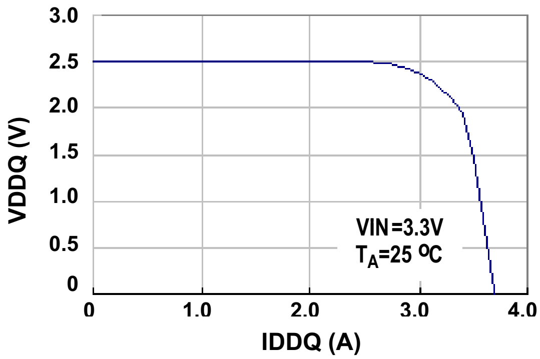
VTT vs. VDDQ



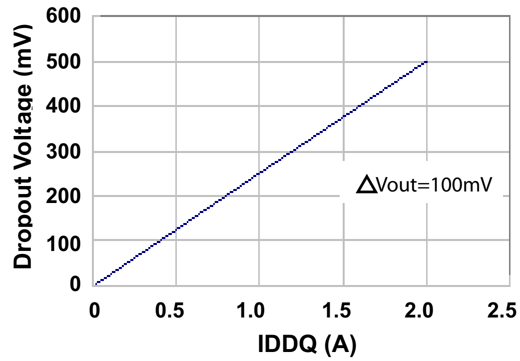
VDDQ vs. Temperature



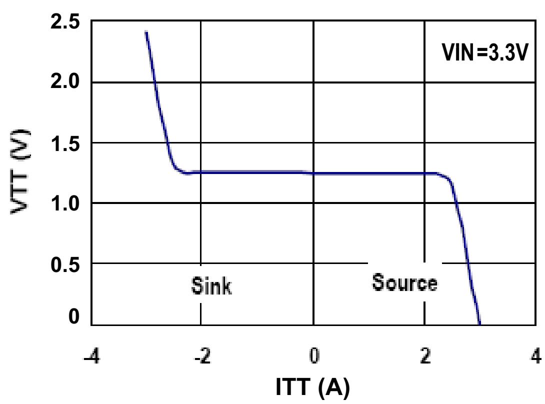
VDDQ vs. Load Current



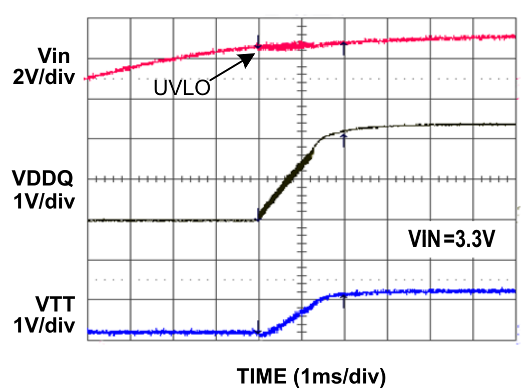
VDDQ Dropout vs. IDDQ



VTT vs. Load Current

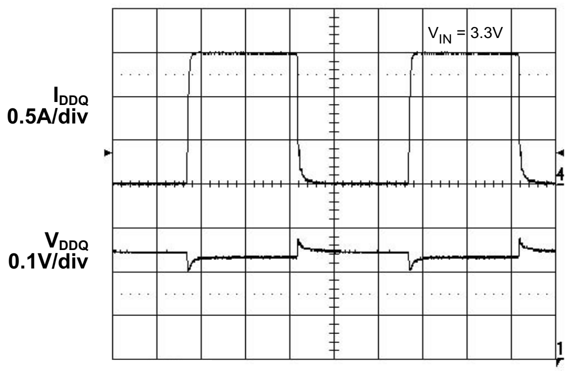


Startup into Full Load



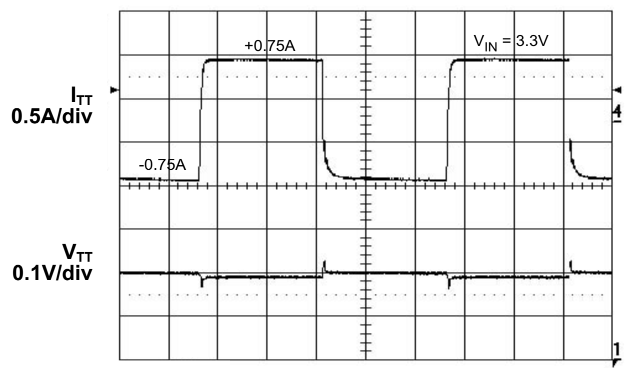
Typical Operating Characteristics (cont'd)

VDDQ Transient Response



TIME (0.2ms/div)

VTT Transient Response



TIME (0.2ms/div)

Application Info

Powering DDR Memory

Double-Data-Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAMs transmit data at both the rising and falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power-supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2), and by the use of a termination voltage, V_{TT}. SSTL_2 is an industry standard defined in JEDEC document JESD8-9. SSTL_2 maintains high-speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: V_{DDQ}, V_{TT}, and V_{REF} (see Figure 1). In a typical SSTL_2 receiver, the higher current V_{DDQ} supply voltage is normally 2.5V with a tolerance of ±200mV. The active bus termination voltage, V_{TT}, is half of V_{DDQ}. V_{REF} is a reference voltage that tracks half of V_{DDQ} ±1%, and is compared with the V_{TT} terminated signal at the receiver. V_{TT} must be within ±40 mV of V_{REF}.

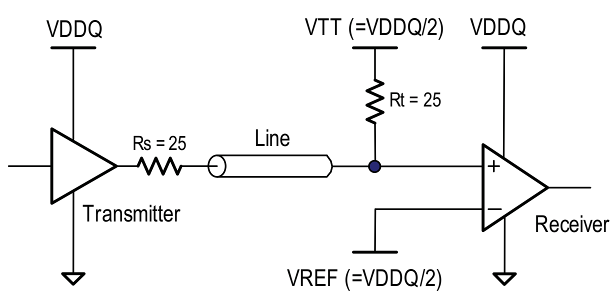


Figure 1. Typical DDR terminations, Class II

The VTT power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2mA to achieve the 405mV minimum over V_{TT} needed at the receiver:

$$I_{terminaton} = \frac{405mV}{Rt(25\Omega)} = 16.2mA$$

A typical 64Mbyte SSTL-2 memory system, with 128 terminated lines, has a worst-case maximum V_{TT} supply current up to ± 2.07A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ±200mA.

The VDDQ power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5A to 1A, with peaks up to 2A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

CM3212 Regulator

The CM3212 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single package. VDDQ regulator can supply up to 2A current, and the two-quadrant V_{TT} termination regulator has current sink and source capability to ±2A. The VDDQ linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500mV at a 2A output. The output voltage of V_{DDQ} can be set by an external voltage divider. The use of regulators for both the upper and lower side of the VDDQ output allows a fast transient response to any change of the load, from high current to low current or inversely. The second output, V_{TT}, is regulated at $V_{DDQ}/2$ by an internal resistor divider. Same as VDDQ, VTT has the same fast transient response to load change in both directions. The V_{TT} regulator can source, as well as sink, up to 2A

Application Info (cont'd)

current. The CM3212 is designed for optimal operation from a nominal 3.3VDC bus, but can work with VIN up to 5V. When operating at higher VIN voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation. Limited by the package thermal resistance, the maximum output current of the device at higher VIN cannot exceed the limit imposed by the maximum power dissipation value.

V_{REF} is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate V_{REF} can be created with a simple voltage divider of precision, matched resistors from V_{DDQ} to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

Input and Output Capacitors

The CM3212 requires that at least a 220µF electrolytic capacitor be located near the VIN pin for stability and to maintain the input bus voltage during load transients. An additional 4.7µF ceramic capacitor between the VIN and GND, located as close as possible to those pins, is recommended to ensure stability.

At a minimum, a 220µF electrolytic capacitor is recommended for the V_{DDQ} output. An additional 4.7µF ceramic capacitor between the V_{DDQ} and GND, located very close to those pins, is recommended.

At a minimum, a 220µF electrolytic capacitor is recommended for the V_{TT} output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7µF ceramic capacitor between the V_{TT} pin and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the V_{TT} window of 40mV during the transition for source to sink. An average current step of ±0.5A requires:

$$ESR < \frac{40\text{mV}}{1\text{A}} = 40\text{m}\Omega$$

Both outputs will remain stable and in regulation even during light or no load conditions. The general recommendation for circuit stability for the CM3212 requires the following:

1.) $C_{in}=C_{ddq}=C_{tt}=220\mu F/4.7\mu F$ for the full temperature range of –40 to +85°C.

2.) $C_{in}=C_{ddq}=C_{tt}=100\mu F/2.2\mu F$ for the temperature range of –25 to +85°C.

Adjusting VDDQ Output Voltage

The CM3212 internal bandgap reference is set at 1.25V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

$$V_{DDQ} = V_{ADJ} \times \frac{R1 + R2}{R2}$$

where V_{ADJ} = 1.25V. The recommended divider value is $R_1=R_2=10k\Omega$ for DDR-1 application, and $R1=4.42k\Omega$, $R2=10k\Omega$ for DDR-2 application (V_{DDQ}=1.8V, V_{TT}=0.9V).

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high (SHDN_H), both the VDDQ and the VTT outputs tri-state and could sink/source less than 10µA. During shutdown, the quiescent current is reduced to less than 0.5mA, independent of output load.

It is recommended that a low leakage Schottky diode be placed between the ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the CM3212 is again enabled.

For Shutdown operation, observe the following:

V_{DDQ}	Under ADJSD shutdown condition, V_{DDQ} should go to tri-state.
	Under EN_VTT shutdown condition, V_{DDQ} should keep state (2.5V).
V_{TT}	Under ADJSD or EN_VTT shutdown condition, V_{TT} should go to tri-state and should sink or source less than 10µA.
V_{REF}	Under ADJSD shutdown condition, V_{REF} should go to zero.
	Under EN_VTT shutdown condition, V_{REF} should keep state (1.2V or V_{DDQ}/2).

Application Info (cont'd)

Current Limit and Over-temperature Protection

The CM3212 features internal current limiting with thermal protection. During normal operation, V_{DDQ} limits the output current to approximately 2A and V_{TT} limits the output current to approximately ±2A. When V_{TT} is current limiting into a hard short circuit, the output current folds back to a lower level (~1A) until the over-current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170°C (typical), the thermal protection circuitry triggers and tri-states both VDDQ and VTT outputs. Once the junction temperature has cooled to below about 120°C the CM3212 returns to normal operation.

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) primarily consists of two paths in the series. The first path is the junction to the case (θ_{JC}) which is defined by the package style and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any condition can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D \times (\theta_{JC}) + P_D \times (\theta_{CA})$$

$$= T_{AMB} + P_D \times (\theta_{CA})$$

When a CM3212 using TDFN-8 package is mounted on a double-sided printed circuit board with four square inches of copper allocated for "heat spreading," the θ_{JA} is approximately 55°C/W. Based on the over temperature limit of 170°C with an ambient temperature of 85°C, the available power of the package will be:

$$P_D = \frac{170°C - 85°C}{55°C/W} = 1.5W$$

PCB Layout Considerations

The CM3212 has a heat spreader (exposed pad) attached to the bottom of the TDFN-8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad with slightly smaller dimensions than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. Figure 2 shows the CM3212 recommended PCB layout. Please note there are four vias to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias must be placed underneath the chip but this can result in solder blockage. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and away from other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3212 to ambient temperature.

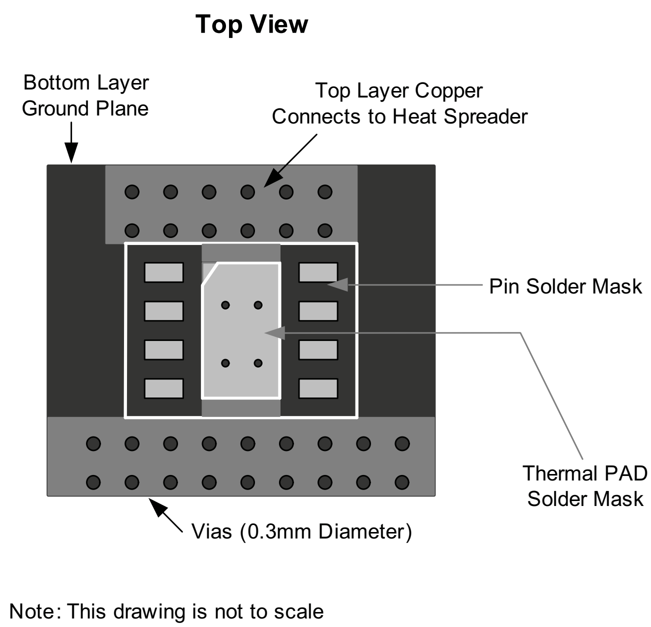


Figure 2. Thermal Layout for TDFN-8 package

Mechanical Details

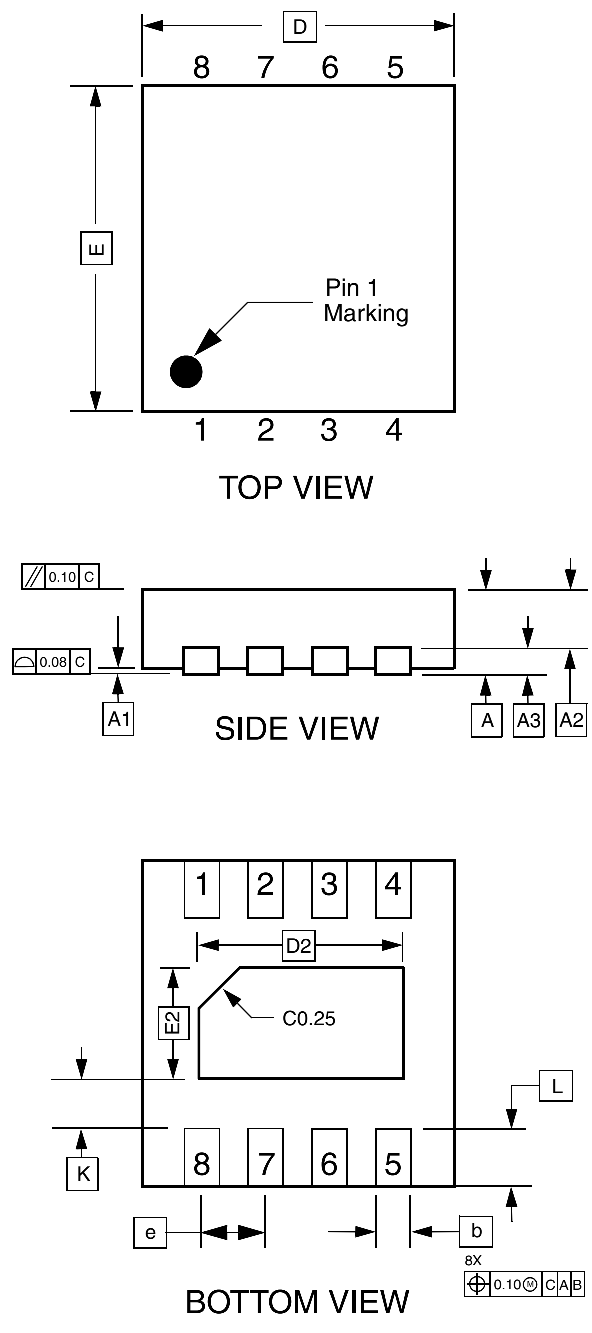
TDFN-08 Mechanical Specifications

The CM3212-02DE is supplied in an 8-lead, 0.65mm pitch TDFN package. Dimensions are presented below.

PACKAGE DIMENSIONS						
Package	TDFN					
JEDEC No.	MO-229 (Var. WEEC-1)*					
Leads	6					
Dim.	**Millimeters**			**Inches**		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.45	0.55	0.65	0.018	0.022	0.026
A3	0.20 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.20	2.30	2.40	0.087	0.091	0.094
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.40	1.50	1.60	0.055	0.059	0.063
e	0.65 BSC			0.026 BSC		
K	0.45 REF			0.018 REF		
L	0.20	0.30	0.40	0.008	0.012	0.016
# per tape and reel	3000 pieces					
Controlling dimension: millimeters						

*This package is compliant with JEDEC standard MO-229, variation VEEC-1 with exception of the D2, E2, and b dimensions as called out in the table above.

Mechanical Package Diagrams



Package Dimensions for 8-Lead TDFN

Mechanical Details (cont'd)

SOIC-8 Mechanical Specifications

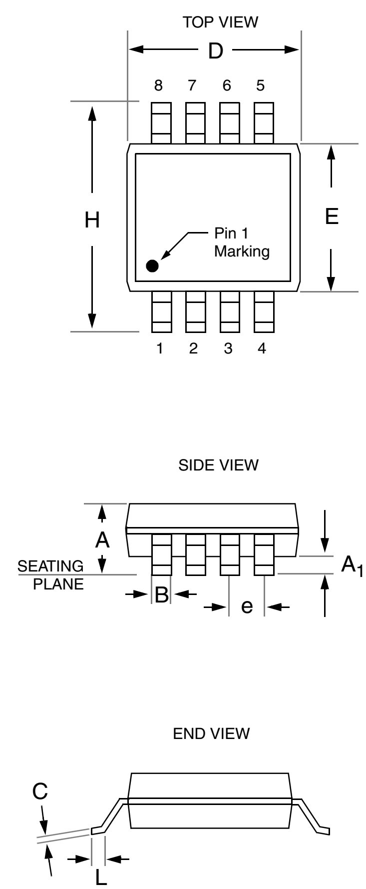
The CM3212-02SM is supplied in an 8-pin SOIC package. Dimensions are presented below.

For complete information on the SOIC-8, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: millimeters				

* This is an approximate number which may vary.

Mechanical Package Diagrams



Package Dimensions for SOIC-8