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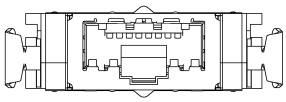
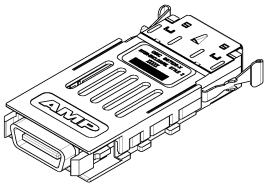
DOC	REV
BD 39	

REVISIONS

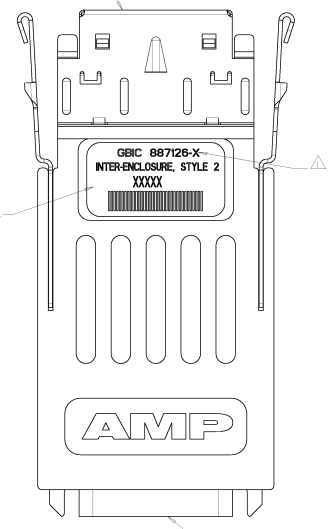
P	LTR	DESCRIPTION	DATE	DWN	APVD
	O	RLSE PER NPR 288	02MAY99	DLB	RF
	A	REVISED PER EC 0S1A-0111-00	15JUN00	JG	AF

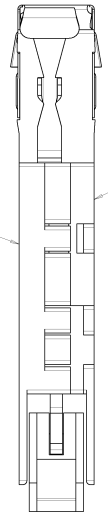


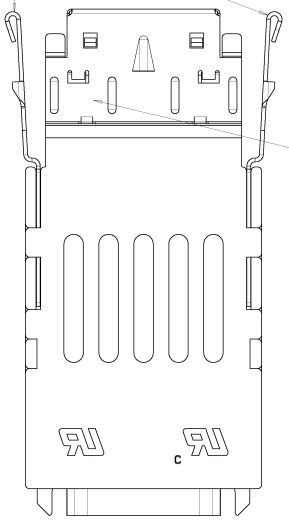


SCALE 2:1

△1 -X DENOTES DASH NUMBER







CHAMP BLINDMATE, SCA 2,
20 POSN, QTY: 1

DESCRIPTION	PART NUMBER
ACTIVE GBIC WITH SERIAL ID	887126-2
ACTIVE GBIC WITHOUT SERIAL I.D.	887126-1

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AMP Incorporated
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DIMENSIONS: mm[INCHES]
TOLERANCES, UNLESS OTHERWISE SPECIFIED:
± PLC ±-
± PLC ±-
± PLC ±-
± PLC ±-
ANGLES ±-
MATERIAL -
FINISH -
WEIGHT -
PROJ. ENG. -
APPLICATION SPEC -

NAME: ASSEMBLY, ACTIVE, HSSDC, GBIC

SIZE A1 | CAGE CODE 00779 | DRAWING NO C-887126 | RESTRICTED TO -

CUSTOMER DRAWING | SCALE 4:1 | SHEET 1 OF 2 | REV A

AMP 4005 REV 27JUN94
Pro/ENGINEER DRAWING

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	-	SEE SHEET 1	-	-	-

TECHNICAL SPECIFICATIONS

Gigabit Interface Converter (GBIC)
Style 2 (HSSDC) Inter-Enclosure

Table 1. CHAMP SCA 2 CONNECTOR PINOUT

Pin #	Pin Name	Description	I/O	Logic Level	Signal specification
1	RX_LOS	Receiver Loss of Signal	Output	TTL	Open collector compatible Pullup to $V_{DD}T$ on host Logic high when V_{input} (receiver)<150mV Logic low when V_{input} (receiver)>400mV Logic high during power-on initialization
2	RGND	Receiver Ground	Input	Ground	Ground, to GBIC
3	RGND	Receiver Ground	Input	Ground	Ground, to GBIC
4	MOD_DEF(0)	Module Definition and presence, bit 0	Output	TTL	Parallel ID, most significant bit, pullup to $V_{DD}T$ on host Logic low on 887126-2 No connection on 887126-1
5	MOD_DEF(1)	Module Definition and presence, bit 1	Output	TTL	Parallel ID, second-most significant bit pullup to $V_{DD}T$ on host SCL on 887126-2 No connection on 887126-1
6	MOD_DEF(2)	Module Definition and presence, bit 2	Output	TTL	Parallel ID, least significant bit, pullup to $V_{DD}T$ on host SDA on 887126-2 Logic low on 887126-1
7	TX_DISABLE	Transmitter Disable	Input	TTL	Open collector compatible pullup to $V_{DD}T$ on GBIC Logic high input disables transmitter
8	TGND	Transmitter Ground	Input	Ground	Ground, to GBIC
9	TGND	Transmitter Ground	Input	Ground	Ground, to GBIC
10	TX_FAULT	Transmitter Fault	Output	TTL	Open collector compatible pullup to $V_{DD}T$ on host High during power-on initialization
11	RGND	Receiver Ground	Input	Ground	Ground, to GBIC
12	-RX_DAT	Receive Data	Output	Differential PECL	High speed differential data from GBIC
13	+RX_DAT	Receive Data	Output	Differential PECL	High speed differential data from GBIC
14	RGND	Receiver Ground	Input	Ground	Ground, to GBIC
15	$V_{DD}R$	Receiver +5 Volt	Input	Power	Power, to GBIC
16	$V_{DD}T$	Transmitter +5 Volt	Input	Power	Power, to GBIC
17	TGND	Transmitter Ground	Input	Ground	Ground, to GBIC
18	-TX_DAT	Transmit Data	Input	Differential PECL	High speed differential data to GBIC
19	+TX_DAT	Transmit Data	Input	Differential PECL	High speed differential data to GBIC
20	TGND	Transmitter Ground	Input	Ground	Ground, to GBIC

Table 2. HSSDC Connector Pinout

Pin #	Pin Name	Description	I/O	Logic Level	Signal Specification
1	+TX	Transmit Data	Output	Differential PECL	High speed differential data from GBIC
2	No Connection	-			
3	-TX	Transmit Data	Output	Differential PECL	High speed differential data from GBIC
4	No Connection	-			
5	No Connection	-			
6	-RX	Receive Data	Input	Differential PECL	High speed differential data to GBIC
7	No Connection	-			
8	+RX	Receive Data	Input	Differential PECL	High speed differential data to GBIC

Table 3. DC Electrical Specifications

T_A = 0°C to +70°C

Parameter	Symbol	Min.	TYP.	Max.	Unit	Conditions
Operating Voltage	$V_{DD}T$ $V_{DD}R$	4.75	5.00	5.25	V	Inclusion of ripple from 0 to 500 KHz
Current	I		130	300	mA	steady state, after t_init
Surge Current	I_{surge}			+30	mA	hot plug, above actual steady state current

Table 4. Low speed control and sense signals, electronic characteristics

Parameter	Symbol	Min.	Max.	Unit	Conditions
TTL Data Input Voltage, Low	V_{IL}	0	0.8	V	4.7kΩ pullup to $V_{DD}T$, measured at GBIC side of connector
TTL Data Input Voltage, High	V_{IH}	2.0	$V_{DD}T$ + 0.3	V	4.7kΩ pullup to $V_{DD}T$, measured at GBIC side of connector
TTL Data Output Voltage, Low	V_{OL}	0.0	0.5	V	4.7kΩ to 10kΩ pullup to host_V_{CC}, measured at host side of connector
TTL Data Output Voltage, High	V_{OH}	host_V_{CC}-0.5	host_V_{CC} + 0.3	V	4.7kΩ to 10kΩ pullup to host_V_{CC}, measured at host side of connector

Table 5.Required electrical signal interface to GBIC from host

Parameter	Symbol	Min.	Max.	Unit	Conditions
PECL amplitude	V_I	650	2000	mV	differential, pk-pk
Deterministic Jitter	$DJ_{elec-xmt}$		0.12	UI	pk-pk
Total Jitter	$TJ_{elex-xmt}$		0.25	UI	pk-pk
PECL rise/fall		100	350	ps	20-80%, differential
differential skew			20	ps	

Table 6. Electrical signal interface from GBIC to host

Parameter	Symbol	Min.	Max.	Unit	Conditions
PECL amplitude	V_O	370	2000	mV	differential, pk-pk
Deterministic Jitter	$DJ_{elec-xmt}$		0.36	UI	pk-pk
Total Jitter	$TJ_{elex-xmt}$		0.56	UI	pk-pk
PECL skew			205	ps	20-80%, differential

Table 7. Timing Parameters for GBIC Management

Parameter	Symbol	Min.	Max.	Unit	Conditions
TX_DISABLE assert time	t_off		10	µsec	Rising edge of TX_DISABLE to fall of output below 10% of nominal
TX_DISABLE negate time	t_on		1	msec	Falling edge of TX_DISABLE to rise of output signal above 90% of nominal
Time to initialize, includes reset of TX_FAULT	t_init		300	msec	From power on or hot plug after $V_{DD}T$>4.75 volts
TX_DISABLE time to start reset	t_reset	10		µsec	TX_DISABLE HIGH before TX_DISABLE set LOW
RX_LOS assert delay	t_loss_on		100	µsec	From detection of loss of signal to assertion of RX_LOS
RX_LOS negate delay	t_loss_off		100	µsec	From detection of presence of signal to negation of RX_LOS

Table 8. Insertion, Extraction, and Retention Forces

Measurement	Minimum	Maximum	Units	Conditions
GBIC Insertion	0	20	newtons	
GBIC Extraction	0	15	newtons	
GBIC Retention	130	N/A	newtons	straight out
Insertion/Removal Cycles	100		cycles	

Table 9, General Specification

Parameter	Value
Distance, 100-XX-EL-S	TP cable, 0-28 meters TW cable, 0-33 meters
Data Rate	1062.5 Mbit ±100 ppm (100-TW-EL-S) 1062.5 Mbit ±100 ppm (100-TP-EL-S) 1.25 Gbit IEEE802.3z, 1000BASE-CX
Data Format	8B/10B
Link Characteristic Impedance	150±10 Ohms
Transmitted signal	1100-2000 mv, differential PECL, measured at HSSDC
Received signal requirement	400-2000 mv, differential PECL, measured at HSSDC

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DWN T.A.MAYER 18APR99
CHK A.L.HERB 18APR99
APVD D.ELCKLINGER 19APR99
PRODUCT SPEC -
APPLICATION SPEC -
WEIGHT -

CUSTOMER DRAWING

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Harrisburg, PA 17105-3608

NAME ASSEMBLY, ACTIVE, HSSDC, GBIC

SIZE A | CAGE CODE | DRAWING NO 00779 | C-887126 | RESTRICTED TO -

SCALE 4:1 | SHEET 2 OF 2 | REV A

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